ECE210-Intro. Digital Logic Design

LAB 1: – Simple AND-OR-NOT Circuits

Fall 2024

DATES

Date	Section	Time
08-Oct-2023	D21	08:00AM - 10:50AM
	D25	02:00PM - 04:50PM
09-Oct-2023	D31	08:00AM - 10:50AM
10-Oct-2023	D45	02:00PM - 04:50PM
15-Oct-2023	D22	08:00AM - 10:50AM
	D26	02:00PM - 04:50PM
16-Oct-2023	D32	08:00AM - 10:50AM
17-Oct-2023	D46	02:00PM - 04:50PM

INTRODUCTION

In this laboratory, students will engage in the development of combinational logic circuits, initially utilizing basic AND, OR, and NOT logic gates. Following this, they will code their solutions using VHDL, utilizing the Xilinx Zybo Z7 FPGA development board along with the Vivado software. This lab serves as a crucial stepping stone, providing a transition from circuit prototyping with Integrated Circuits (ICs) to Field-Programmable Gate Arrays (FPGAs).

LEARNING OBJECTIVES

Upon completion of this laboratory exercise, students will be able to:

1. Demonstrate a comprehensive understanding of the fundamental concepts and operations of combinational logic circuits, including **AND**, **OR**, and **NOT** logic gates.
2. Apply knowledge of Karnaugh Maps (K-maps) in the design and optimization of logic circuits.
3. Integrate the theoretical knowledge of digital logic design with practical skills in FPGA development, K-map optimization, and circuit monitoring, preparing for more advanced studies and applications in the field of electronics and digital system design.
4. Utilize VHDL programming to implement and validate logic circuit designs on the Xilinx Zybo Z7 FPGA development board using the Vivado software.
5. Acquire hands-on experience prototyping circuits by building them on a breadboard and also more versatile methodologies like programming Field-Programmable Gate Arrays (FPGAs) using VHDL.
6. Develop proficiency in utilizing the Analog Discovery 2 for real-time monitoring of circuit inputs and outputs, aiding in performance analysis and troubleshooting.

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PRE-LAB

You are expected to first read the lab instructions and background and then complete the pre-lab assignment before attending the lab sessions. The pre-lab assignment must be submitted on eClass and no late submission is accepted. You are responsible for including your pre-lab assignment as an appendix to your lab report if necessary. Refer to Tutorial Lab as well to refresh lessons learnt.

Logic equation(s) minimization using Karnaugh Map (K-Map):

a. Simplify the logic relationship between inputs A,B,C & D to outputs F1 and F2 using K-Map, helping us find the simplest logic equation for any given truth table. (Prelab write up required).

Inputs				Output 1	Output 2
A	B	C	D	F1	F2
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	1	0
0	1	0	0	x	0
0	1	0	1	x	0
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	x	1
1	0	0	1	x	1
1	0	1	0	x	1
1	0	1	1	x	0
1	1	0	0	x	1
1	1	0	1	x	1
1	1	1	0	x	1
1	1	1	1	x	0

b. Draw the schematic diagram of minimized equations using only AND, OR and NOT gates. (Pre-lab write up required).

c. It's highly recommended to finish breadboarding of minimized functions (F1, F2) before coming to the lab, this will help you accomplish assigned tasks within lab time. If you aren't familiar with breadboarding, you must watch the tutorial videos posted on eClass, helping you understand the basics on how to use the breadboard to build a circuit. (no write up required).

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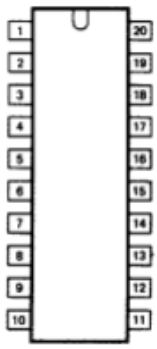
BACKGROUND

Integrated Circuits (IC's) pinouts and packaging forms:

The primary categorization of IC packaging can be divided into two groups: **through-hole** and **surface mount**. ICs are available in a variety of packaging forms, each offering its unique set of features and uses. Key types include **DIP** (Dual In-line Package), **SOIC** (Small Outline Integrated Circuit), **QFP** (Quad Flat Package), and **BGA** (Ball Grid Array). The following table offers a comparative view of these popular IC packaging forms.

Package Names, relevant questions and answers	Pictorial Looks
Dual-In-Line Package (DIP) DIP is a through-hole type and has two rows of pins intended for insertion into a breadboard or PCB.	
Where is DIP package pin #1? **Answer:** Seeing the package from the top, one can see a notch in the top middle or a circle on the top left hand side or both, as shown in the pictures. The top left pin is #1 and the pin numbering goes as shown and in the respective IC datasheet.	 
Small outline integrated circuit (SOIC) A smaller, surface mount type, is designed for situations where space efficiency is crucial.	 
Where is SOIC package pin #1? Same as described for DIP packages.	

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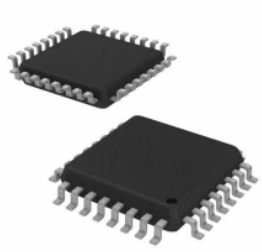
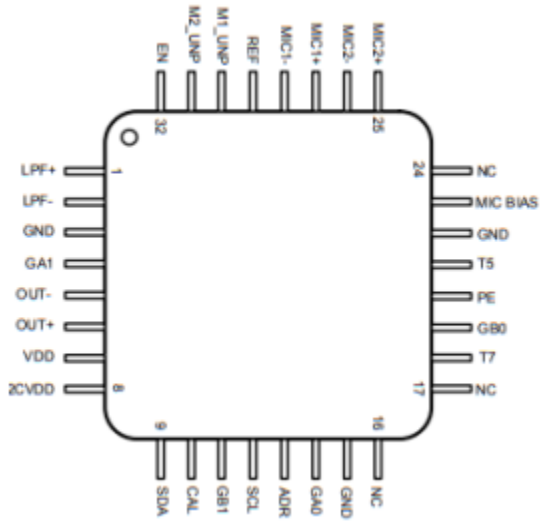
Quad Flat Pack (QFP)
Another surface mount type, has four sides of pins and is useful for higher pin count applications.



Where is QFP package pin 1?
Top left has the etched circle or cut corners as shown.

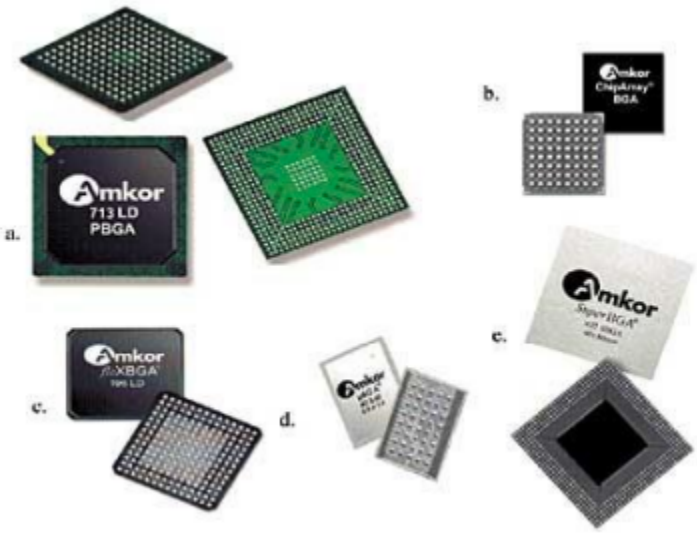
click here to see an example from a component datasheet



Ball Grid Array (BGA)
Known for its underside grid of solder balls, allows for even higher pin densities and improved heat dissipation.

Where is BGA package pin #1
An etched circle, marked line, cut corners or all combined on the top left hand side of the package. Refer to package datasheet for pinout details.

click here to see an example from a component datasheet



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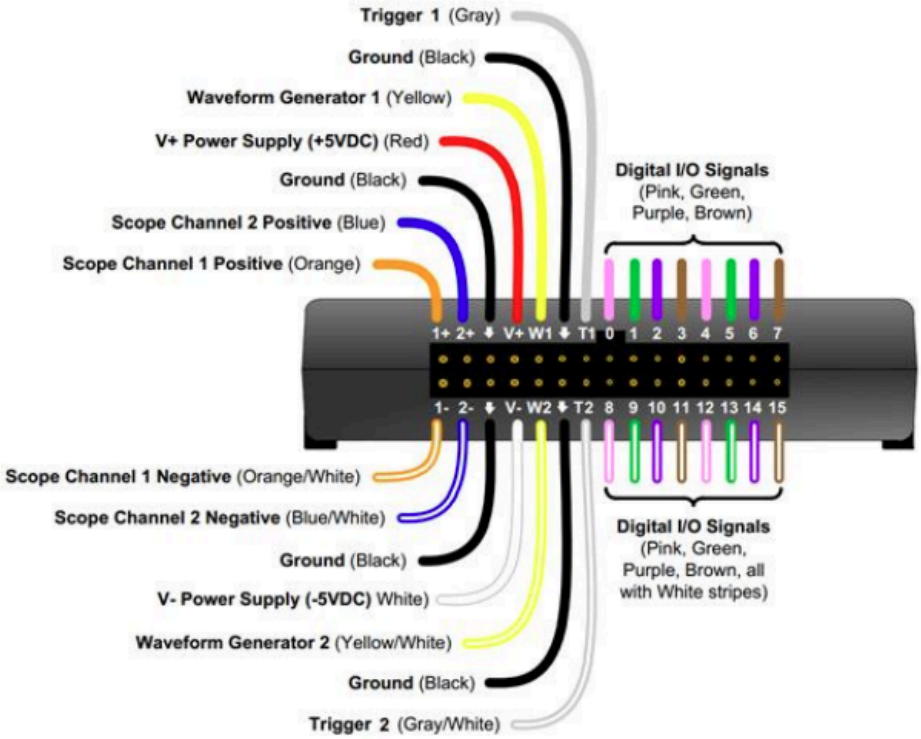
LAB HARDWARE

Students will use Digilent Analog Discovery 2 hardware to complete this lab. Let's get you introduced to this hardware tool.

Key features and associated details:

- ➔ 30MHz bandwidth 2 channel (1+, 1-and 2+, 2-) oscilloscope.
- ➔ 12MHz bandwidth 2 channel (W1, W2) waveform generator.
- ➔ One positive supply channel (V+) of up to +5 volts.
- ➔ One negative supply channel of (V-) up to -5 volts.
- ➔ Two channels for external triggering (T1, T2).
- ➔ 16-channel (0-15) digital logic analyzer.
- ➔ ↓ => Ground (GND) lines.

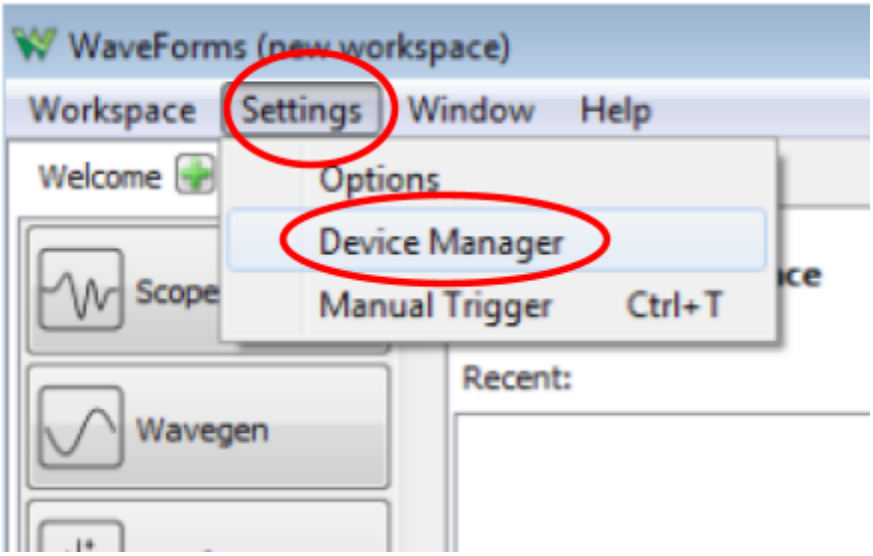


DIGILENT ANALOG DISCOVERY 2

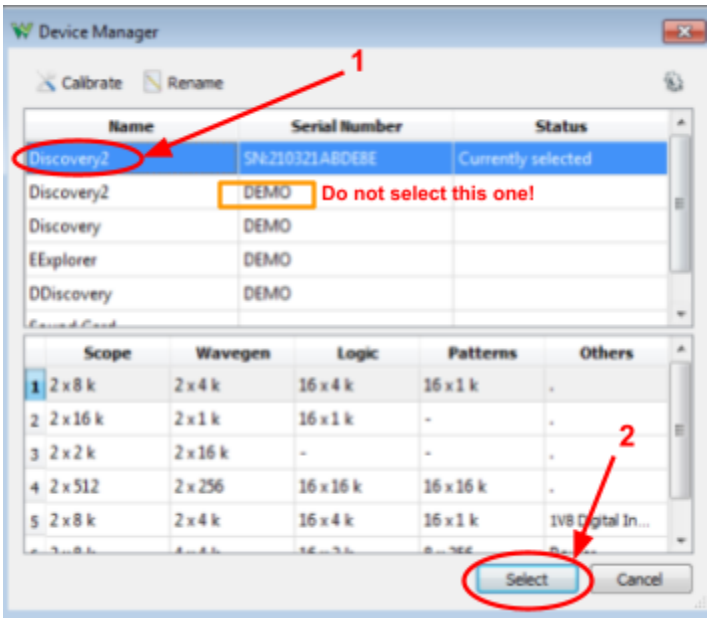
WaveForms is the software for Analog Discovery 2 and here are details on how to use it.

1. Doubleclick on Waveforms icon on desktop 

OR click
Start→All Programs→Digilent→Waveform Applications→Waveforms
2. Click on the **Settings** menu and select Device Manager.

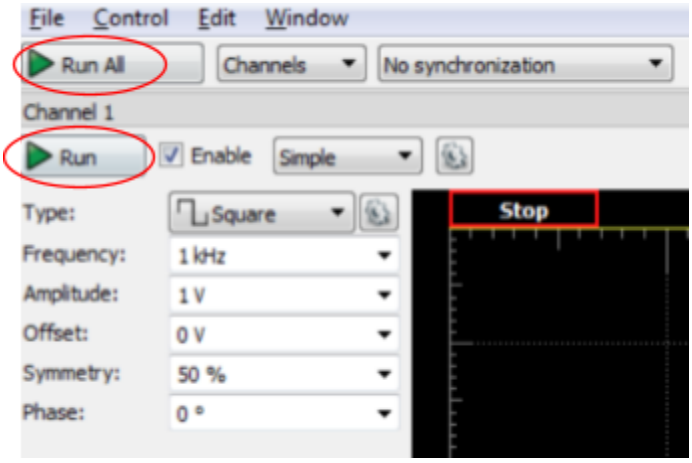


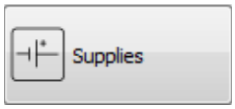
3. Select "**Discovery2**" and click "**Select**" on bottom right. This will bring you back to the main screen.



4. Click on the Wavegen button 

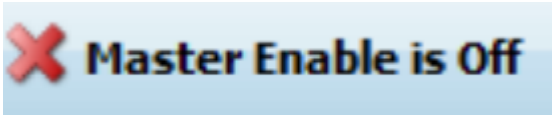
to open the waveform generation tab. Click the "**Run All"** or "**Run**" button.



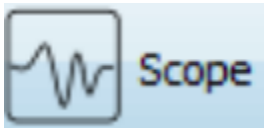
a. Click on the Supplies button 

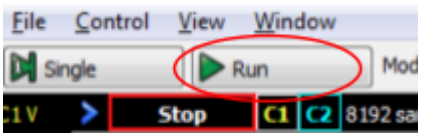
to open the DC power supply generation tab.

b. Select **5V** 

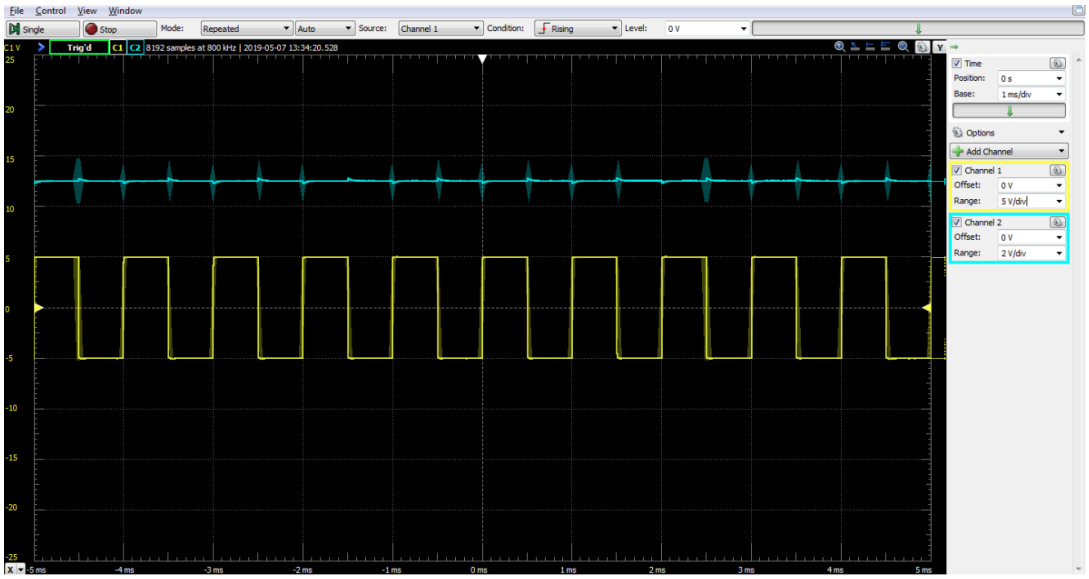
for **V+** and click on 

to turn it on.

c. Click on Scope button 

to open oscilloscope channels monitoring tab and click **Run** 

5. This step is only for students to learn the capabilities offered by Digilent Analog Discovery. Students may or may not use the waveform generator capability of Analog Discovery in this lab.
   a. Connect waveform generation W1 channel with oscilloscope channel 1+ and power supply V+ channel with 2+, using male header pins or stripped wires.
   b. You will get the following view depending on your selection on the right hand side menu options.



6. Learn how to use the voltmeter. Turn the voltmeter selector knob from off to DC voltage, make sure the red voltmeter cable is inserted in and black cable is inserted into . Now touch the red cable with V+ output channel and black to ⏚ (GND) to see results.

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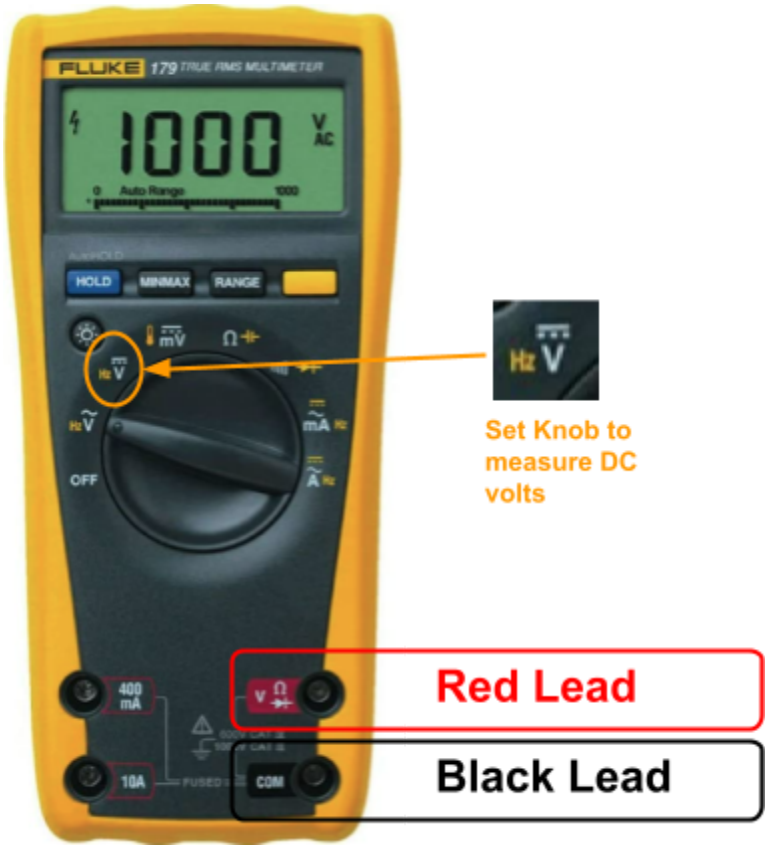

Students should now be comfortable in using additional lab resources to what they learnt in Lab 0 to complete this lab, any questions kindly seek guidance from lab teaching staff.

Note 1: Human touch to an IC package pins without properly grounding their body can potentially damage the IC due to the body's static electricity discharge to IC. Lab teaching staff will demonstrate how to hold and use IC packages.

Note 2: In this lab we will only be working with DIP IC packages.

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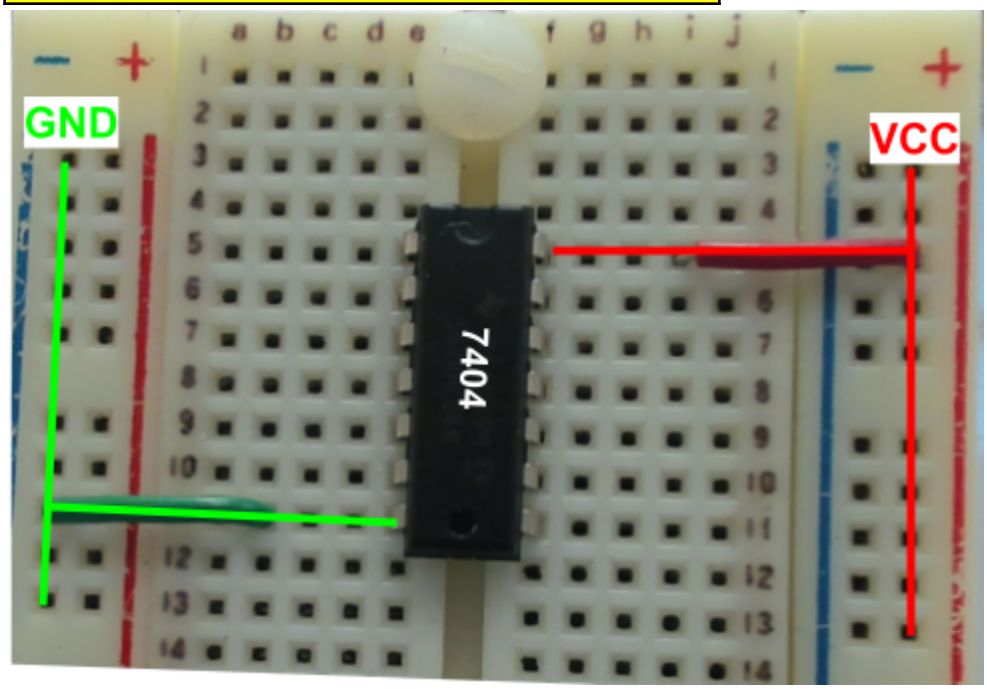
LAB COMPLETION REQUIREMENTS

1. Implement your pre-lab design using breadboard, stripped wires and AND, OR, NOT logic gates, for F1 and F2. Relevant components datasheets will provide all information required to complete this section of the lab. Use voltmeter to verify a few cases.

Note 3: Use the V+ DC supply output to power IC's. Refer to the IC datasheet to find the pinout and connect VCC and GND appropriately



Note 4: The use of pull up and pull down resistors is a common practice in digital electronics by ensuring that the input pins are always in a well-defined state, either 'HIGH' (logic 1) or 'LOW' (logic 0) to prevent 'floating' states from generating noisy signals that might interfere with the circuit's expected behavior. In the next drawing and picture you can see the schematic diagram and breadboard connections for both of these.

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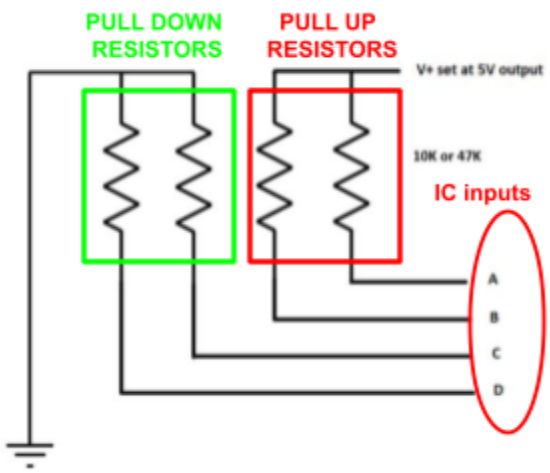
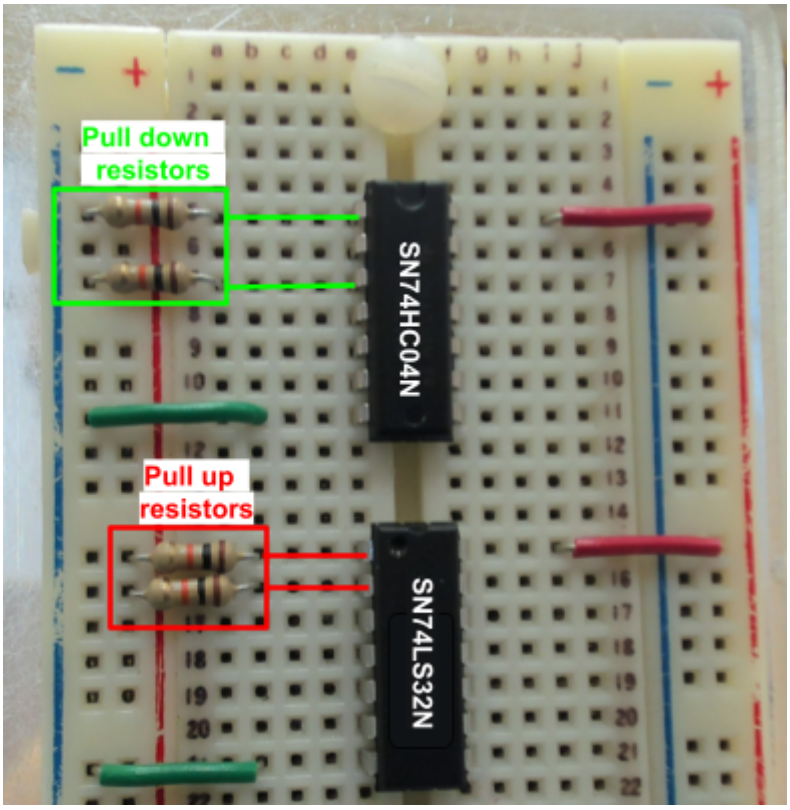




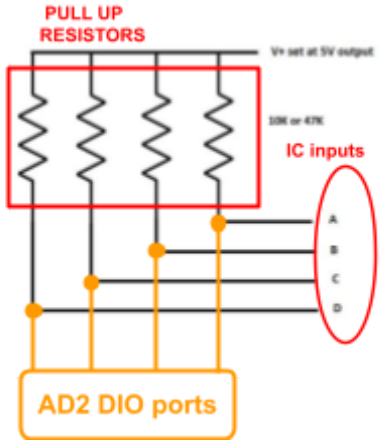
Note 4: With pull up/down resistors in place you can connect the DIO ports from the Analog Discovery 2 as you would connect normal inputs, this approach guarantees that the inputs will always have a defined value in case the input is left 'floating'

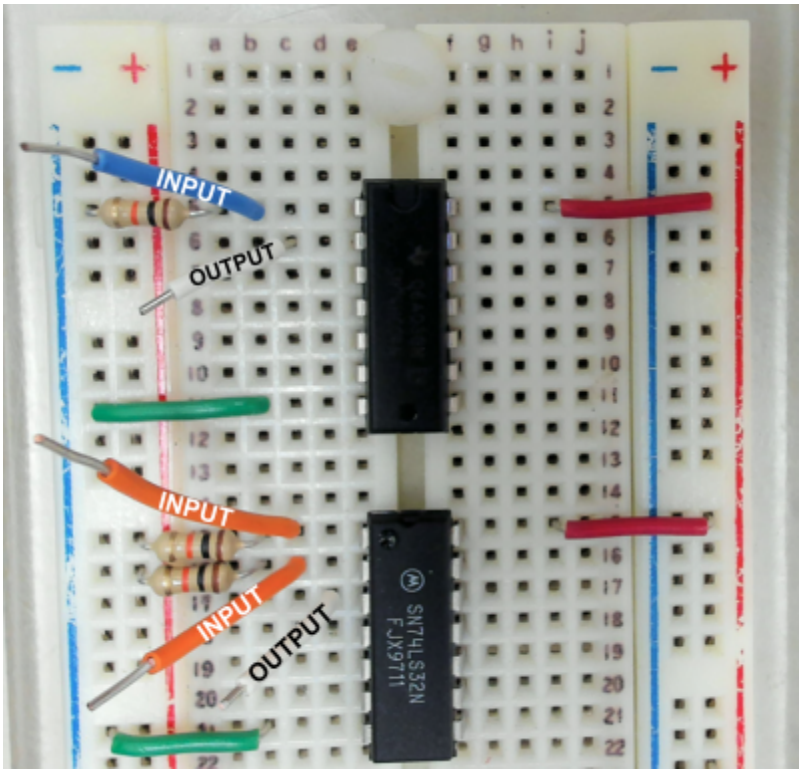
Instead of connecting your inputs to power and ground through the pull up or pull down resistors, connect them to the DIO ports of the AD2(Analog Discovery 2)

AD2 port	Input
DIO0	A
DIO1	B
DIO2	C
DIO3	D

AD2 port	Output
DIO4	F1
DIO5	F2

Using the patterns window and the logic window, you can test your circuit.



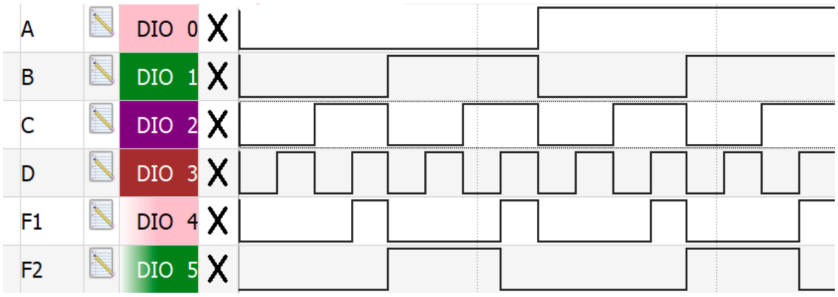


Note 5: The circuits depicted in the previous illustrations serve only as a demonstrative example and should not be construed as a solution to the exercise problem. They are intended to illustrate key concepts and assist you in understanding the overall layout and connections. Students are expected to refer to relevant IC datasheets to find pinouts and make the required connections to implement the solution for F1 and F2.

Open the **patterns window** and set up input patterns as shown in the next picture:

Name	Pin	Output	Type	Parameter1
A	DIO 0	PP	Clock	1 Hz
B	DIO 1	PP	Clock	2 Hz
C	DIO 2	PP	Clock	4 Hz
D	DIO 3	PP	Clock	8 Hz

In the **logic window**, add the input and output signals (DIO0 to DIO5) as shown in the next picture. Change the scan mode to "**Shift**" and then click on **Scan**. You should be able to see the patterns live, for both the inputs and outputs. Click on Stop and capture all cases. Include such snapshots in your report.



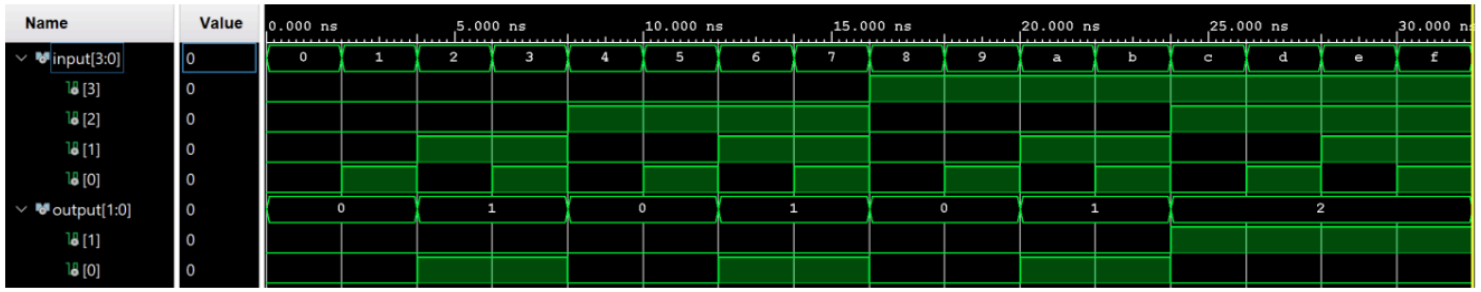
2. Implement pre-lab work using VHDL and show simulation test cases results. Open a new project in Vivado, follow the same steps mentioned in lab 0. Download **lab1.vhd**, **lab1_tb.vhd**, and **const.xdc** from e-class and add them to your project. Complete source file, lab1.vhd. Assume:

sw(0)= A
sw(1)= B
sw(2)= C
sw(3)= D
led(0)= F1
led(1)= F2

```
led(0) <= ( sw(??) and sw(??) ) or sw(??); -- Sample solution for F1
led(1) <= ( sw(??) and sw(??) ) or ( sw(??) and sw(??) ); -- Sample solution for F2
```

Implement and demonstrate your design on the Zybo Z7 board.

Note 6: Don't try to match your test cases with the picture shown below, since it most likely won't match yours given that your design might be different.



DOCUMENTATION

This lab exercise requires a formal report. This report is due within two weeks of completing the lab and must be uploaded to the appropriate submission link on eClass. Don't forget to include your name, section number, and lab number on the title page, and follow the guidelines described on eClass. Hand written reports will not be accepted. Items your report should include are:

1. Your name, section number, and lab number on the title page.
2. The pre-lab assignment.
3. Photos of breadboard from Requirement 1.
4. Screenshots of logic window from Requirement 1.
5. Code written for Requirement 2.
6. Screenshot of simulation window from Requirement 2.
7. **Organized and written as per guidelines on eClass.**

REFERENCES

- References
- Zybo Z7 Documentation, Tutorials and Example Projects
- Zybo Z7 Reference Manual
- "Introduction to Logic Circuits & Logic Design with VHDL" ; Brock J. LaMeres; Pub. Date: 2019 Springer Nature Switzerland AG; Print ISBN: 978-3-030-12488-5

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MARKING GUIDELINES

Student Names:_____

_____

Pre-Lab

(15) Derivation of Output Equations for F1 and F2

(15) Schematics (hand drawn or using any tool of your choice)

Sub-total_____/30

In-Lab

(20) Requirement 1

(20) Requirement 2

TA Signatures:_____ Sub-total_____/40

Lab Report

(06) Title Page Abstract, and Introduction

(12) Design Section and Procedure:

- i. The pre-lab solution (2)
- ii. Photos of breadboard from Requirement 1 (4)
- iii. Code written for Requirement 2 (4)
- iv. Some brief explanation (2)

(12) Results, Discussion and Conclusion:

- i. Screenshots of the logic window from Requirement 1. (4.5)
- ii. Screenshot of simulation window from Requirement 2. (4.5)
- iii. Discussion (1.5)
- iv. Conclusion (1.5)

Sub-total_____/30

Lab Report Total_____/100