



ECE210-Intro. Digital Logic Design

LAB 3:7-Segment LED Decoder

Fall 2024

DATES

Date	Section	Time
Nov 05-2024	D21	08:00 - 10:50 AM
	D25	02:00 - 04:50 PM
Nov 06-2024	D31	08:00 - 10:50 AM
Nov 07-2024	D45	02:00 - 04:50 PM
Nov 19-2024	D22	08:00 - 10:50 AM
	D26	02:00 - 04:50 PM
Nov 20-2024	D32	08:00 - 10:50 AM
Nov 21-2024	D46	02:00 - 04:50 PM

INTRODUCTION

In this lab, we will implement a 7-Segment LED decoder displaying the hex value of binary inputs (SW0- SW3). Students will then learn implementing a binary up counter (0 to F) every second and the value displaying on 7-Segment LED. The 7-Segment LED decoder will be implemented using VHDL, simulation test bench for verification, implementing it on Zybo Z7 board.

LEARNING OBJECTIVES

Upon completion of this laboratory exercise, students will be able to:

- Implement a 7-segment decoder and display switches (SW0-SW3) data.
- Implement a two-digit decimal up counter.



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PRELAB

You are expected to read the lab instructions and complete the pre-lab assignments before attending the lab sessions. You are responsible for submitting your pre-lab assignment in time in the drop-box on eClass.

1. Given the truth table below, Use K-Maps, determine the minimum logical expression for each of the 7 outputs (A through G):

Switches Input				Selected 7-Segment Binary Inputs								Display
					out_7seg(6)	out_7seg(5)	out_7seg(4)	out_7seg(3)	out_7seg(2)	out_7seg(1)	out_7seg(0)	
SW3	SW2	SW1	SW0	CC	A	B	C	D	E	F	G	
0	0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	0	0	0	0	1	1	0	1
0	0	1	0	0	1	1	0	1	1	0	1	2
0	0	1	1	0	1	0	0	1	1	1	1	3
0	1	0	0	0	0	0	1	0	1	1	1	4
0	1	0	1	0	1	0	1	1	0	1	1	5
0	1	1	0	0	1	1	1	1	0	1	1	6
0	1	1	1	0	0	0	0	1	1	1	0	7
1	0	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	1	0	1	1	1	1	1	9
1	0	1	0	0	0	1	1	1	1	1	1	A
1	0	1	1	0	1	1	1	0	0	1	1	b
1	1	0	0	0	1	1	1	1	0	0	0	C
1	1	0	1	0	1	1	0	0	1	1	1	d
1	1	1	0	0	1	1	1	1	0	0	1	E
1	1	1	1	0	0	1	1	1	0	0	1	F

Note: The provided truth table has been designed in accordance with the inverted schematic presented in the manual. This is due to the particular orientation of the Zybo boards when mounted to the lab bench, which results in the display of digits in an upside-down fashion. Therefore, be mindful when interpreting the truth table and correspondingly programming your display to ensure accurate output, reflecting this unique setup of the Zybo boards in our lab environment.



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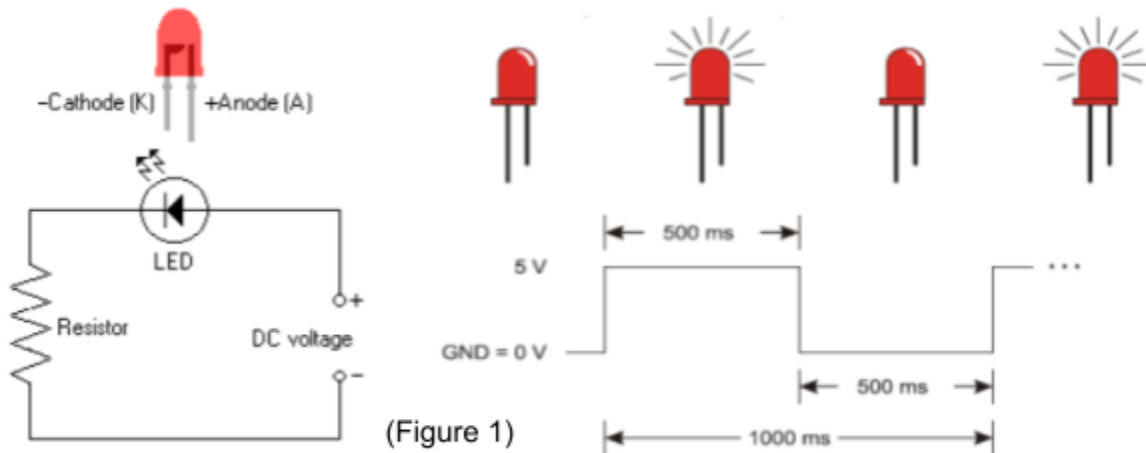
2. Draw circuit schematic diagram using minimized logical expressions, either use all AND-OR-NOT logic or all NAND logic gates.
3. Write and include VHDL solutions in your pre-lab assignment (using VHDL logical operators, such as AND, OR, etc).
4. Please watch the following video to get familiar with implementing a complete truth table using VHDL conditional statements: [VHDL essentials 10 majority architecture](#).

NOTE: It is very important that you complete the pre-lab components before you come to the lab. Failing to do so will impede your ability to complete the lab within the allotted time.



BACKGROUND

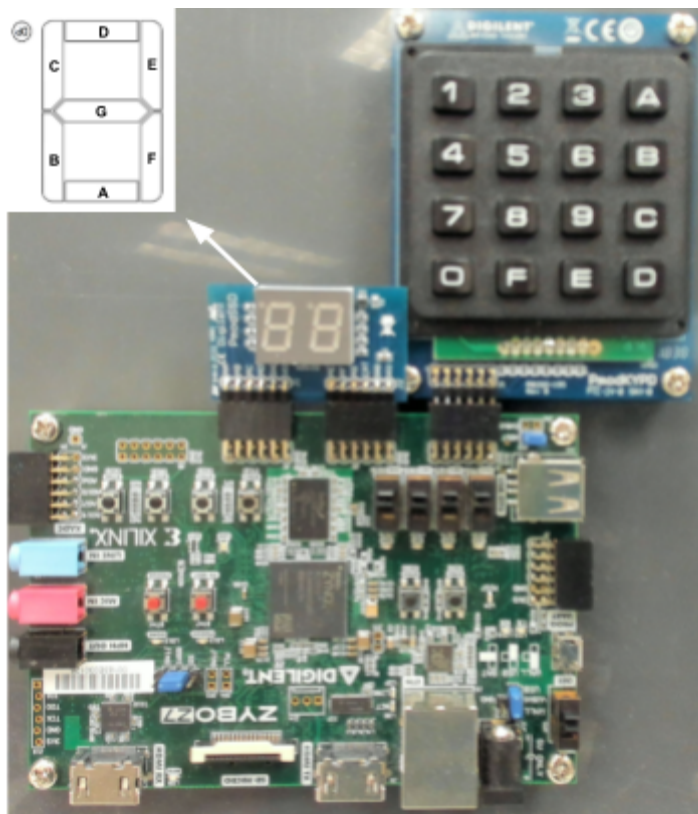
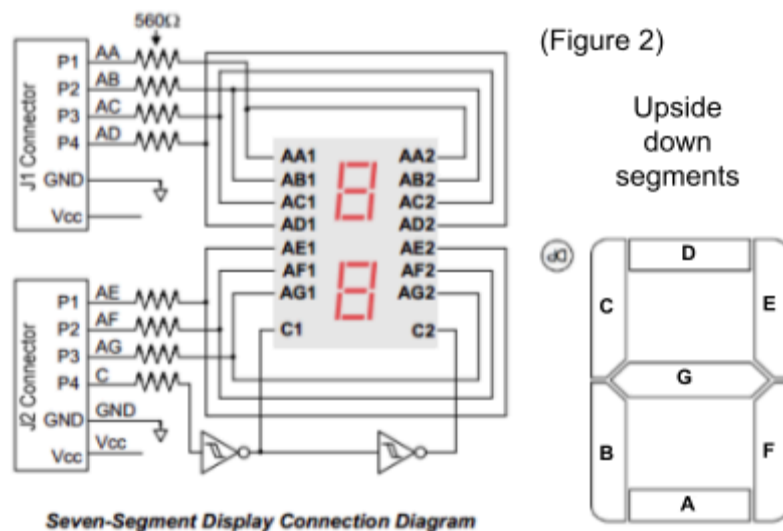
A 7-Segment display as shown below is manufactured using 7-LED's (segments A, B, C, D, E, F, G), as shown in Figure 2. An LED (Light Emitting Diode) emits light when the Anode is connected with the positive side of DC voltage and the cathode is connected with the negative side, as shown below. Such a connection enables current to flow through the diode, enabling it to emit light.



There are two standard types of 7-Segment displays; Common-Anode and Common-Cathode. The 7-Segment board connected with Zybo Z7 has Common-Cathode configuration, as shown in the schematic below.



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Common-Anode or **Common-Cathode** configuration reduces the number of pins necessary to operate the device, and also provides a global ON or OFF control. In this digital system, logic '1' is equivalent to +3.3 volts and logic '0' is equivalent to 0 volts.

Note: Due to the unique constraints of our lab setup, specifically the manner in which the Zybo boards are mounted to the bench, it isn't feasible to orient both the seven-segment display and the keypad in the standard 'right side up' position simultaneously. After careful consideration, we have opted to adhere to an upside-down representation to match the physical orientation of the seven-segment display on the Zybo board.

As you can see both on the schematic above and the 7-Segment board connected to the Zybo Z7, we have two 7-Segments. **In order to turn ON a segment on the first 7-Segment:**

1. We must first apply logic '0' to the cathode signal (C=>P4 pin), which makes C1 logic '1'.
2. Then apply logic '1' to the respective segment (AA to AG) you want to turn ON.

To select and display on second 7-Segment, follow these steps:

1. Apply logic '1' to the cathode signal (C=>P4 pin), which makes C2 logic '1'.
2. Then apply logic '1' to the respective segment (AA to AG) you want to turn ON.



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PART 1: 7-SEGMENT DECODER IMPLEMENTATION

1. Download from eClass: design source, constraint file, and simulation test bench.
2. Create a new VHDL project to implement your minimized logical equations for all segments (the pre-lab work).
3. Demo your work to a TA or LI for a checkoff and present simulation results in your lab report.

PART 2: 7-SEGMENT DECODER IMPLEMENTATION USING VHDL

1. Implement 7-segment decoder design using VHDL **if-else or case statement**. You can find an introduction to these statements in VHDL in this video: [VHDL essentials 10 majority architecture](#).
2. Demo your works to a TA or LI for a checkoff and present simulation results in your lab report.

PART 3: COUNTER FROM 0 TO LAST 2 DIGITS OF STUDENT ID

1. Download from eClass: design source, constraint file, and simulation test bench.
2. Create a new project and complete the design source. Comments in the design source explain what needs to be done. You are required to simulate and implement an up counter starting from 0 to the last 2 digits of your student ID in decimal.
Note: If the last 2 digits of your student ID are less than 10, please choose any number greater than or equal to 10.
Hint: CC signal can toggle between '0' and '1'. While it is zero, you are displaying 4 bits on one 7-segment. While it is one, you are displaying another 4 bits on the other 7-segment.
3. Demo your work to a TA or LI for checkoff and present simulation results in your lab report.



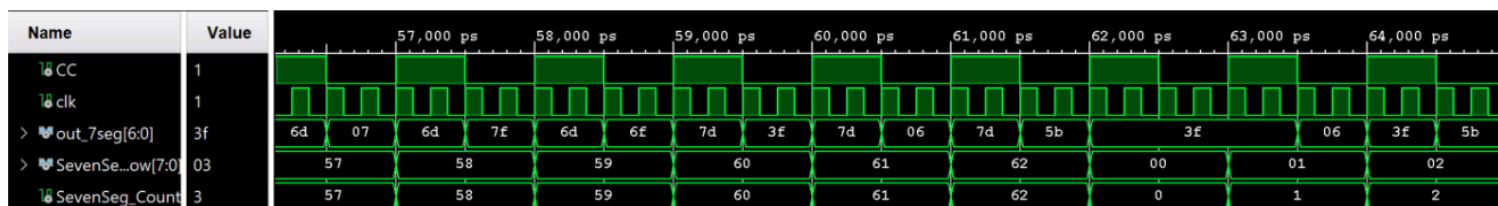
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REPORT REQUIREMENTS

1. Simulation results of parts 1 and 2 for digit 0 to F.
2. Codes for parts 1, 2 and 3.
3. Simulation results for part 3. (Showing up counting to the last two digits of your student ID and starting back from zero. For example, Student ID = *****62)

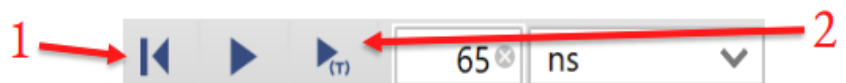


Note: In order to show signals in your waveform window, on the scope select your design source. Right click on the signal and select Add to waveform window

Scope
Sources
Na... Design Unit Block Type
Seven_Segments_tb(Behavior) VHDL Entity
SevenSegments2digits(Behavior) VHDL Entity

Objects
Protocol Instances
Name Value Data Type
clk 1 Logic
CC 1 Logic
out_7seg[6:0] 3f Array
count[7:0] 00 Array
count_7seg[7:0] 00 Array
clk_out_7seg 1 Logic
SevenSeg_Count 3 Integer
SevenSeg_show[7:0] 03 Array
clk_divider_forOneHz 3 Integer
clk_divider_for7seg 1 Integer
countwidth 8 Integer
max_SevenSeg_Count 62 Integer

Note: In order to run the simulation as long as your student ID, click on 1 to reset it, then set a time in ns (suggested time: last 2 digits of your student ID + a few ns e.g., 65 for someone with the last two digits equal to 62). Then click on 2 to run the simulation.





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REFERENCES

- [Zybo Z7 Documentation, Tutorials and Example Projects,](#)
- [Zybo Z7 Reference Manual](#)
- [PMOD Seven Segment display Reference Manual](#)



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MARKING GUIDELINES

Student Names:_____

Pre-Lab

- (15) Derivation of minimized equations for 7-segment display.
- (15) Schematic of minimized logic using AND-OR or NAND logic.
- (05) Handwritten or electronic version of VHDL solution(s).

Sub-total_____/35

In-Lab

- (10) Lab3 Part #1
- (10) Lab3 Part #2
- (20) Lab3 Part #3

TA Signatures:_____ Sub-total_____/40

Lab Report

- (05) Title page, Abstract and Introduction.
- (10) Design section and procedure.
 - (1) Circuit diagrams for part I (from pre-lab if correct)
 - (1) Logic expressions for part I (from pre-lab if correct)
 - (2) Code for part I
 - (2) Code for part II
 - (1) Code for part III
 - (3) Explanation for part III code (General description of the whole VHDL design)
- (10) Results, Discussion, and Conclusion.
 - (3) Simulation result for part I
 - (3) Simulation result for part II
 - (3) Simulation result for part III
 - (1) Discussion and Conclusion

Sub-total_____/25

Lab Report Total_____/100