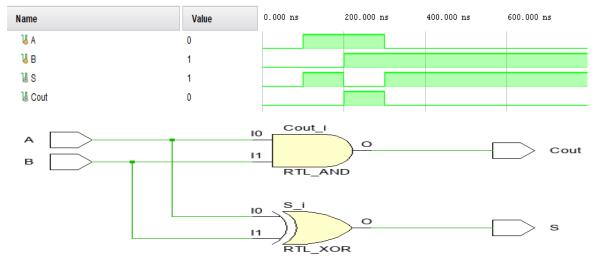
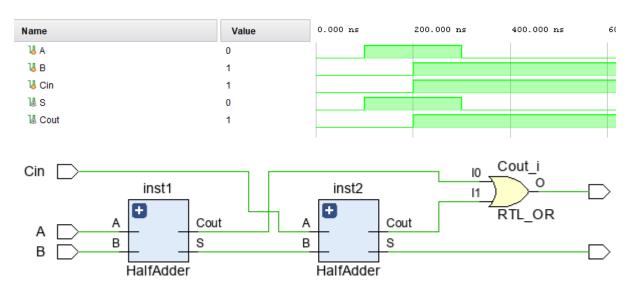
Simulation and RTL synthesis of designed modules

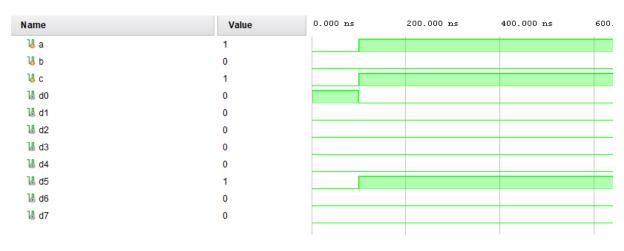
Half Adder

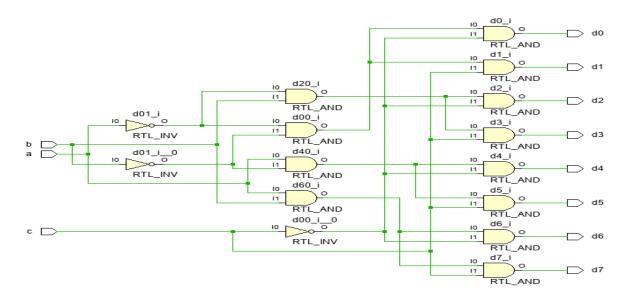


Full Adder

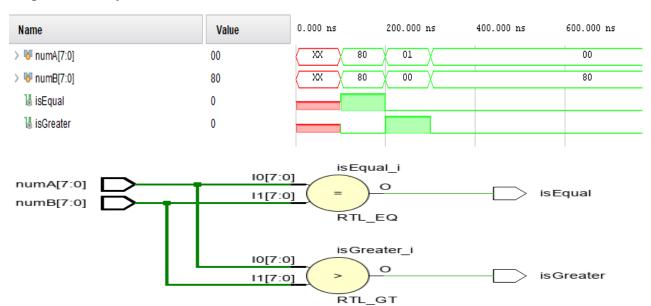


Decoder 3x8

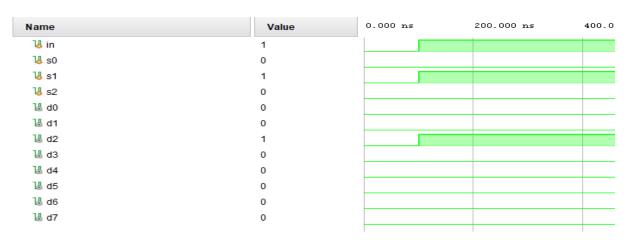


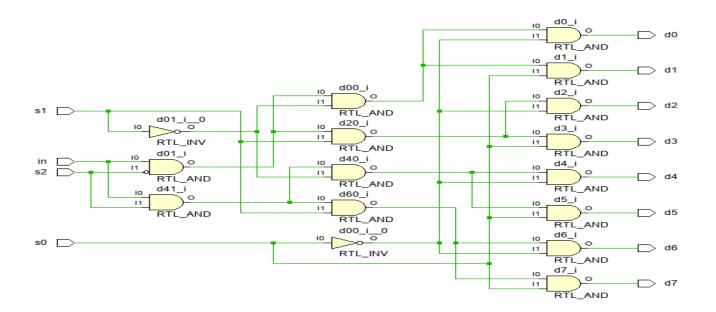


Magnitude Comparator

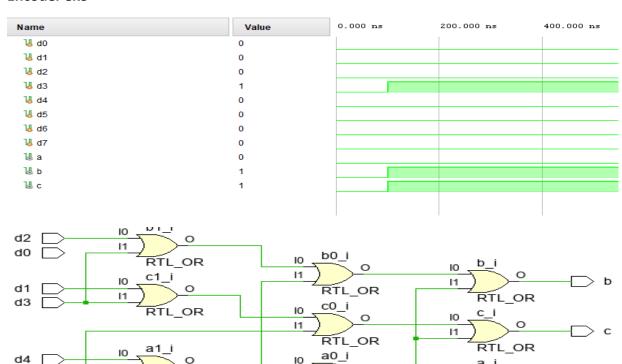


Demux 8x1





Encoder 8x3



0

RTL_OR

10

RTL_OR

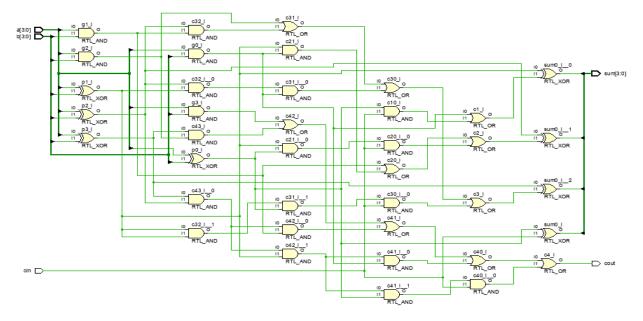
Carry Look Ahead Adder

RTL_OR

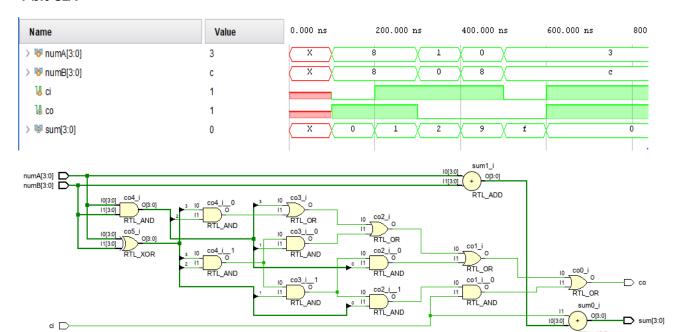
d5

d6 d7

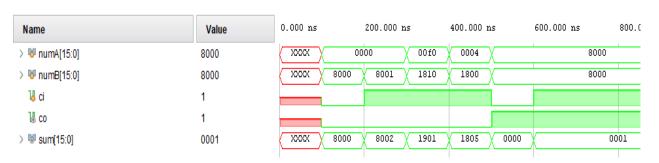
Name	Value	0.000 ns	200.000 ns	400.000 ns	600.
> 💗 a[3:0]	5	0 \	1	5	'
> 😽 b[3:0]	6	0		6	
¹ √s cin	1				
> 😻 sum[3:0]	С	0		С	
¼ cout	0				



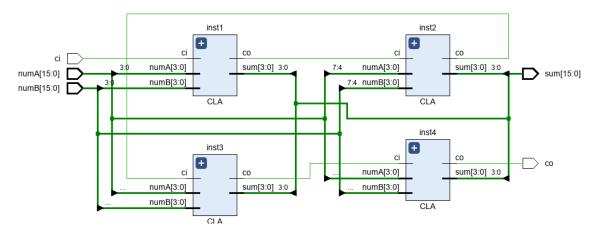
4-bit CLA



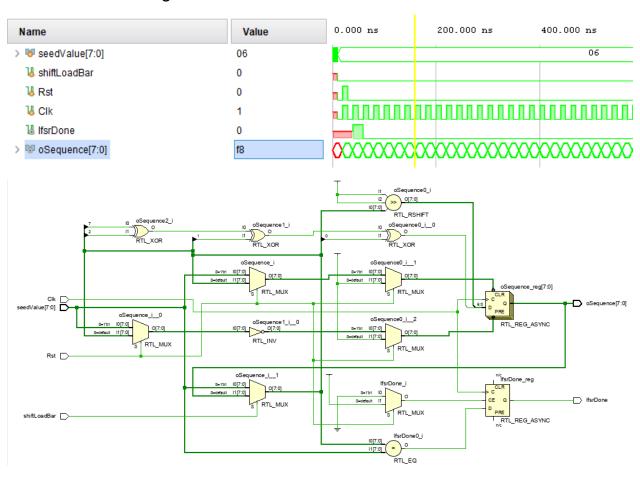
16-bit CLA



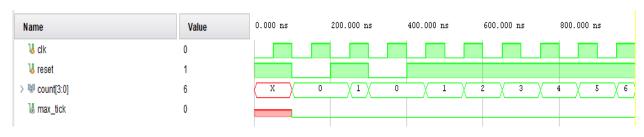
RTL_ADD

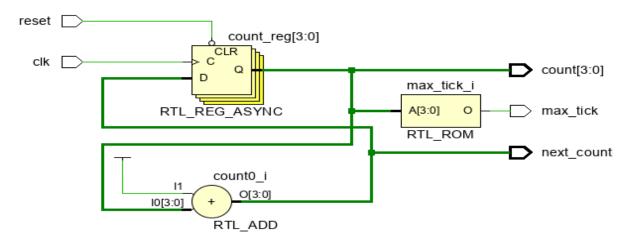


Linear feedback shift register

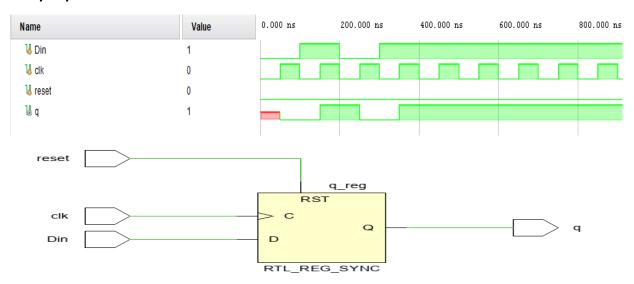


Counter





D Flipflop



T Flipflop

