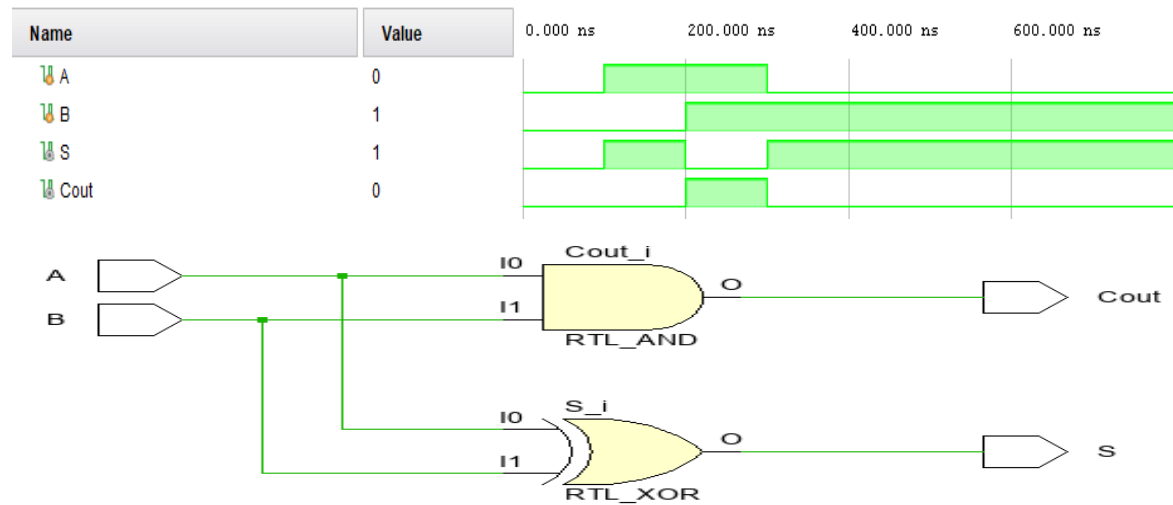
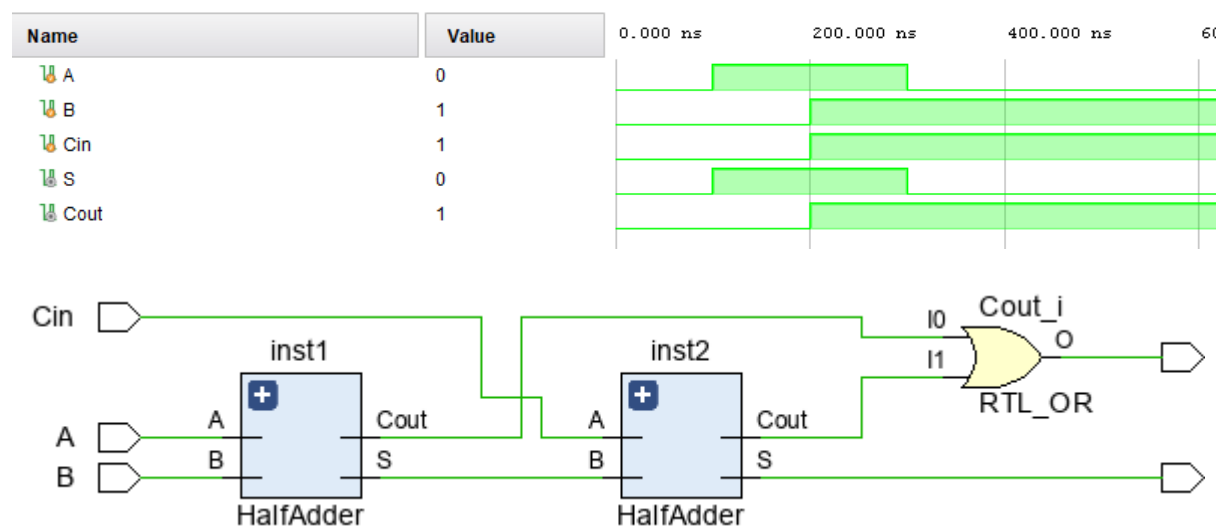


Simulation and RTL synthesis of designed modules

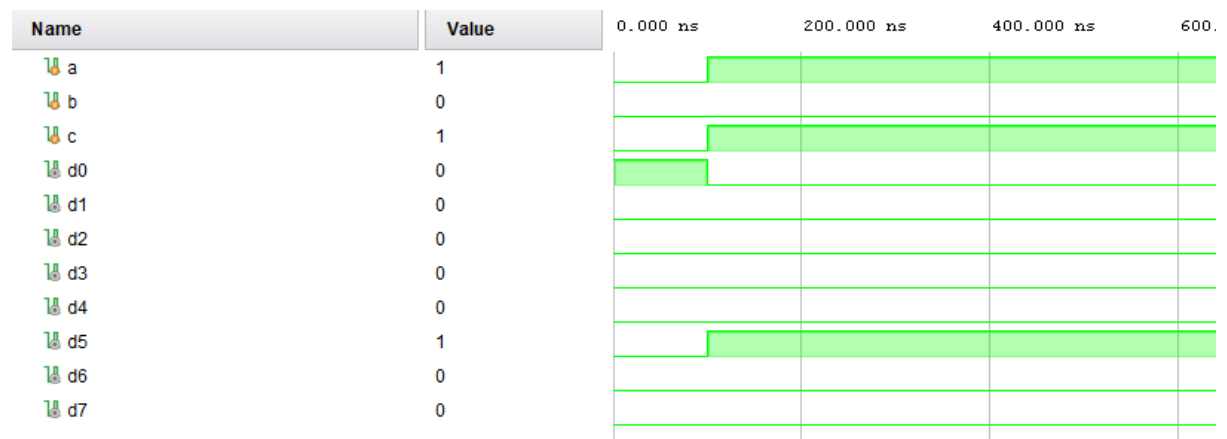
Half Adder

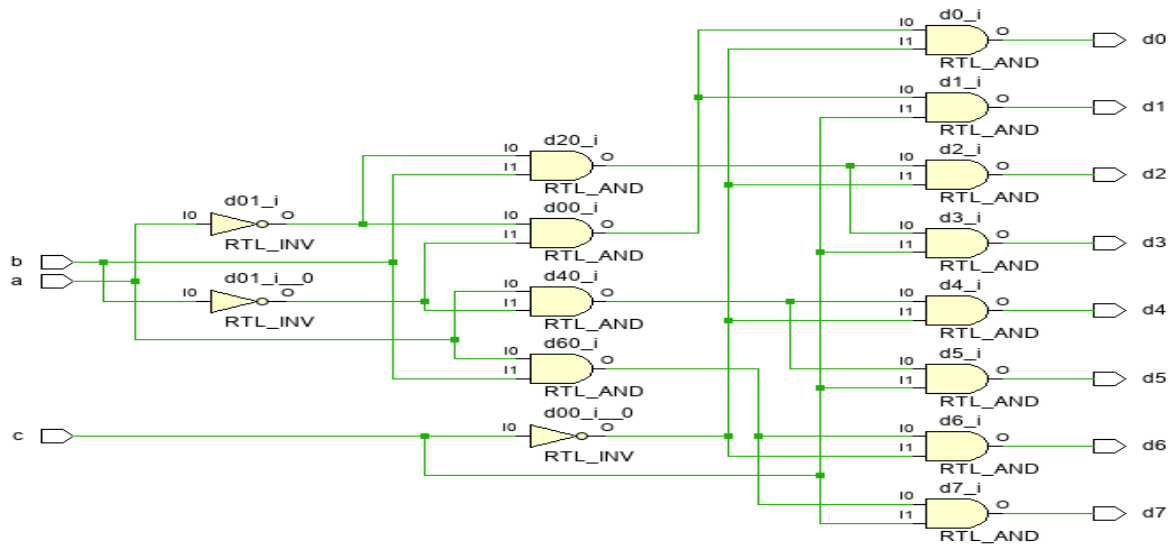


Full Adder

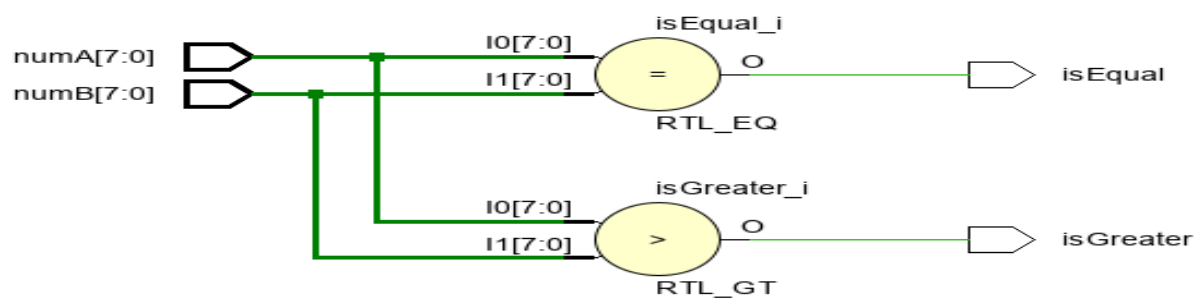
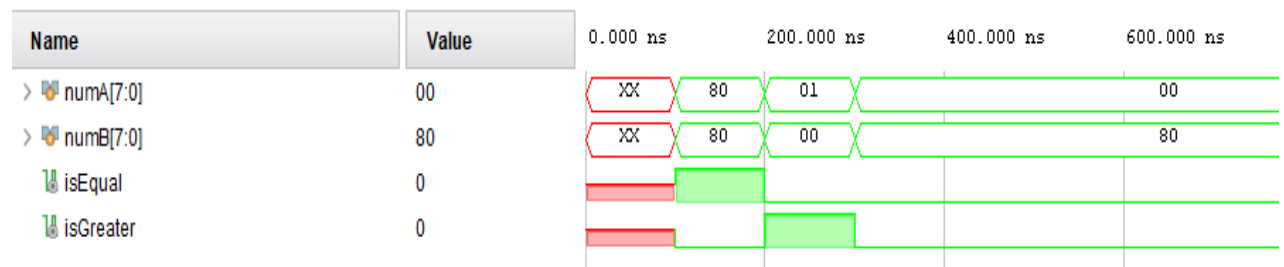


Decoder 3x8

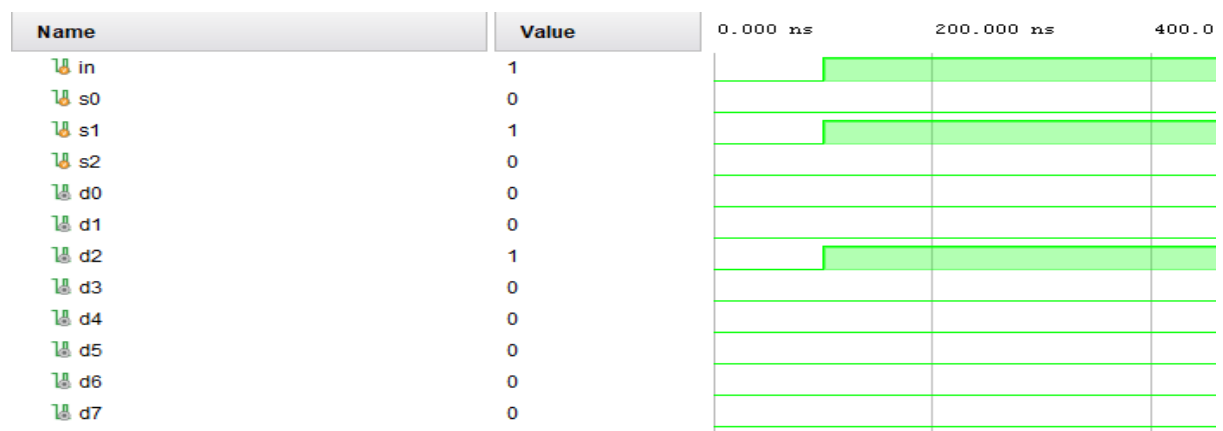


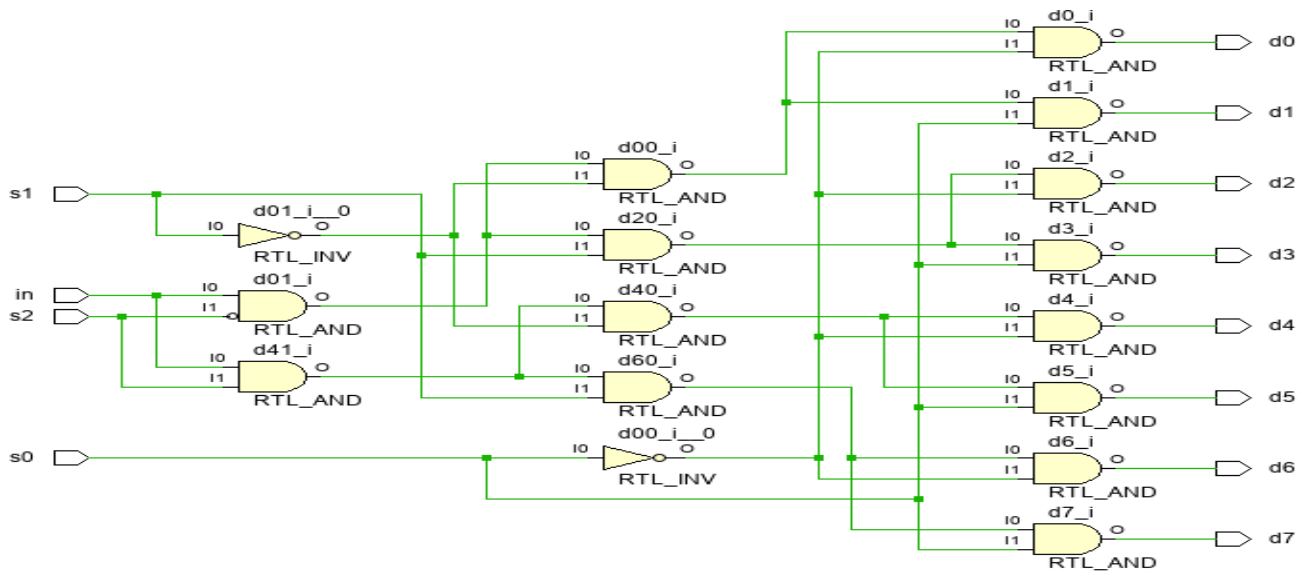


Magnitude Comparator

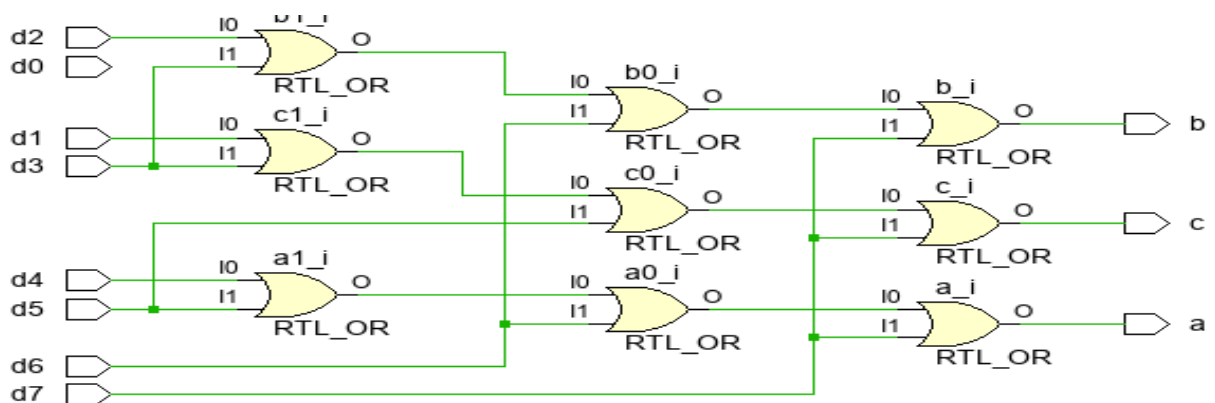
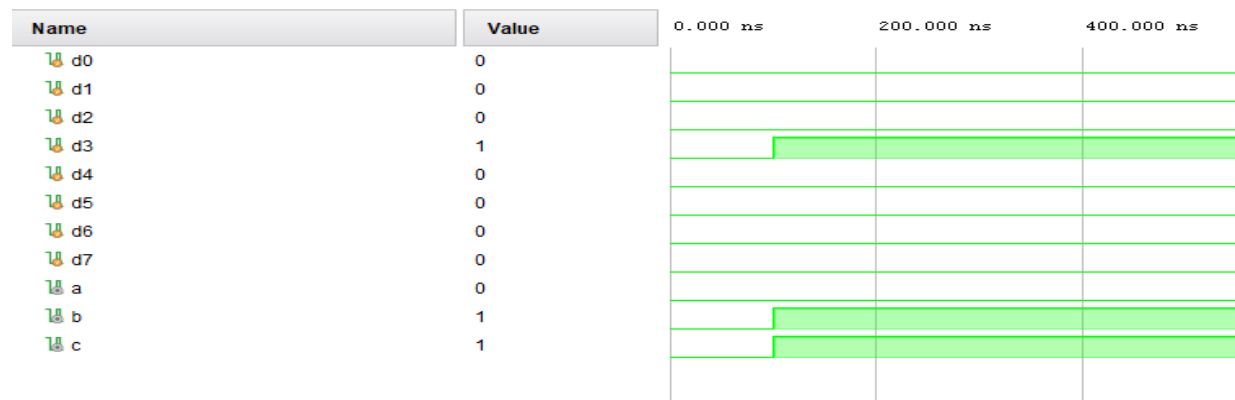


Demux 8x1

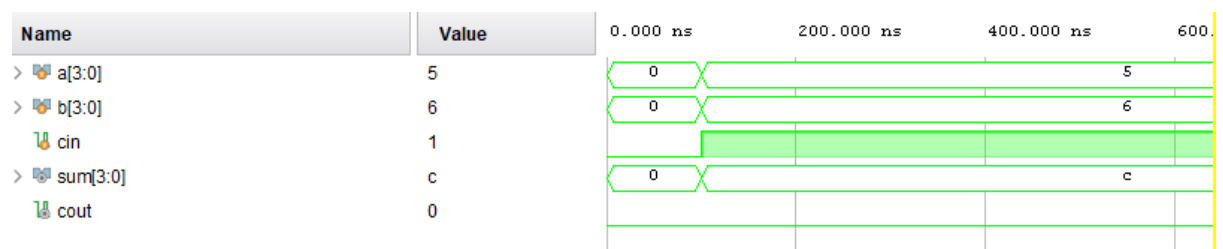


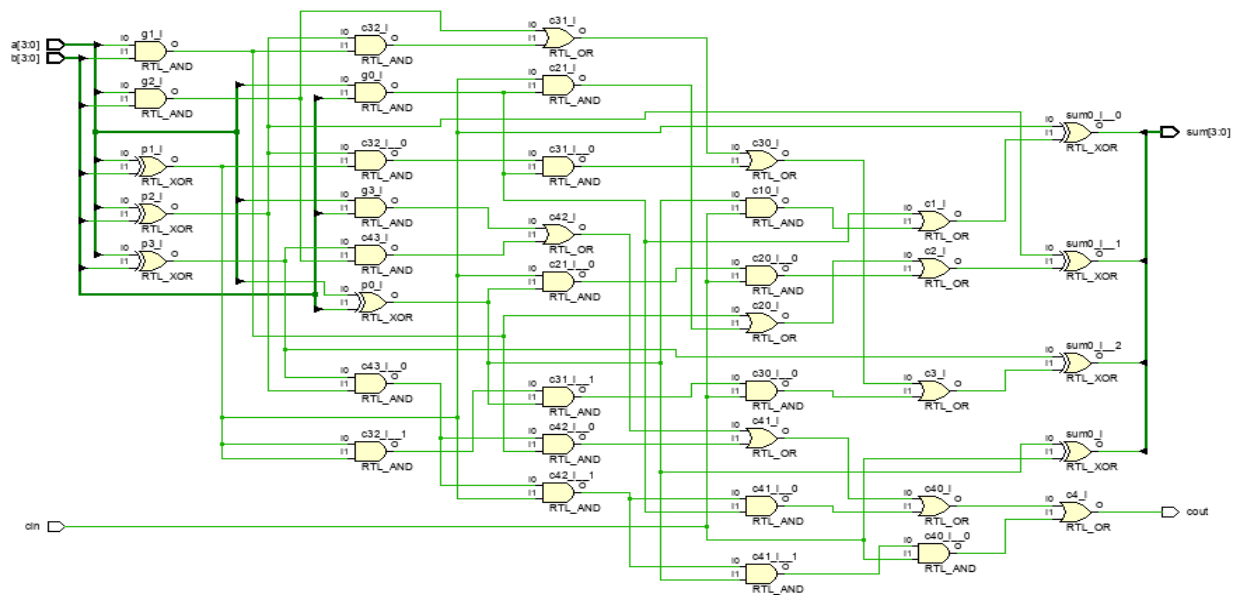


Encoder 8x3

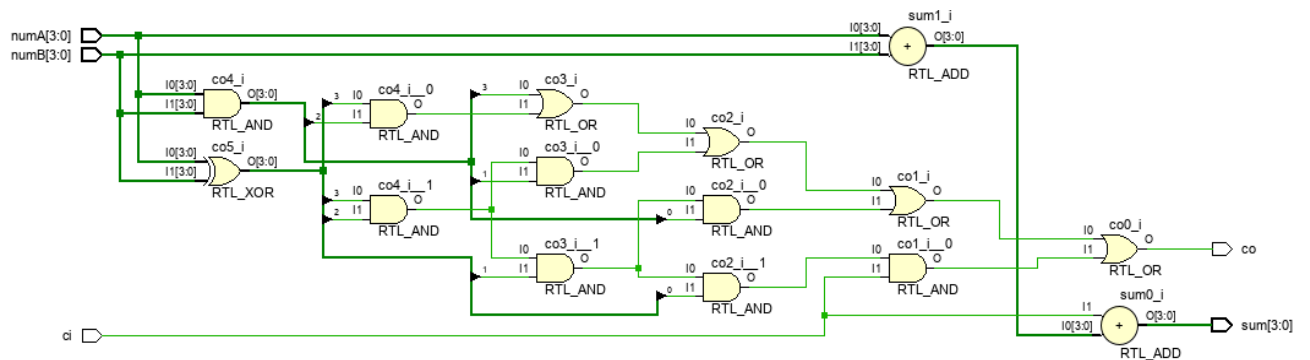
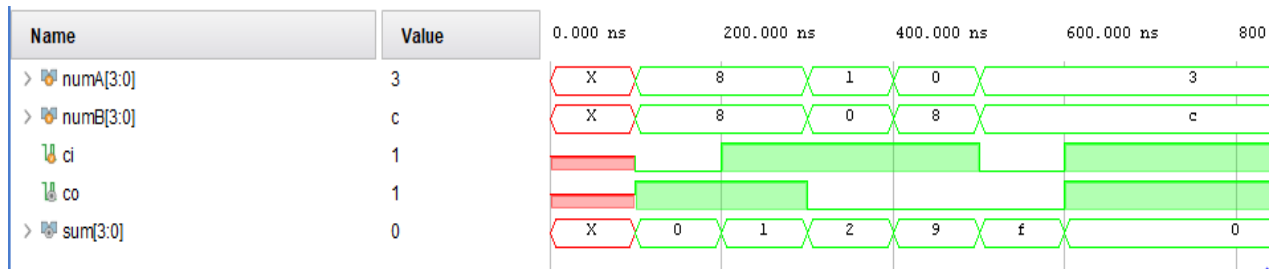


Carry Look Ahead Adder

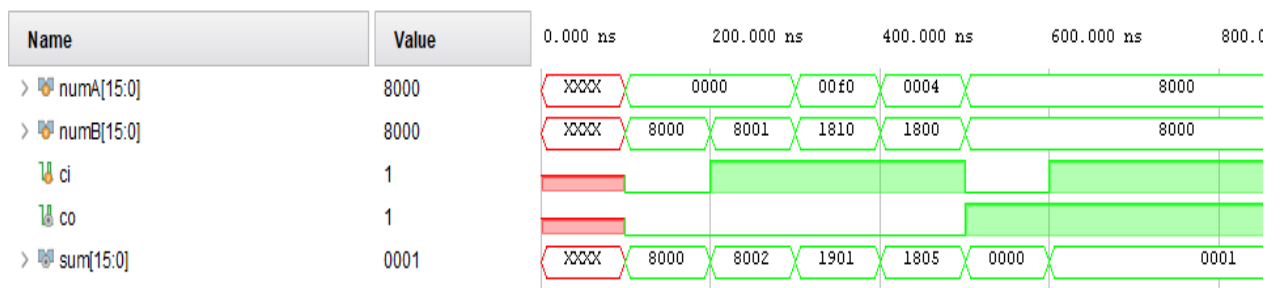


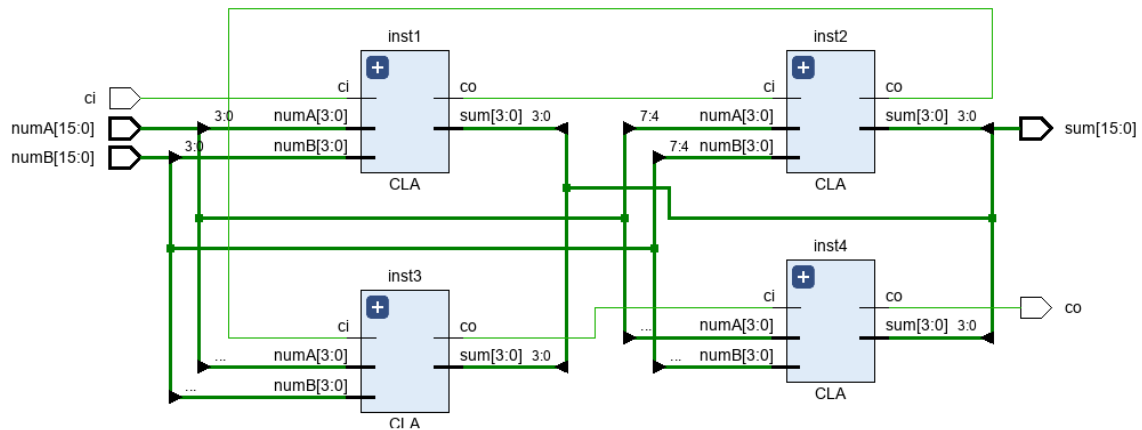


4-bit CLA

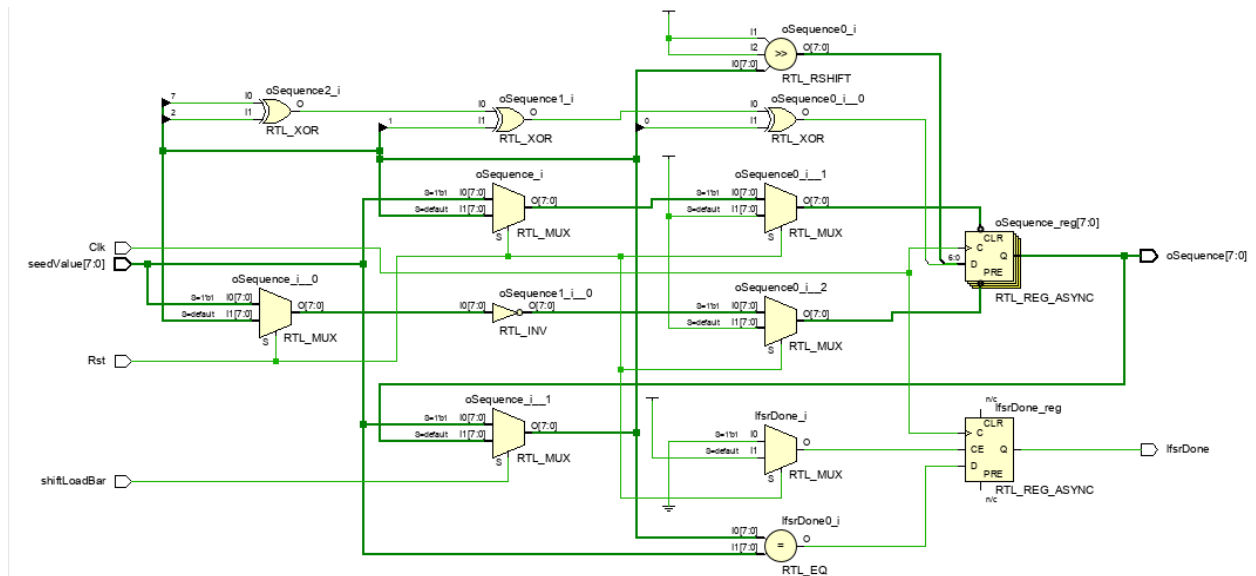
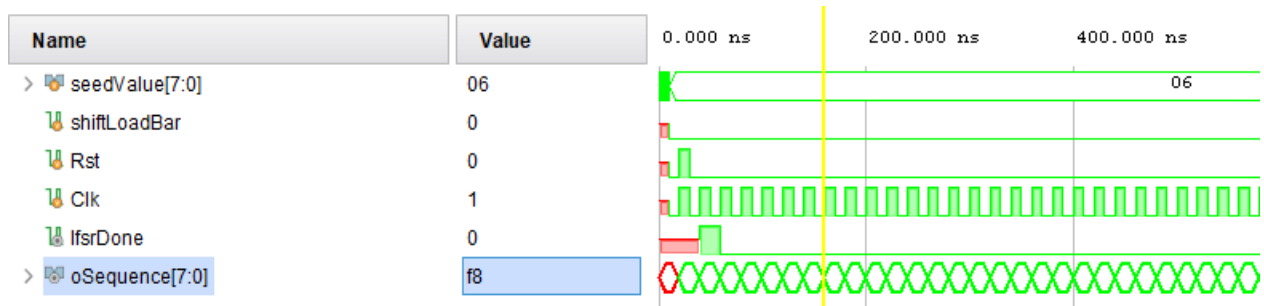


16-bit CLA

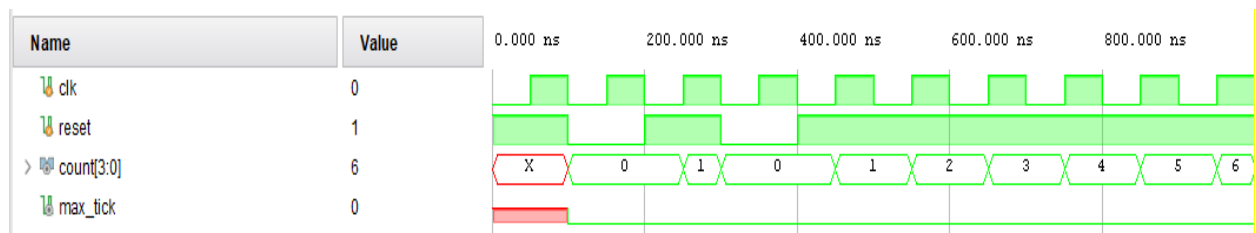


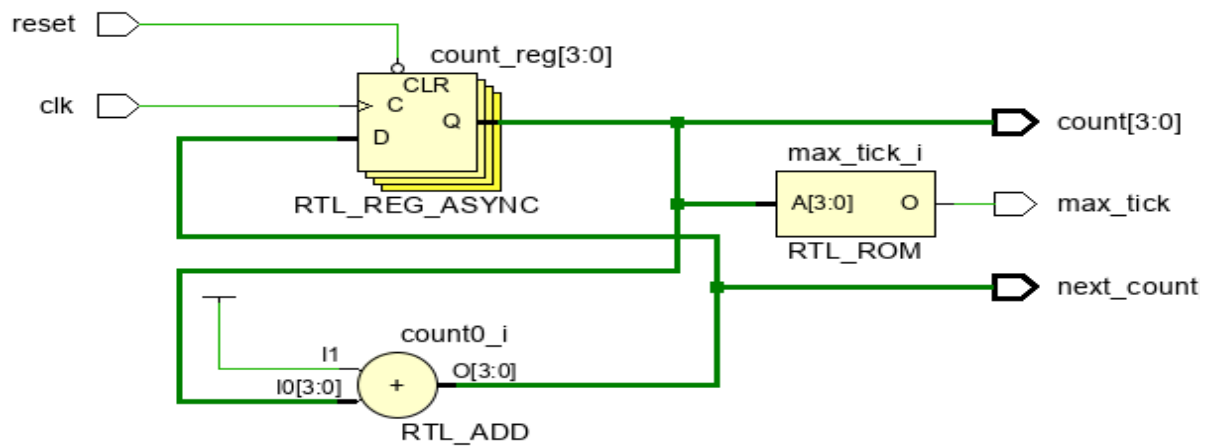


Linear feedback shift register

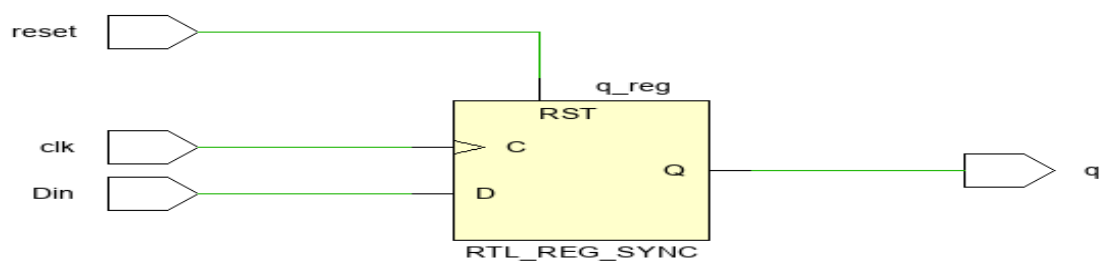
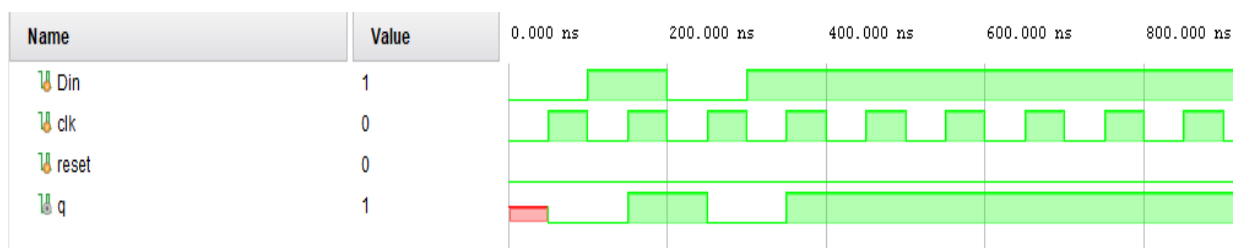


Counter





D Flipflop



T Flipflop

