NANO LETTERS

Letter

pubs.acs.org/NanoLett

Ambipolar MoS_2 Thin Flake Transistors

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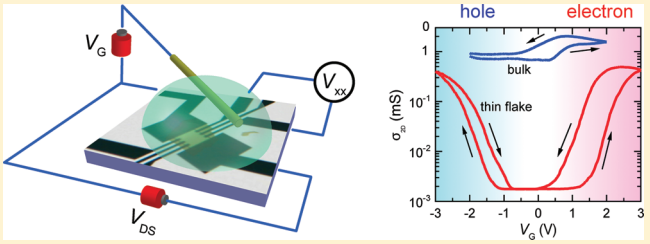
Supporting Information

ABSTRACT: Field effect transistors (FETs) made of thin flake single crystals isolated from layered materials have attracted growing interest since the success of graphene. Here, we report the fabrication of an electric double layer transistor (EDLT, a FET gated by ionic liquids) using a thin flake of MoS_2, a member of the transition metal dichalcogenides, an archetypal layered material. The EDLT of the thin flake MoS_2 unambiguously displayed ambipolar operation, in contrast to its commonly known bulk property as an *n*-type semiconductor. High-performance transistor operation characterized by a large "ON" state conductivity in the order of ~mS and a high on/off ratio >10^2 was realized for both hole and electron transport. Hall effect measurements revealed mobility of 44 and 86 $cm^2 V^{-1} s^{-1}$ for electron and hole, respectively. The hole mobility is twice the value of the electron mobility, and the density of accumulated carrier reached 1×10^{14} cm^{-2}, which is 1 order of magnitude larger than conventional FETs with solid dielectrics. The high-density carriers of both holes and electrons can create metallic transport in the MoS_2 channel. The present result is not only important for device applications with new functionalities, but the method itself would also act as a protocol to study this class of material for a broader scope of possibilities in accessing their unexplored properties.



KEYWORDS: *Transition metal chalcogenide, electric double layer, FET*

Transition metal dichalcogenides (TMDs) are characterized by layered crystal structures with two-dimensional (2D) layers composed of strong X−M−X intralayer covalent bonding (where M and X represent transition metal and chalcogen elements, respectively). On the other hand, the bonding between layers is van der Waals in nature, showing very weak interlayer interactions. This strong bonding anisotropy creates interesting 2D electronic structures. Interesting electronic phases of Mott insulators,[1,2] charge density wave,[2,3] and superconductivity[1,3] have frequently been observed in this class of materials.

Recently, semiconducting TMDs have been regarded as promising candidates for field effect transistor (FET) because MX_2 with atomically flat surface can be easily made by means of cleavage. In particular, following the introduction of the microcleavage technique used in making graphene,[4,5] an ideally flat crystal surface even without a single atomic step can be obtained which has been used as a FET channel.[5−9] TMD-FETs based on graphene techniques are important from the viewpoint of both new physics and device applications. For example, the critical temperature of superconductivity in $NbSe_2$ (a superconducting TMD) can be tuned by an external electric field.[8] For device applications, semiconducting MX_2 are attracting growing interest because they can be made into devices that have organic-like flexibility[10] in addition to a high mobility, over ~10^2 cm^2 V^{-1} s^{-1},[7,10] exceeding those of most organic FETs and approaching the mobility of devices made of graphene nanoribbons.[11] In particular, MX_2-based FETs[7] exhibits much larger on/off ratio of resistance switching properties compared with those made by graphene and its multilayers.[4,5]

Among semiconducting TMDs, 2H-type molybdenum disulfide (2H-MoS_2), as shown in Figure 1a, is a typical example. Bulk MoS_2 is an n-type semiconductor with an indirect band gap of 1.3 eV.[12] Up to now, many interesting properties have been found in bulk MoS_2. For instance, superconductivity could be induced by intercalating alkali or alkaline earth metals with the highest critical temperature up to 6.9 K ($Rb_{0.3}MoS_2$).[14,15] In addition, thin flakes of MoS_2 were obtained by microcleavage (graphene techniques) and made into solid-state FETs. Early thin flake MoS_2 FET devices with 300 nm SiO_2 dielectric showed transistor operation with a mobility and channel conductivity nearly 3 orders of magnitude lower than graphene devices.[5] However, by improving device structures with a stronger gate dielectric (30 nm HfO_2), the thin flake MoS_2 FET was revived to be an useful transistor, and an electron mobility of more than 200 cm^2 V^{-1} s^{-1} and an on/off ratio of up to a 10^8 were demonstrated.[7] Interestingly, the electronic properties of MoS_2 strongly depend on its thickness; the band structure of MoS_2 changes from a 1.3 eV indirect band gap to a 1.9 eV direct band gap when the thickness is decreased

Received: June 26, 2011
Revised: January 5, 2012
Published: January 25, 2012

   dx.doi.org/10.1021/nl2021575 | *Nano Lett.* 2012, 12, 1136−1140

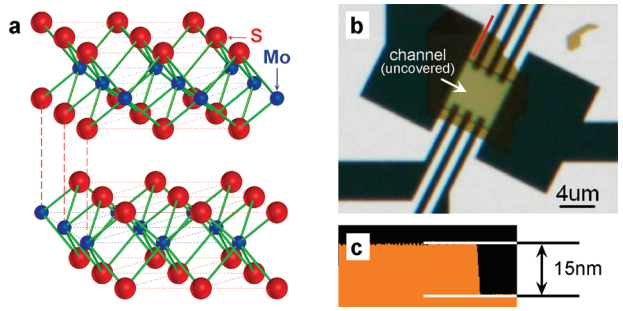


Figure 1. Thin flake MoS_2-EDLT. (a) Ball-and-stick model of a 2H-MoS_2 single crystal whose structure is composed of stacks of layers separated by Van de Waals gaps. Each layer is formed by covalent bonds (green sticks) between molybdenum (blue) and sulfur (red) atoms. (b) Optical micrograph of a MoS_2 thin flake patterned with metal electrodes and SiO_2 layer (100 nm thick) in a transmission mode. The light brown area in the middle of the flake is the exposed channel surface in contact with ionic liquids. (c) Thickness profile of the bare thin flake (15 nm thick) measured with AFM along the red line shown in (b) before device fabrication.

from bulk to monolayer.[12,13] Therefore, if both n- and p-type field effect doping is possible in MoS_2, light-emitting devices such as light-emitting transistors[16] using monolayer MoS_2 would be a promising target for the future study.

As mentioned above, changing the gate material from SiO_2 to stronger gate dielectrics (for instance, HfO_2) has been proved to be useful in improving the device performance of MoS_2 FET.[7] Using electric double layer structure is considered to improve the device properties more drastically because an electric double layer transistor (EDLT) can accumulate carriers up to 2 orders of magnitude higher than that of conventional FETs[4] (using solid state dielectrics, for instance, 300 nm SiO_2). Such a capability of EDLTs in accumulating large amount of carriers has been demonstrated by the gate-induced insulator-to-metal transition in ZnO,[17] followed by gate-induced superconductivity in $SrTiO_3$,[18] ZrNCl,[9] and $KTaO_3$.[19] In addition, the EDLT of metal dichalcogenides was recently demonstrated on a bulk crystal of SnS_2.[20] In this work, we applied the EDLT technique to a mechanically exfoliated MoS_2 thin flake and succeeded in demonstrating ambipolar operation in MoS_2 by observing hole conductivity in a MoS_2 EDLT in addition to the conventional electron transport. Hall effect measurements showed that the hole mobility is even larger than that of the electrons, suggesting that p-type operation is more favorable for FET devices. The ambipolarity in MoS_2 EDLTs provides possibilities for realizing new device functionalities, such as light-emitting devices.[16]

We fabricated MoS_2 thin flakes by cleaving a bulk single crystal (SPI Supplies). The exfoliated thin flakes were transferred to transparent sapphire substrates. In the present study, we focused on flakes with the thickness of larger than 10 nm rather than monolayer ones, since we found that those thicker flakes are very abundant while monolayer or a few layer flakes are very rare. Suitable flakes with flat surfaces were selected by examining the change of transmittance under an optical microscope (see Supporting Information, Section 1). Compared with observation in the reflection mode usually used in the identification of graphene, it is much easier to visualize the profile of flakes over a very wide range of thickness by examining from the transmission because the change in reflectance caused by an atomic step cannot be easily distinguished when the flake is thicker than ~10 nm. The thickness of our thin MoS_2 flakes was estimated from a color code created from the relationship between thickness and transmittance, which enabled the estimation of thickness up to 30 nm without AFM measurements and identification of atomically flat flakes for device fabrication.

Electrodes (Ti/Au, 3/77 nm) in a Hall bar configuration were formed on the flake by conventional microfabrication techniques of e-beam lithography, electron beam evaporation, and lift off. By this, a rectangular channel area was formed on the flake by covering the surroundings with 100 nm SiO_2. This step not only defined a channel area with a good shape but also constrained the possibility of unintentional interaction of ions from the boundary of the flake, which may appear at high gate biases. The optical image of the device is shown in Figure 1b. The thickness and surface morphology of the flake were confirmed by AFM. Although residues of e-beam resists (ZEP 520A) used during fabrication process can be found occasionally, no clear contribution to the transport property was observed (see Supporting Information, Section 2). Figure 1c shows the thickness profile of the thin flake (along the red line given in Figure 1b). The thickness was 15 nm.

Pt wire was chosen as the gate electrode. A droplet of the dehydrated ionic liquid called DEME-TFSI (*N*,*N*-diethyl-*N*-methyl-*N*-(2-methoxyethyl) ammonium bis (trifluoromethylsulfonyl) imide, one of the most widely used ionic liquid in EDLT studies[9,20−22]) was employed between the device and the tip of Pt wire by the capillary force to form the EDLT structure. All the transport measurements were performed under high vacuum (10^{-5} Torr) using a physical property measurement system (PPMS, Quantum Design, Inc.). The device was biased with a constant voltage between the source and drain electrodes, and the four-probe resistance was measured by voltage probes. To reduce the possibility of any chemical reaction between ionic liquids and MoS_2, the transport measurements were performed at 220 K, which is just above the glass transition temperature of the ionic liquid, because the rate of chemical reactivity of the ionic liquid decreases exponentially with decreasing temperature.[21]

As shown in Figure 2a, we first measured the transfer curve (I_{DS} as a function of V_G) of the thin flake MoS_2 EDLT (red curve). For comparison, a transfer curve of the bulk single crystal (blue curve) was also measured on a device fabricated on the surface of a cleaved bulk single crystal using a device configuration reported previously.[20] The surface flatness was confirmed by AFM (see Supporting Information, Section 2). For both bulk and thin flake MoS_2 EDLTs, the source−drain current I_{DS} increased as a function of applied gate voltage V_G when V_G was positive, being consistent with the behavior of *n*-type bulk crystal and electron conductivity found in thin flake solid-state devices.[5,7] No saturation was observed in I_{DS}, even when V_G is as high as 3 V, indicating high-performance transistor operation. The on/off ratio was over 200 in thin flake EDLT, indicating a highly tunable MoS_2 channel. It is worth noting that the on/off ratio is mainly limited by the "OFF" state current passing through the inside of the crystal beneath the channel surface (see Supporting Information, Section 4). In comparison with the bulk device, less contribution from the inside in the thin flake device (15 nm) is responsible for the increase in the on/off ratio by 1 order of magnitude. The higher on/off ratio in thinner devices agrees with the high-performance switching found in monolayer MoS_2 devices.[7] Despite the difference in the "OFF" state as a function of thickness, the

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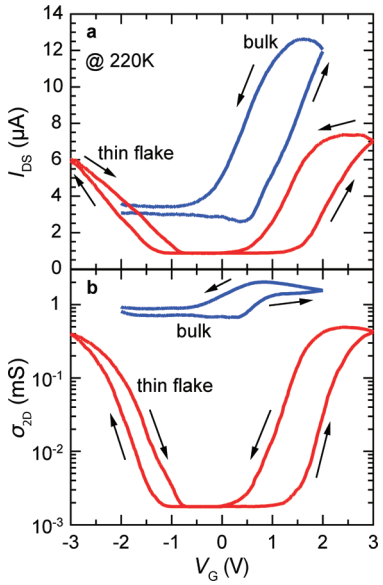

Figure 2. Transfer curve of bulk (1000 μm × 500 μm × 10 μm) and thin flake (20 μm × 20 μm × 15 nm) MoS_2 EDLTs. (a) Change in the channel current I_{DS} as a function of gate voltage V_G. V_{DS} is 0.2 V for both samples. Ambipolar transistor operation is only observed in thin flake devices, showing an increase in the channel current with an increase in the gate voltage $|V_G|$ for both hole and electron conductivities. The I_{DS} (thus on/off ratio) is limited by large contact resistance for both bulk and thin flake devices (see Supporting Information, Section 4). (b) Change of sheet conductivity σ_{2D} (4-probe) as a function of gate voltage V_G. The on/off ratio of the thin flake sample is up to >200 for both electron and hole transport. Transport with high sheet conductivity in the order of ~mS was observed in the thin flake MoS_2 EDLT for both electron and hole carriers. Large conductivity in bulk device is mainly ascribed to the small inside resistance that is parallel to the surface channel (see Supporting Information, Section 4).

"ON" state currents at high gate voltage of the two types of devices were consistent and of the same order of magnitude (~10 μA), indicating the dominating role of transport through the channel in the "ON" state.

When the gate voltage was biased toward the negative side, significant differences were found between the thin flake and bulk devices. A clear hole current was switched on at $|V_G| > 1$ V in the thin flake devices, whereas no clear increase in the channel current could be observed in the bulk devices (also see Supporting Information, Section 3). Compared with the electron transport, the transfer curve of the thin flake devices showed almost symmetric dependences on $|V_G|$ in the hole conductivity, indicating that the device property in the hole conduction channel is at least comparable to that of the electron conduction channel. As shown in Figure 2b, the channel conductance, accurately measured using a 4-probe method in the Hall bar configuration, became very high in the "ON" state. Compared with the solid-state devices,[5,7] the maximum "ON" state sheet conductivity, σ_{2D} (corresponding to a sheet resistance of $R_{sheet} \approx 3$ kΩ for hole and electron conductivity) was improved by 2−3 orders of magnitude. This is highly plausible for real device applications because higher conductivity facilitates a larger channel current and smaller heating effect.

Because the EDLT devices were operated at 220 K, relatively large hysteresis was observed, mainly due to the slow motion of the ions at low temperature. The hysteresis is related to the scanning speed of gate bias, and a fixed value of 20 mV/s was used in our study. Smaller hysteresis could be achieved with lower gate scanning speed. However, lower scanning speed will cause exposure of the device under high gate bias for longer time, which will increase the possibility of chemical reaction. Except for the hysteresis, the features in the transfer curve are consistent in the forward and backward scans of V_G.

We measured the output characteristics (I_{DS} as a function of V_{DS} at different V_G) of both electron and hole conductivity. As shown in the inset of Figure 3a, at $V_G < 0.2$ V, the I_{DS} increased

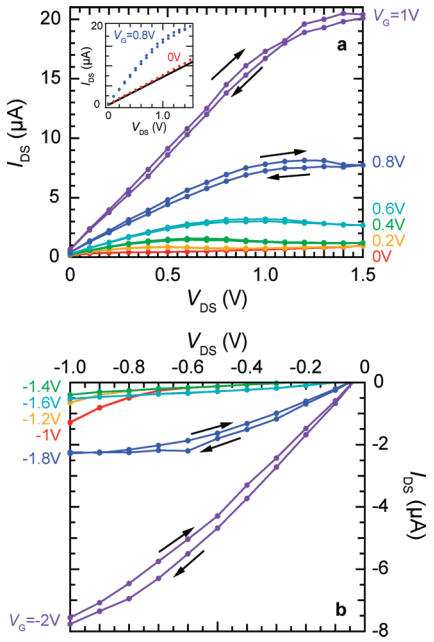

Figure 3. Output curve of the thin flake MoS_2 EDLT with both electron and hole transport. (a) Output curve in electron accumulation. The inset shows the change of I_{DS} as a function of V_{DS} in the "ON" (blue) and "OFF" (red) state. The black line shows a common linear contribution corresponding to a 140 kΩ parallel resistor originating from the transport in the inside of the single crystal beneath the surface channel. (b) Output curve in the hole conduction channel.

almost linearly with the increase in V_{DS}, indicating almost ohmic contact at the source and drain electrodes. The slope of dI_{DS}/dV_{DS} measured for -1.4 V $< V_G < 0.2$ V corresponds to a resistance of 140 kΩ, which is consistent with the "OFF" state resistance shown in the transfer curve of Figure 2a. This "OFF" state current arises mainly due to the parallel channel transporting through the inside of the thin flake and is limited by the contact resistance in series. This contribution can be fitted linearly by the black line shown in the inset of Figure 3a. The current passing through this parallel channel (with constant resistance) can be extracted from the total current passing the source and drain at higher V_G. As shown in Figure 3a, the net channel current I_{DS} exhibits clear switching properties as a function of the gate voltage V_G with saturation at high V_{DS}. Similar output properties were also observed in hole transport (see Figure 3b), showing ambipolar FET operation.

Hall effect measurement was also carried out to quantify the sheet carrier density n_{2D} and the carrier polarity (see Supporting Information, Section 5) to confirm the hole conductivity observed in the transfer curve (Figure 2a). We

dx.doi.org/10.1021/nl2021575 | Nano Lett. 2012, 12, 1136−1140

measured the Hall resistance R_{xy} under a magnetic field B and observed a change in the sign as a function of the gate voltage, as shown in Figure 4a. The change of slope directly showed

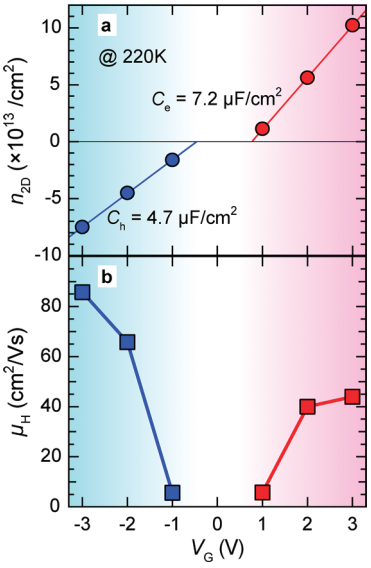

Figure 4. Hall effect measurement of carrier accumulation in the same thin flake MoS_2 EDLT as shown in Figures 1, 2, and 3. (a) Change of sheet carrier density n_{2D} as a function of gate voltage V_G at 220 K. The positive and negative n_{2D} correspond to the electron and hole densities, respectively. For both carriers, n_{2D} can be fitted linearly as a function of V_G corresponding to capacitances of 7.2 and 4.7 uF/cm^2 for electron (red) and hole (blue) accumulation, respectively. (b) Hall mobility $\mu_H = \sigma/n_{2D}e$ as a function of the gate voltage V_G. μ_H first increases and then starts to saturate after formation of the conductive channel. The maximum mobility of hole is almost twice that of electron.

positive and negative values of n_{2D} corresponding to electron and hole accumulations, respectively. The n_{2D} reached 1.0 and 0.75 × 10^{14} cm^{-2} for electrons and holes at $|V_G|$ = 3 V, respectively. For both carriers, these values are more than 1 order of magnitude higher than the maximum carrier density found in solid-state MoS_2 FETs.[5] The high carrier density for both holes and electrons are believed to be due to the large EDL capacitance of the MoS_2 channel. Using $C = dn_{2D}e/dV_G$, the EDL capacitance was calculated by a linear fit of n_{2D} as a function of V_G. The EDL capacitances were estimated to be 7.2 and 4.7 μF/cm^2 for electrons and holes, respectively. As shown in Figure 4b, both the electron and hole mobility increased with the increase in the carrier density and started to saturate after the formation of the transistor channel. The maximum Hall mobility $\mu_H = \sigma/n_{2D}e$ found in the MoS_2 EDLT device were 44 and 86 cm^2 V^{-1} s^{-1} for electron and hole transport, respectively. Comparable mobility of holes and electrons indicates this material is suitable for high-performance complementary circuits.

Shown in Figure 5 is the temperature dependence of σ_{2D} and ρ_{2D} under various V_G. At small $|V_G|$ (low n_{2D} range), σ_{2D} became smaller (sheet resistivity ρ_{2D} increased as clearly seen in Figure 5b) with decreasing temperature being typical semiconducting behavior. However, the temperature dependence is very weak, because of the contribution in transport from the inside of the thin flake is unchanged with V_G. On the other hand, at large $|V_G|$ (high n_{2D} range) clear metallic behavior was demonstrated by the temperature dependence of σ_{2D} or ρ_{2D}. In

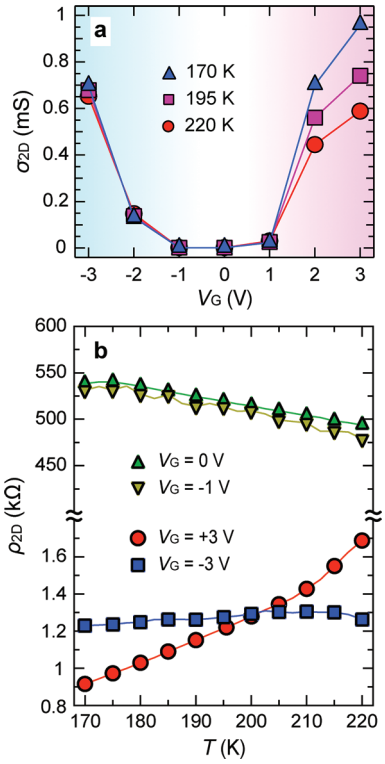

Figure 5. Temperature and gate voltage V_G dependence of the channel conductivity σ_{2D} and resistivity ρ_{2D}. (a) V_G dependence of σ_{2D} at three different temperatures. (b) Temperature dependence of ρ_{2D} at fixed gate voltages. The high and low conductivity states show contrasting temperature dependences. Under low gate bias (small $|V_G|$), ρ_{2D} shows negative slopes in (b), mainly attributed by the inside transport without the formation of a highly conductive channel. At high gate bias, (larger than around 2 V), ρ_{2D} shows positive slopes, indicating the formation of metallic channel.

the present experiment, the change from an insulating to a metallic state was more clearly demonstrated on the electron side than on the hole side, where ρ_{2D} only showed a slight decrease with decreasing temperature. For a more convincing demonstration of the metallic state in hole transport, higher carrier accumulation with larger gate biases might be required. Here, small gate voltages ($|V_G| \leq 3$ V) were chosen due to the limitation of the electrochemical window of ionic liquid (DEME-TFSI) under room temperature. The voltage range is effectively widened with lowering the temperature to 220 K, but the exact values remain unknown and can be strongly materials dependent. To avoid a chemical reaction, we limited the bias range to a conservative value. In addition, serious mechanical mismatch between organic and inorganic materials due to very different thermal expansion coefficients are also unavoidable. As a result, the sample stability gets worse rapidly as lowering temperature. This may be extremely serious when the temperature is close to 170 K, where glass transition takes place for the ionic liquids. For higher FET reproducibility, the experiment was performed in a small voltage range and under temperatures above 170 K.

In conclusion, we demonstrated that MoS_2 thin flake transistor shows ambipolar transistor operation using an EDLT device configuration. By creating a p-type conducting state, we achieved a high on/off ratio (>200) for FET operation with both electron and hole carriers, as well as high hole mobility up to 86 cm^2 V^{-1} s^{-1}), twice the value of electron

dx.doi.org/10.1021/nl2021575 | *Nano Lett.* 2012, 12, 1136–1140

mobility. The carrier density was in the order of $\sim 10^{14}$ cm^{-2}, which promoted the channel conductivity to the order of $\sim$ mS and modulated the electronic properties of MoS_2 to show an insulator-to-metal transition, for both types of carriers. The p-type transport, high-performance transistor operation, as well as gate modulation of electronic phases demonstrates that MoS_2 thin flake transistors are a promising candidate for functional applications in future electronic devices. The method established in this study could be widely applied for other layered metal chalcogenides and play an important role in exploring new physics and device applications.

■ ASSOCIATED CONTENT

Supporting Information

Detailed information is provided on MoS_2 thin flake preparation, thickness identification, and surface morphologies. Transport properties of transfer characteristics of MoS_2 thin flakes, equivalent circuit analysis, and Hall effect measurement are also included. This material is available free of charge via the Internet at http://pubs.acs.org.

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■ ACKNOWLEDGMENTS

We thank H. T. Yuan, H. Shimotani, and Y. Kasahara for fruitful discussions and R. Deacon for experimental help. This work was supported by Grant-in-Aid for Scientific Research (S) (No. 21224009) from Japan. Y.I. was supported by the Japan Society for the Promotion of Science (JSPS) through its Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program).

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