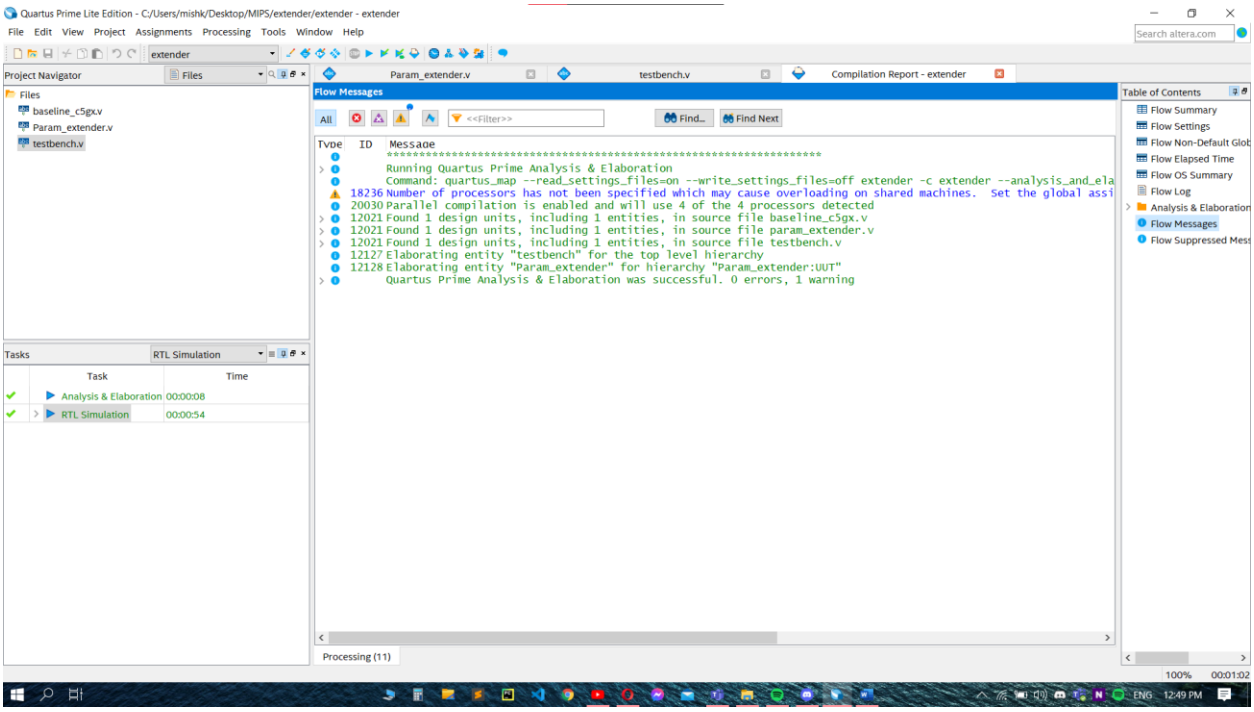
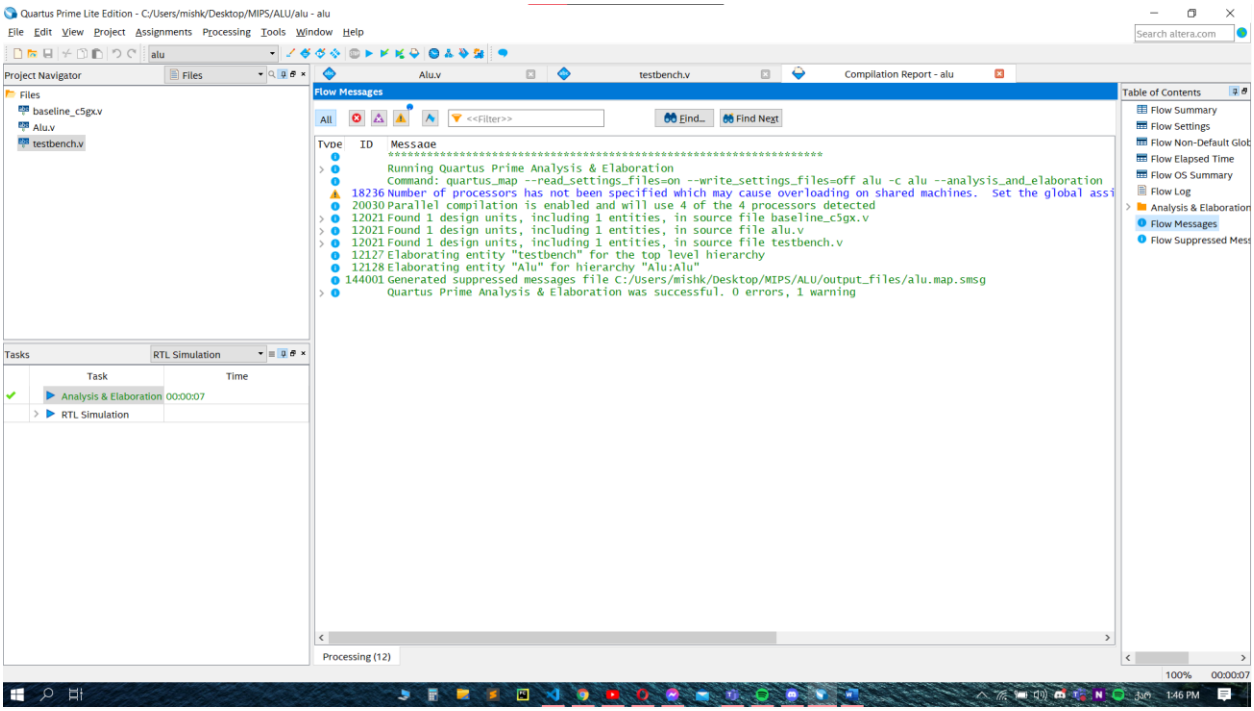
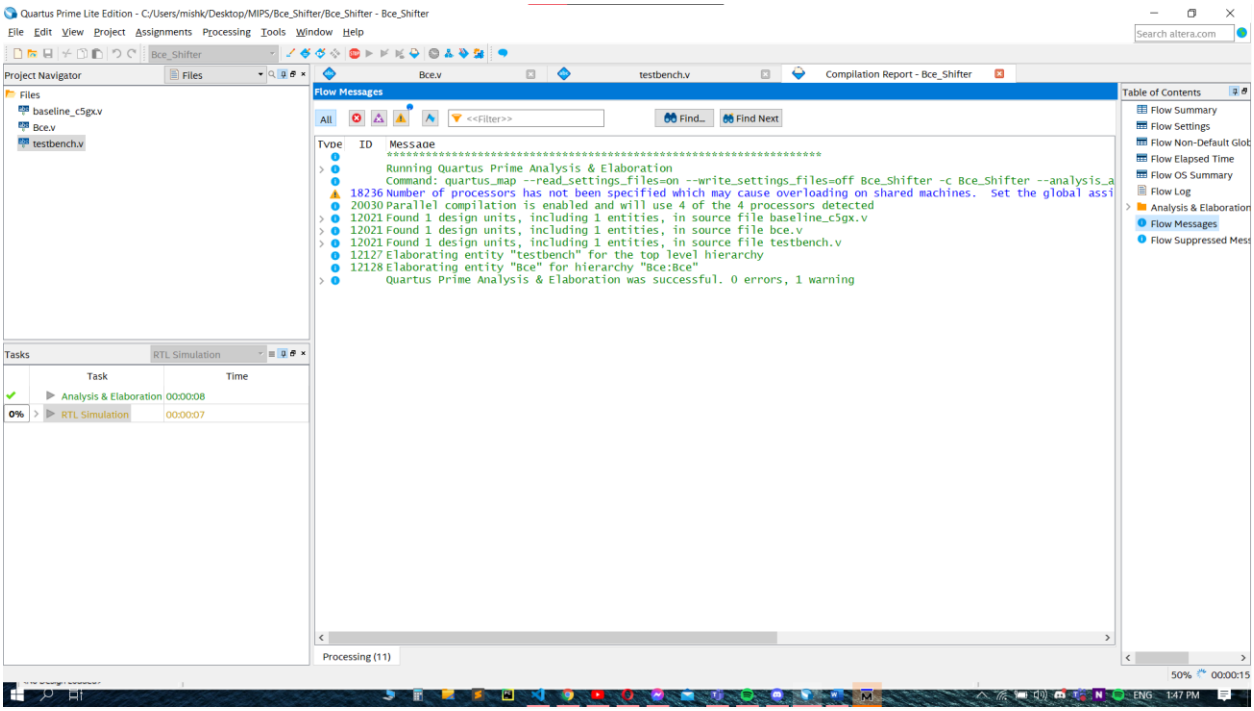
Immediate Extension Unit (IEU)



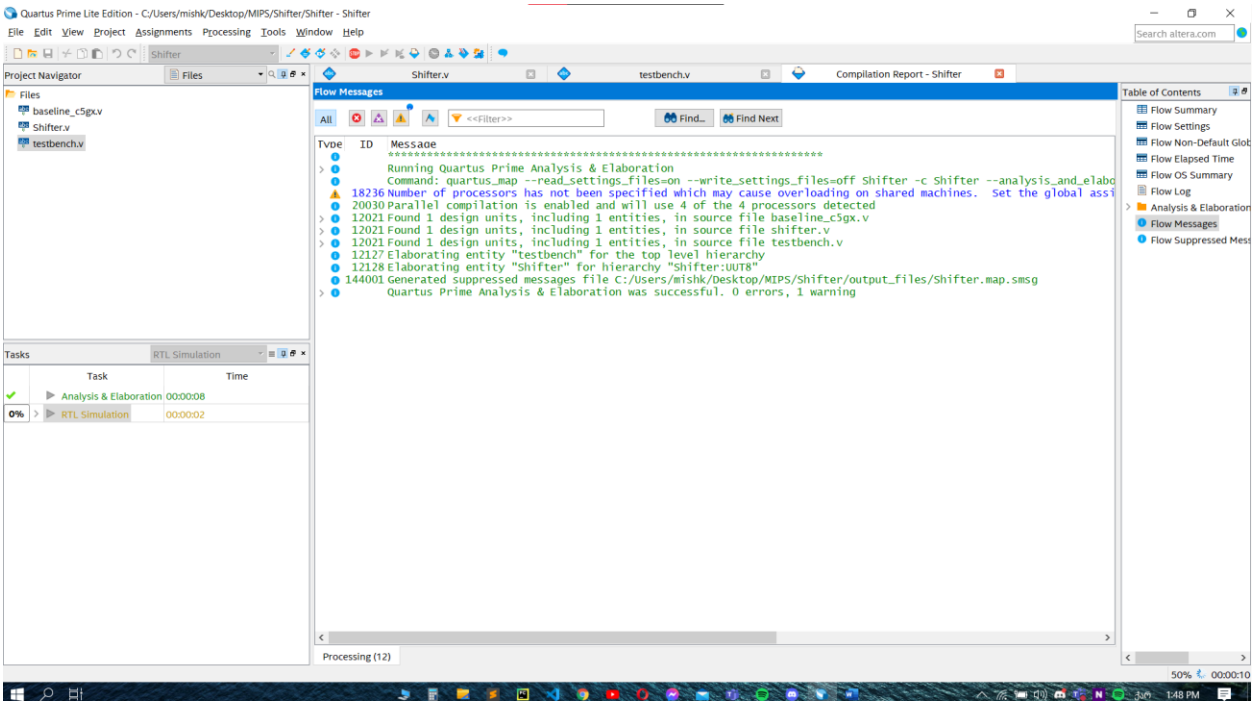
Arithmetic Logic Unit (ALU)



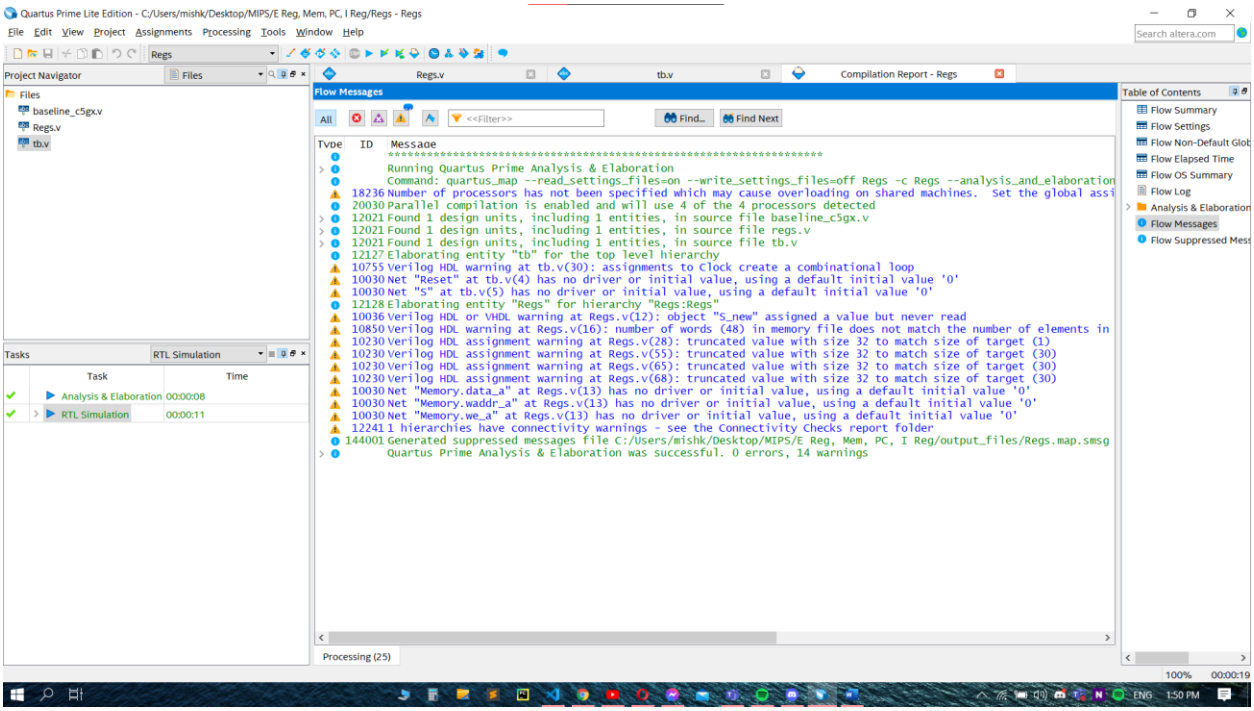
Branch Condition Evaluation Unit (BCE)



Shifter



Regs / Memory


Quartus Prime Lite Edition - C:/Users/mishk/Desktop/MIPS/E Reg, Mem, PC, I Reg/Regs - Regs
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
baseline_c5gx.v
Regs.v
tb.v
Tasks
RTL Simulation
Task
Time
Analysis & Elaboration 00:00:08
RTL Simulation 00:00:11
Regs.v
tb.v
Compilation Report - Regs
Flow Messages
Table of Contents
Flow Summary
Flow Settings
Flow Log
Flow Messages
Type ID Message
Running Quartus Prime Analysis & Elaboration
Command: quartus_map --read_settings_files=on --write_settings_files=off Regs -c Regs --analysis_and_elaboration
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assi
20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
12021 Found 1 design units, including 1 entities, in source file baseline_c5gx.v
12021 Found 1 design units, including 1 entities, in source file regs.v
12021 Found 1 design units, including 1 entities, in source file tb.v
12127 Elaborating entity "tb" for the top level hierarchy
10755 Verilog HDL warning at tb.v(30): assignments to Clock create a combinational loop
10030 Net "Reset" at tb.v(4) has no driver or initial value, using a default initial value '0'
10030 Net "S" at tb.v(5) has no driver or initial value, using a default initial value '0'
12128 Elaborating entity "Regs" for hierarchy "Regs:Regs"
10036 Verilog HDL or VHDL warning at Regs.v(12): object "S_new" assigned a value but never read
10850 Verilog HDL warning at Regs.v(16): number of words (48) in memory file does not match the number of elements in
10230 Verilog HDL assignment warning at Regs.v(28): truncated value with size 32 to match size of target (1)
10230 Verilog HDL assignment warning at Regs.v(55): truncated value with size 32 to match size of target (30)
10230 Verilog HDL assignment warning at Regs.v(65): truncated value with size 32 to match size of target (30)
10230 Verilog HDL assignment warning at Regs.v(68): truncated value with size 32 to match size of target (30)
10030 Net "Memory.data_a" at Regs.v(13) has no driver or initial value, using a default initial value '0'
10030 Net "Memory.waddr_a" at Regs.v(13) has no driver or initial value, using a default initial value '0'
10030 Net "Memory.we_a" at Regs.v(13) has no driver or initial value, using a default initial value '0'
12241 1 hierarchies have connectivity warnings - see the Connectivity Checks report folder
144001 Generated suppressed messages file C:/Users/mishk/Desktop/MIPS/E Reg, Mem, PC, I Reg/output_files/Regs.map.smsg
Quartus Prime Analysis & Elaboration was successful. 0 errors, 14 warnings
Processing (25)
100% 00:00:19
ENG 1:50 PM