USB 2.0 Controller IP

Highlights

- Low gate count to save area
- Low-power architecture
- Silicon proven, shipped in billions of units
- Supports USB 2.0 Hi-Speed, Full Speed, and Low Speed
- HS OTG, Dual Role, Host and Device functions available
- AHB interface for rapid integration
- Save software engineering effort by using drivers for OHCI-compatible Host

Target Applications

- Mobile
- Cloud computing
- Wireless
- Digital home
- Digital office
- PC peripherals
- IoT
- Automotive

Overview

The DesignWare® USB 2.0 Controllers support Hi-Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps) operation based on USB specification from the USB Implementer Forum. The DesignWare USB 2.0 IP offering consists of the Hi-Speed USB On-The-Go (HS OTG), USB 2.0 Device, and USB 2.0 EHCI Host controllers for integration into SoCs, and Verilog testbench for integration testing. These elements enable quick development of SoC designs incorporating the USB functionality. The DesignWare USB 2.0 IP is targeted for SoCs requiring the smallest area and lowest power, such as those used in IoT applications.

The DMA in the HS OTG and Device controllers, and list processor in the Host controller, reduce interrupts to the CPU/MPU and bus, reducing power consumption and leaving MIPS and bus bandwidth for other functions.

The DesignWare USB Digital Controllers offer easy integration, reliable data transfer speeds, and low overall power consumption. As the leading supplier of USB IP for more than a decade, Synopsys provides designers with efficient USB IP for cost-effective integration into SoC designs. Synopsys' expertise in developing and supporting USB IP enables us to build a low risk, high quality USB IP solution.

USB 2.0 Device Controller IP

Features

- Fully supports Hi-Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps) (USB 2.0 Speeds) specifications
- 60MHz or 30MHz input clock, and 48MHz and 12MHz input clocks
- ULPI and UTMI+ interfaces for rapid PHY integration
- Low gate counts, starting at 22k gates
- Low integration effort required for faster time-to-market
- Verilog testbench includes a USB test environment, Synopsys Verification IP, and integration tests that can be ported to the system level
- Compatible with open source and commercially available drivers to reduce software engineering effort
- Hibernation option for additional power savings

Architecture

The DesignWare USB 2.0 Device Controller IP includes:

- Packet FIFO controller which executes all USB commands in hardware
  - Tracks endpoint information in the endpoint info block
  - Processes data to and from UTMI+PHY in the parallel interface engines
  - Saves power by suspending and resuming controller operation in compliance with the USB specification
  - Offers FIFO control logic for buffering data in and out of the controller while minimizing configuration, design, and verification time
- Control and status registers for reconfiguring the controller through firmware for maximum flexibility
- Bus interface unit with Arm® AMBA® AHB™ includes a DMA controller
  - Reduces CPU interrupts
  - Enhances AHB throughput
- Hibernation Add-On option adds Wakeup and Power Control support for:
  - Reduced power consumption by stopping the PHY clock when USB is suspended or the session is not valid
  - Further power reduction with AHB clock-gating and partial power-down methods

Deliverables

- Synopsys coreConsultant tool
- Verilog RTL source code
- ASIC and FPGA synthesis example scripts
- Verilog testbench
- Verification IP
- Databooks

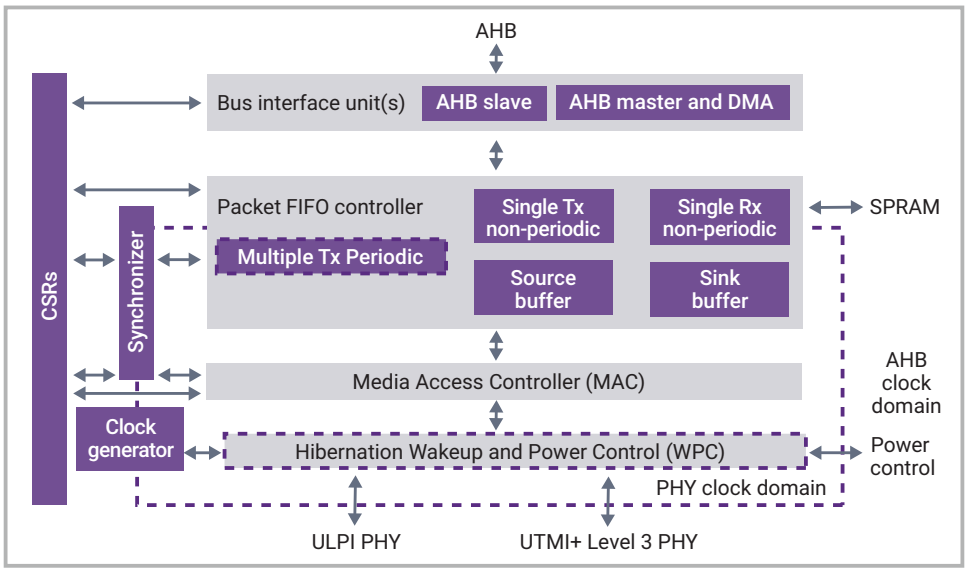

Figure 1: DesignWare USB 2.0 Device Controller IP

USB 2.0 EHCI Host Controller IP

Features

- Fully supports Hi-Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps) (USB 2.0 Speeds) specifications
- Configurable root hub supports 1 to 15 downstream ports
- 60MHz or 30MHz input clock, and 48MHz and 12MHz input clocks
- ULPI and UTMI+ interfaces for rapid PHY integration
- Low gate counts, starting at 90k gates
- Verilog testbench includes a USB test environment, Synopsys Verification IP, and integration tests that can be ported to the system level
- Compatible with the EHCI 2.0 specification, enabling designers to use drivers broadly available from open sources and supported in popular operating systems

Architecture

The DesignWare USB 2.0 EHCI Host Controller includes:

EHCI Registers

EHCI registers provide a standard EHCI register set. Operating systems with software stacks supporting EHCI read and write to these registers. EHCI is standard in most open source and commercial operating systems.

List Processor

The list processor processes the lists scheduled according to the priority set in the operational registers. This offloads the MPU/CPU and reduces the interrupts to the bus.

AHB Master

The AHB master handles read/write requests to the system memory that are initiated by the list processor while the Host is in the operational state and is processing the lists queued by the host controller. The AHB master generates the addresses for all the memory accesses. The AHB master:

- Fetches endpoint descriptors and transfer descriptors
- Reads/writes endpoint data from/to system memory
- Writes status and retires transfer descriptors

Start-of-Frame (SOF) Generator

The SOF generator generates SOF tokens every 128 µs and triggers the list processor while the Host controller is in an operational state.

Data FIFO

The data FIFO contains a 16/32/64/128/256 x 32 packet buffer to store the data returned by endpoints on IN tokens, and the data to be sent to the endpoints on OUT tokens. The FIFO is used as a buffer in case the Host controller does not receive timely access to the host bus.

Root Hub and Host PIE

The root hub propagates reset and resume to downstream ports and handles port connect/disconnect. The Host serial interface engine converts parallel to serial, serial to parallel, and NRZI encoding/ decoding, and manages the USB serial protocol.

USB 1.1 OHCI Host

The fully integrated USB 1.1 OHCI supports the OHCI standard and both Full Speed and Low Speed USB.

Deliverables

- Synopsys coreConsultant tool
- Verilog RTL source code
- ASIC and FPGA synthesis example scripts
- Verilog testbench
- Databooks

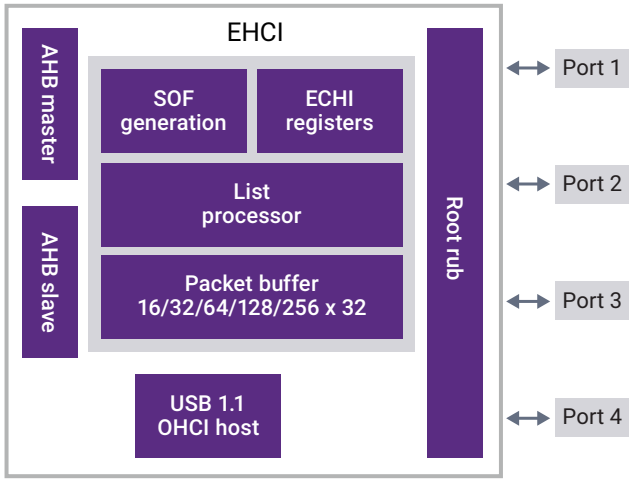

Figure 2: DesignWare USB 2.0 EHCI Host Controller IP

USB 2.0 Hi-Speed OTG Controller IP

Features

- Fully supports Hi-Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps) (USB 2.0 Speeds) specifications
- Supports Hi-Speed OTG, Dual Role Device, Hi-Speed Host, and Hi-Speed Device functions for low gate count, power sensitive products
- Flexible, post silicon configuration by software for number of endpoints or setting host or device mode
- Supports adaptable, shared FIFO memory to minimize and save RAM area
- 60MHz or 30MHz input clock, and 48MHz and 12MHz input clocks
- ULPI and UTMI+ interfaces for rapid PHY integration
- Low gate counts, starting at 22k gates
- Low integration effort required for faster time-to-market
- Verilog testbench includes a USB test environment and integration tests that can be ported to the system level
- Compatible with open source and commercially available drivers to reduce software engineering effort in the target configuration

Architecture

Protocol Layer

The protocol layer executes all USB and OTG commands in hardware.

- Tracks endpoint information in the endpoint info (EP Info) block
- Processes data to and from UTMI+ PHY in the parallel interface engines
- The OTG dynamic role changing features, Host negotiation protocol and session request protocol, may be removed during configuration to save gate count
- Manages downstream devices through the root hub
- Saves power by suspending and resuming controller operation using USB specification power states

Transaction Layer Interface

The transaction layer interface buffers data for the protocol layer. It includes:

- FIFO control logic for buffering data in and out of the controller and minimizing configuration, design, and verification time
- Control and status registers for reconfiguring the controller through firmware for maximum flexibility
- The DMA controller provides AHB Master capability, including:
  - Interfacing through descriptors for the software
  - Reducing CPU interrupts
  - Enhancing throughput on AHB

Deliverables

- Synopsys coreConsultant tool
- Verilog RTL source code
- ASIC and FPGA synthesis example scripts
- Verilog testbench
- Verification IP
- Databooks

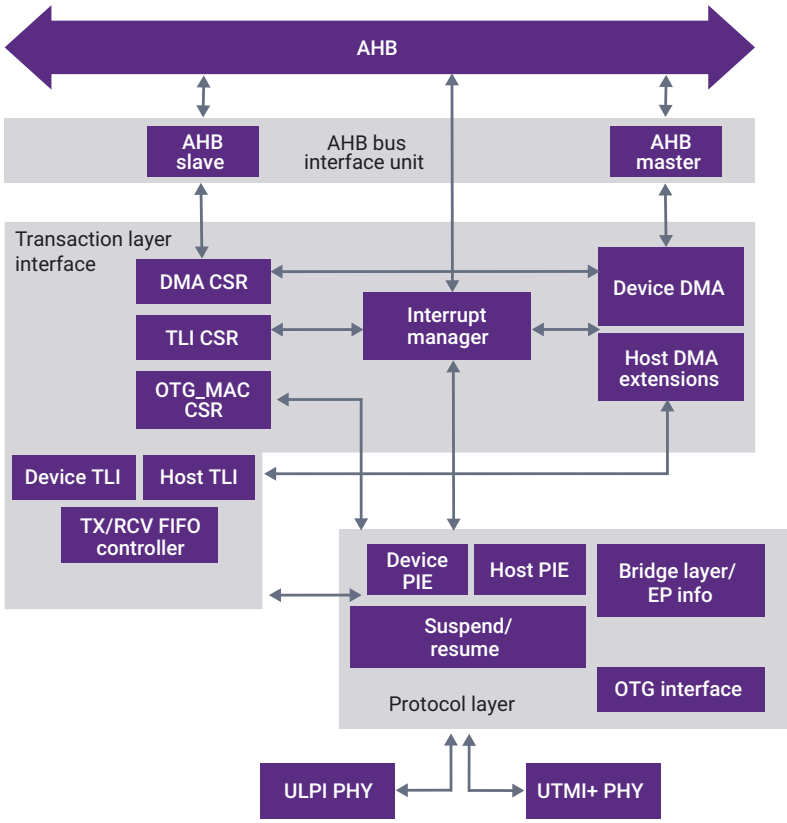

Figure 3: DesignWare USB 2.0 Hi-Speed OTG Controller IP

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtualizer Development Kit and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit synopsys.com/designware.