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Project and Deliverable Information Sheet

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Document Control Sheet

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References and Applicable Documents

*List all external documents referenced in this document*

1. <http://www.prace-project.eu>

1. <http://www.prace-ri.eu/ueabs/> - The Unified European Application Benchmark Suite
2. D7.4 Unified European Applications Benchmark Suite – Mark Bull et al. – 2013
3. <http://www.nvidia.com/object/quadro-design-and-manufacturing.html>

1. <https://userinfo.surfsara.nl/systems/cartesius/description>

1. <https://www.bsc.es/support/MareNostrum3-ug.pdf> – MareNostrum III User’s Guide Barcelona Supercomputing Center
2. http://www.idris.fr/eng/ouessant/

List of Acronyms and Abbreviations

*Below is an extensive the List of Acronyms used in previous deliverables. Please add additional ones specific to this deliverable and delete unrelated ones.*

aisbl Association International Sans But Lucratif   
 (legal form of the PRACE-RI)

BCO Benchmark Code Owner

CoE Center of Excellence

CPU Central Processing Unit

CUDA Compute Unified Device Architecture (NVIDIA)

DARPA Defense Advanced Research Projects Agency

DEISA Distributed European Infrastructure for Supercomputing Applications EU project by leading national HPC centres

DoA Description of Action (formerly known as DoW)

EC European Commission

EESI European Exascale Software Initiative

EoI Expression of Interest

ESFRI European Strategy Forum on Research Infrastructures

GB Giga (= 230 ~ 109) Bytes (= 8 bits), also GByte

Gb/s Giga (= 109) bits per second, also Gbit/s

GB/s Giga (= 109) Bytes (= 8 bits) per second, also GByte/s

GÉANT Collaboration between National Research and Education Networks to build a multi-gigabit pan-European network. The current EC-funded project as of 2015 is GN4.

GFlop/s Giga (= 109) Floating point operations (usually in 64-bit, i.e. DP) per second, also GF/s

GHz Giga (= 109) Hertz, frequency =109 periods or clock cycles per second

GPU Graphic Processing Unit

HET High Performance Computing in Europe Taskforce. Taskforce by representatives from European HPC community to shape the European HPC Research Infrastructure. Produced the scientific case and valuable groundwork for the PRACE project.

HMM Hidden Markov Model

HPC High Performance Computing; Computing at a high performance level at any given time; often used synonym with Supercomputing

HPL High Performance LINPACK

ISC International Supercomputing Conference; European equivalent to the US based SCxx conference. Held annually in Germany.

KB Kilo (= 210 ~103) Bytes (= 8 bits), also KByte

LINPACK Software library for Linear Algebra

MB Management Board (highest decision making body of the project)

MB Mega (= 220 ~ 106) Bytes (= 8 bits), also MByte

MB/s Mega (= 106) Bytes (= 8 bits) per second, also MByte/s

MFlop/s Mega (= 106) Floating point operations (usually in 64-bit, i.e. DP) per second, also MF/s

MooC Massively open online Course

MoU Memorandum of Understanding.

MPI Message Passing Interface

NDA Non-Disclosure Agreement. Typically signed between vendors and customers working together on products prior to their general availability or announcement.

PA Preparatory Access (to PRACE resources)

PATC PRACE Advanced Training Centres

PRACE Partnership for Advanced Computing in Europe; Project Acronym

PRACE 2 The upcoming next phase of the PRACE Research Infrastructure following the initial five year period.

PRIDE Project Information and Dissemination Event

RI Research Infrastructure

TB Technical Board (group of Work Package leaders)

TB Tera (= 240 ~ 1012) Bytes (= 8 bits), also TByte

TCO Total Cost of Ownership. Includes recurring costs (e.g. personnel, power, cooling, maintenance) in addition to the purchase cost.

TDP Thermal Design Power

TFlop/s Tera (= 1012) Floating-point operations (usually in 64-bit, i.e. DP) per second, also TF/s

Tier-0 Denotes the apex of a conceptual pyramid of HPC systems. In this context the Supercomputing Research Infrastructure would host the Tier-0 systems; national or topical HPC centres would constitute Tier-1

UNICORE Uniform Interface to Computing Resources. Grid software for seamless access to distributed resources.

List of Project Partner Acronyms

BADW-LRZ Leibniz-Rechenzentrum der Bayerischen Akademie der Wissenschaften, Germany (3rd Party to GCS)

BILKENT Bilkent University, Turkey (3rd Party to UYBHM)

BSC Barcelona Supercomputing Center - Centro Nacional de Supercomputacion, Spain

CaSToRC Computation-based Science and Technology Research Center, Cyprus

CCSAS Computing Centre of the Slovak Academy of Sciences, Slovakia

CEA Commissariat à l’Energie Atomique et aux Energies Alternatives, France (3 rd Party to GENCI)

CESGA Fundacion Publica Gallega Centro Tecnológico de Supercomputación de Galicia, Spain, (3rd Party to BSC)

CINECA CINECA Consorzio Interuniversitario, Italy

CINES Centre Informatique National de l’Enseignement Supérieur, France (3 rd Party to GENCI)

CNRS Centre National de la Recherche Scientifique, France (3 rd Party to GENCI)

CSC CSC Scientific Computing Ltd., Finland

CSIC Spanish Council for Scientific Research (3rd Party to BSC)

CYFRONET Academic Computing Centre CYFRONET AGH, Poland (3rd party to PNSC)

EPCC EPCC at The University of Edinburgh, UK

ETHZurich (CSCS) Eidgenössische Technische Hochschule Zürich – CSCS, Switzerland

FIS FACULTY OF INFORMATION STUDIES, Slovenia (3rd Party to ULFME)

GCS Gauss Centre for Supercomputing e.V.

GENCI Grand Equipement National de Calcul Intensiv, France

GRNET Greek Research and Technology Network, Greece

INRIA Institut National de Recherche en Informatique et Automatique, France (3 rd Party to GENCI)

IST Instituto Superior Técnico, Portugal (3rd Party to UC-LCA)

IUCC INTER UNIVERSITY COMPUTATION CENTRE, Israel

JKU Institut fuer Graphische und Parallele Datenverarbeitung der Johannes Kepler Universitaet Linz, Austria

JUELICH Forschungszentrum Juelich GmbH, Germany

KTH Royal Institute of Technology, Sweden (3 rd Party to SNIC)

LiU Linkoping University, Sweden (3 rd Party to SNIC)

NCSA NATIONAL CENTRE FOR SUPERCOMPUTING APPLICATIONS, Bulgaria

NIIF National Information Infrastructure Development Institute, Hungary

NTNU The Norwegian University of Science and Technology, Norway (3rd Party to SIGMA)

NUI-Galway National University of Ireland Galway, Ireland

PRACE Partnership for Advanced Computing in Europe aisbl, Belgium

PSNC Poznan Supercomputing and Networking Center, Poland

RISCSW RISC Software GmbH

RZG Max Planck Gesellschaft zur Förderung der Wissenschaften e.V., Germany (3 rd Party to GCS)

SIGMA2 UNINETT Sigma2 AS, Norway

SNIC Swedish National Infrastructure for Computing (within the Swedish Science Council), Sweden

STFC Science and Technology Facilities Council, UK (3rd Party to EPSRC)

SURFsara Dutch national high-performance computing and e-Science support center, part of the SURF cooperative, Netherlands

UC-LCA Universidade de Coimbra, Labotatório de Computação Avançada, Portugal

UCPH Københavns Universitet, Denmark

UHEM Istanbul Technical University, Ayazaga Campus, Turkey

UiO University of Oslo, Norway (3rd Party to SIGMA)

ULFME UNIVERZA V LJUBLJANI, Slovenia

UmU Umea University, Sweden (3 rd Party to SNIC)

UnivEvora Universidade de Évora, Portugal (3rd Party to UC-LCA)

UPC Universitat Politècnica de Catalunya, Spain (3rd Party to BSC)

UPM/CeSViMa Madrid Supercomputing and Visualization Center, Spain (3rd Party to BSC)

USTUTT-HLRS Universitaet Stuttgart – HLRS, Germany (3rd Party to GCS)

VSB-TUO VYSOKA SKOLA BANSKA - TECHNICKA UNIVERZITA OSTRAVA, Czech Republic

WCNS Politechnika Wroclawska, Poland (3rd party to PNSC)

*Depending on the size (number of pages) of the front matter an empty page has to be inserted to force the Executive Summary (Page 1) to the top of a sheet when printed. Simply specifying Section Change to Odd or Even seems not to work reliably.*

Executive Summary

This document describes an accelerator benchmark suite, a set of 11 codes that includes 1 synthetic benchmarks and 10 commonly used applications. The key focus of this task has been exploiting accelerators or co-processors to improve the performance of real applications. It aims at providing a set of scalable, currently relevant and publically available codes and datasets.

This work has been undertaken be Task7.2B "Accelerator Benchmarks" in the PRACE Forth Implementation Phase (PRACE-4IP) project.

Most of the selected application are a subset of the Unified European Applications Benchmark Suite (UEABS) [2][3]. One application and a synthetic benchmark have been added.

As a result, selected codes are: ALYA, Code\_Saturne, CP2K, GROMACS, GPAW, NAMD, PFARM, QCD, Quantum Espresso, SHOC and SPECFEM3D.

For each code either two or more test case datasets have been selected. These are described in this document, along with a brief introduction to the application codes themselves. For each code, some sample results are presented, from first run on leading edge systems and prototypes.

## Introduction

The work produced within this task is an extension of the UEABS for accelerators. This document will cover each code, presenting the code as well as the test cases defined for the benchmarks and the first results that have been recorded on various accelerator systems.

As the UEABS, this suite aims to present results for many scientific fields that can use HPC accelerated resources. Hence, it will help the European scientific communities to decide in terms of infrastructures they could buy in a near future. We focus on Intel Xeon Phi coprocessors and NVidia GPU cards for benchmarking as they are the two most important accelerated resources available now.

Section 2 will present both type accelerator systems Xeon Phi and GPU card along with architecture examples. Section \ref{applications} gives a description of each of the selected applications, together with the test case datasets, and presents some sample results. Section \ref{conclusion} outlines further work on, and using, the suite.

## Targeted architectures

This suite is targeting accelerator cards, more specifically the Intel Xeon Phi and NVIDIA GPU architecture. This section will quickly describe them and will present the four machine, the benchmarks ran on.

### Co-processor description

Scientific computing using co-processors has gained popularity in recent years. First the utility of GPUs has been demonstrated and evaluated in several application domains [4]. As a response to NVIDA supremacy on this field, Intel designed Xeon Phi cards.

Architectures and programming models of co-processors may differ from CPUs and vary among different co-processor types. The main challenges are the high-level parallelism ability required from software and the fact that code may have to be offloaded to the accelerator card.

The following table enlightens this fact:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Intel Xeon Phi | | NVIDIA GPU | |
|  | 5110P (KNC) | 7250 (KNL) | K40m | P100 |
| public availability date | Nov-12 | Jun-16 | Jun-13 | May-16 |
| theoretical peak perf | 1,011 GF/s | 3,046 GF/s | 1,430 GF/s | 5,300 GF/s |
| offload required | yes | no | yes | yes |
| max number of thread/cuda cores | 240 | 272 | 2880 | 3584 |

### Systems description

The benchmark suite has been officially granted access to 4 different machines hosted by PRACE partners. Most results presented in this paper were obtained on these machines but some of the simulation has run on similar ones. This section will cover specifications of the sub mentioned 4 official systems while the few exotic ones will be presented along with concerned results.

As it can be noticed on the previous section, leading edge architectures have been available quite recently and some code couldn't run on it yet. Results will be completed in a near future and will be delivered with an update of the benchmark suite. Still, presented performances are a good indicator about potential efficiency of codes on both Xeon Phi and NVIDIA GPU platforms.

#### K40 cluster

The SURFsara institute in Nederland granted access to Cartesius which has a GPU island (installed May 2014) with following specifications [5]:

* 66 Bullx B515 GPU accelerated nodes
  + 2x 8-core 2.5 GHz Intel Xeon E5-2450 v2 (Ivy Bridge) CPUs/node
  + 2x NVIDIA Tesla K40m GPGPUs/node
  + 96 GB/node
* Total theoretical peak performance (Ivy Bridge + K40m) 1,056 cores + 132 GPUs: 210 TF/s

The interconnect has a fully non-blocking fat-tree topology. Every node has two ConnectX-3 InfiniBand adapters: one per GPGPU.

#### Xeon Phi 5110P cluster

The Barcelona Supercomputing Center (BSC) in Spain granted access to MareNostrum III which features KNC nodes (upgrade June 2013). Here's the description of this partition [6]:

* 42 hybrid nodes contain:
  + 8x 8G DDR3–1600 DIMMs (4GB/core), total: 64GB/node
* 2x Xeon Phi 5110P accelerators
* Interconnection networks:
  + Infiniband Mellanox FDR10: High bandwidth network used by parallel applications communications (MPI)
  + Gigabit Ethernet: 10GbitEthernet network used by the GPFS Filesystem.

#### P100 cluster

GENCI granted access to the Ouessant prototype at IDRIS in France (installed September 2016). It is composed of 12 IBM Minsky compute nodes with each containing [7]:

* Compute nodes
  + POWER8+ sockets, 10 cores, 8 threads per core (or 160 threads par node)
  + 128 GB of DDR4 memory (bandwidth > 9 GB/s per core)
  + 4 Nvidia new generation Pascal P100 GPUs, 16 GB of HBM2 memory
* Interconnect
  + 4 NVLink interconnects (40GB/s of bi-directional bandwidth per interconnect); each GPU card is connected to a CPU with 2 NVLink interconnects and another GPU with 2 interconnects remaining
  + A Mellanox EDR IB CAPI interconnexion network (1 interconnect per node)

#### Xeon Phi 7250 cluster

GENCI also granted access to the Frioul prototype at CINES in France (installed December 2016). It is composed of 48 Intel KNL compute nodes:

* Peak performance of 146 TF/s
* Interconnect: Infiniband IB 4x FDR
* File system: Lustre, more than 5 Po usable and a maximum bandwidth of 105 Go/s

### Section Title Level 1 (Formatting of Lists)

<Text begins here.>

If possible use only Bullet lists of one or two levels and numbered lists of one level. If you have to deviate from the proposed ‘standard’ make sure you use the same bullets throughout the document.

#### Section Title Level 2 (Bullet Lists)

<Text begins here>

* This is line one of the bullet list. It can span more than one line. Please note that block formatting also applies.
* This is line two of the bullet list. It can span more than one line. Please note that block formatting also applies.
* This is sub-bullet line 1. It can span more than one line. Please note that block formatting also applies.
* This is sub-bullet line 2.
* This is line three of the bullet list. It can span more than one line. Please note that block formatting also applies.

The default formatting of bullet list paragraphs is **0pt** **before** and **3pt** **after** each paragraph.

#### Section Title Level 2 (Numbered Lists)

<Text begins here>

1. This is line one of the bullet list. It can span more than one line. Please note that block formatting also applies.
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     2. This is sub-bullet line 2.
3. This is line three of the bullet list. It can span more than one line. Please note that block formatting also applies.

The default formatting of bullet list paragraphs is **0pt** **before** and **3pt** **after** each paragraph.

### Section Title – Level 1 (Headings)

<Text begins here>.

Three levels of headings are defined and automatically included in the Table of Contents (ToC). All (except the ‘Executive Summary’) are numbered and left justified. The Executive Summary is centred.

*Level 1* is formatted as **Arial, bold face, 14pt** with 18pt before and 18pt after and numbered 1, 2, ….

*Level 2* is formatted as **Arial, bold face, 12pt** with 18pt before and 12pt after and numbered 1.1, 1.2, …, 2.1, 2.2, ….

*Level 3* is formatted as *Arial, italics, 12pt*with 12pt before and 12pt after and numbered 1.1.1, 1.1.2, …, 2.1.1, 2.1.2, ….

It might be appropriate to start a new section on a new page to better structure the document, especially, when the new section starts at the very bottom of the page. A manual page break might be inserted at the final stage of the production. This is the case in this template to start Section 2: Targeted on page 1.

## Section Title (Figures)

<Text begins here.>

This section shows examples how figures can be inserted into the text and how it is insured that the figure subscript is properly included into the List of Figures.

### Section Title – Level 1 (Simple Graphic In Line)

<Text begins here>

PRACE_Logo_pos_CMYKeps

Figure 1: The PRACE logo inserted with text

Inserting figures at a line break works in Word2010. The figures are always left-justified. The description of the figure (e.g. Figure 1: The PRACE logo inserted with text) can be generated by right clicking on the Figure and selecting ‘Insert Caption’ (or the equivalent in the national language that Word is using) and place the caption below the Figure. Enter the title, numbering is automatic. All references to figures within the text must be through cross references (Select: Insert > References > Figure). This ensures that the numbering will remain correct, even if figures are deleted or inserted. Do **not** use absolute numbers (you will pay for this later!).

### Section Title – Level 1 (Graphic on Page)

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Figure 2: This is floating text around the figure with a very long figure subscript that extends over more than one line in the List of Figures (avoid if possible)

In Word2010 you may select the position of the figure anywhere on the page and add figure subscripts that are correctly included in the List of Figures. This feature does not work when you maintain compatibility with Word2003 or in a native Word2003 document.

You can load a Word2010 (.docx) document containing figures like the one in Figure 1 into Word2003 (if you have the converter installed) and view it. However, this figure will not appear in the List of Figures.

Historic note: In the older versions of Word there is a feature called Position Frame that supports this. This is a terrible nuisance, since the figures tend to jump on the page whenever text is added or deleted.

Hint: Use concise Figure (and Table) captions. The full explanation should be in the text. The negative effect can be seen in above example. The Figure subscript overlays part of the footer and produces a cluttered List of Figures.

## Section Title (Tables)

<Text begins here.>

This section shows examples how tables can be inserted into the document and how it is insured that the table subscript is properly included into the List of Tables.

Tables must explicitly be referred to in the text. Tables without a reference are useless and should be removed. Caption for tables appears below the table. See for example: Table 1: Sample table with five columns.

| Number | Name1 | Name2 | Name3 | Name4 |
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Table 1: Sample table with five columns

Always use references to point to tables. Never use absolute numbers.

| **Number** | **Header1** | **Header2** | **Header3** |
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Table 2: Long Table spanning more than one page

If the table does not fit on a page, make sure that the header line is repeated. Mark the header line and the right click and select table properties’ and select ‘repeat header line’.

## Section Title (Text Fields)

Certain data items, like the project acronym or the title appear in several places in the document, e.g. in the header and footer lines. To avoid updating them in each individual place, they have been defined as ***text fields*** on the title page. **Change the text fields only on the title page.** The changed value will appear where ever it is referenced. (Depending on global Word options, the updates become visible only after previewing or printing the documents or if you explicitly select ‘Update Fields’.)

The following fields are defined:

| Text field name | Current value |
| --- | --- |
| DeliverableNumber | D7.5 |
| DeliverableTitle | Application performance on accelerators |
| Acronym |  |
| ReferenceNumber |  |
| PrepDate |  |
| Version | 0.1 |
| Author | Victor Cameo Ponz, |
| Status | Draft/Final |

Table 3: List of Text Fields

The actual values from the title pages are shown here. As a test change one of them on the title page and check how it is changes in column 2 of Table 3.

**The fact that the text on the title page is actually a text field is normally well hidden. To make it visible, click on the round Word button top left and Select Word Options > Extended > Show Text Markers.**

The effect will be that the text fields are shown in grey brackets (see Figure 3):

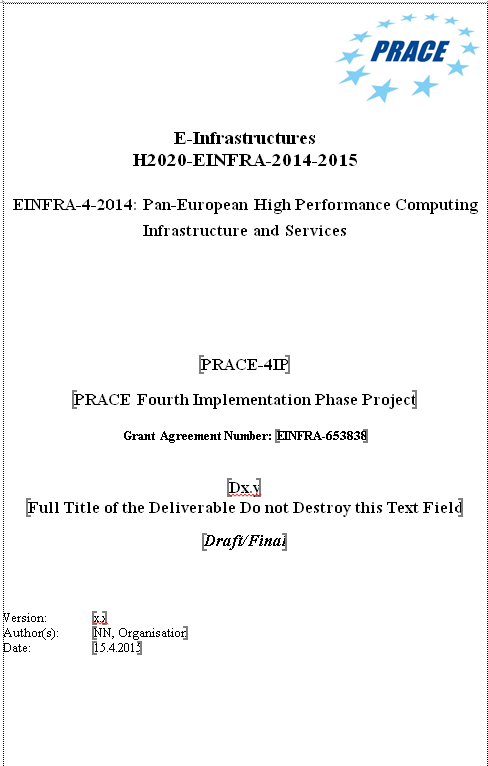


Figure 3: Title page with Text Fields

When changing the text, make sure that you stay within the brackets.

Select also**: Show all formatting** to see line breaks, spaces, tabs, etc. on the screen.

Note: Figure 3 is a screen shot of the title page of this document in jpg format. The Frame around it was added in Word.

## Section Title (General Hints)

When you display or print a document, Word does not always update all references (numbering of figures, updates of page numbers in the ToC and elsewhere) depending on global settings. To be sure everything is correct force the update manually: Press CTRL-a, right click and select update references.

You might be prompted several times for the Table of Contents (ToC), the List of Figures, and the List of Tables. Select update references at least once. If the ToC is correct, you may use Update Page Numbers.

Please verify that text or figures are formatted correctly by re-creating the Table of Contents (right click 🡪 update references). This will reveal if parts of the document are inadvertently formatted as headings.

When different authors contribute to the final deliverables, instruct them to adhere to the conventions described here, especially to use relative references to figures and tables. This will save time for everybody.

## Section Formatted as Landscape

This page is formatted as landscape for example to include a wide table. This is facilitated in Word by starting a new Section. To insure that headers and footers are left/right justified correctly, they must **NOT** be linked to the previous section. See the Word Help for this advanced feature.

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Table 4: Wide Table

The headers and footer of the following Portrait section are again **NOT** linked to this one.

**When you delete this Section make sure that the headers and footers of the next section are linked again to previous one.**

## Annex

*Annexes are optional but if included they form an integral part of the PRACE project report.*

<Text begins here.>

### Annex Title – Level 1

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### Annex Title – Level 1

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### Notes on appending Documents originating from PDF files

(Instructions courtesy Axel Auweter, LRZ)

It is often the case that one wants to append documents from third parties in the Annex section. If these documents are provided as PDF documents, including them to the deliverable while retaining the overall layout can be a tricky task. A working solution is to include the contents of the original document as image files on a page-by-page basis. Therefore, including an external document works in two steps:

* Step 1: Create image files from the original PDF file
* Step 2: Insert the image files to the deliverable

Please note that the EC only accepts PDF files smaller than 10MB. Since including external documents as images occupies quite some disk space, make sure that the final document does not exceed that limit.

*Step 1: Creating image files from the original PDF file*

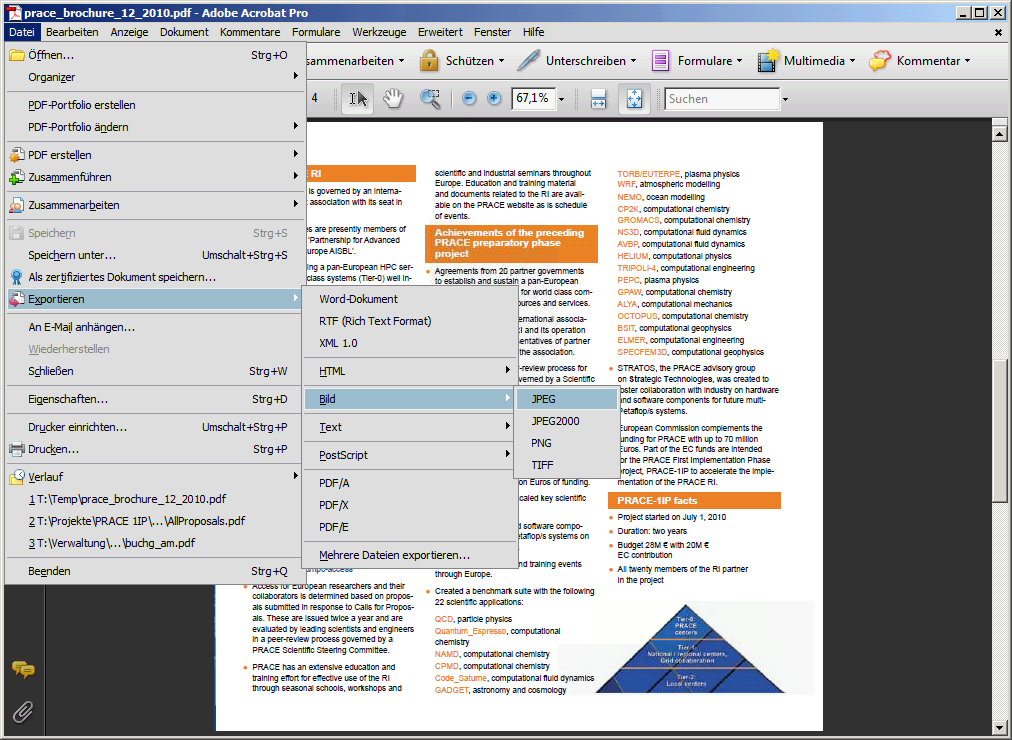


Figure 4: Creating an Image file from pdf

There are multiple options to achieve this. The easiest is to use Adobe Acrobat (you need the Pro version; the free Adobe Reader is not enough). In the File menu select Export/Image. This will create you one image per page in the selected graphics format.

If you do not have access to Adobe Acrobat, you can also do the conversion using the free ImageMagick set of command line utilities:

*convert –density <DPI> input.pdf output-pages-%03d.png*

Replace <DPI> with the desired image resolution (e.g. 600).

*Step 2: Insert the image files into the deliverable*

From the Insert Tab, choose Picture. A file dialog opens. Make sure to have the files showing in ascending order. Select (single click) the last (!) file that you want to insert. Then press the Shift key on your keyboard and hold it while you click on the first file that you want to insert.

You should see a screen that looks like this with all files showing in the right order at the bottom of the dialog window:

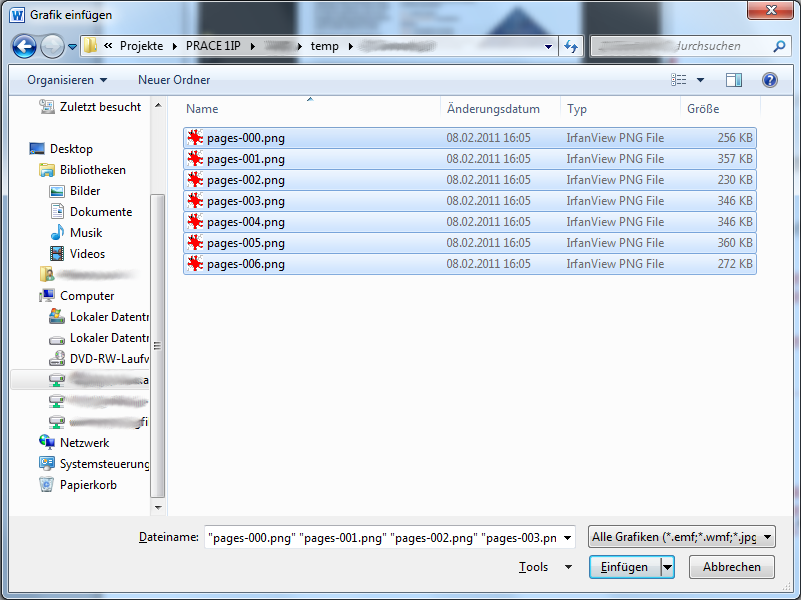


Figure 5: Inserting image files

If you click on “Insert”, your images will be inserted into the document in the right order at a suitable size automatically.