Measure your Frequency at the Slow Corner
Slow 1200 mV 100C Model Fmax Summary
Fmax = 126.95 MHz
Restricted Fmax = 126.95 MHz

Slow 1200mV 100C Model Fmax Summary

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	Fmax	Restricted Fmax	Clock Name	Note
1	126.95 MHz	126.95 MHz	clk	

Measure Your Power with a 20% input activity factor
Total Thermal Power Dissipation: 336.53 mW
Core Dynamic Thermal Power Dissipation: 31.88 mW
Core Static Thermal Dissipation: 119.58 mW
I/O Thermal Power Dissipation: 185.06 mW

Power Analyzer Summary

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Power Analyzer Status	Successful - Tue Nov 25 21:00:26 2025
Quartus Prime Version	19.1.0 Build 670 09/22/2019 SJ Lite Edition
Revision Name	corelet_fpga
Top-level Entity Name	corelet
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Power Models	Final
Total Thermal Power Dissipation	336.53 mW
Core Dynamic Thermal Power Dissipation	31.88 mW
Core Static Thermal Power Dissipation	119.58 mW
I/O Thermal Power Dissipation	185.06 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Power Analyzer Settings

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	Option	Setting	Default Value
1	Use smart compilation	Off	Off
2	Enable parallel Assembler and...g Analyzer during compilation	On	On
3	Enable compact report table	Off	Off
4	Default Power Input I/O Toggle Rate	25390000.0transitions/s	12.5%
5	Power Analyzer Report Signal Activity	On	Off
6	Power Analyzer Report Power Dissipation	On	Off
7	Preset Cooling Solution	23 MM HEAT SINK WITH 200 LFPM AIRFLOW	
8	Board thermal model	None (CONSERVATIVE)	
9	Default Power Toggle Rate	12.5%	12.5%
10	Use vectorless estimation	On	On
11	Use Input Files	Off	Off
12	Filter Glitches in VCD File Reader	On	On
13	Device Power Characteristics	TYPICAL	TYPICAL
14	Automatically Compute Junction Temperature	On	On
15	Specified Junction Temperature	25	25
16	Ambient Temperature	25	25
17	Use Custom Cooling Solution	Off	Off
18	Board Temperature	25	25

TOPS/s = (# of MACs * Frequency) / 1e12 = (128 ops/cycle * 126,950,000 Hz) / 1e12 = 0.01623 TOPS
TOPS/W = (TOPS) / (Power (W)) = 0.01623 TOPS / 0.03188 W = 0.5019 TOPS/W

Resource Usage
Total Logic Elements: 16,711
Logic Elements Usage by # of LUT inputs

- 4 input: 8786
- 3 input: 1856
- <= 2 input: 951
- Register Only: 5118

Registers: 12,106

Fitter Resource Usage Summary

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	Resource	Usage
1	Total logic elements	16,711 / 149,760 (11 %)
1	-- Combinational with no register	4605
2	-- Register only	5118
3	-- Combinational with a register	6988
2		
3	Logic element usage by number of LUT inputs	
1	-- 4 input functions	8786
2	-- 3 input functions	1856
3	-- <=2 input functions	951
4	-- Register only	5118
4		
5	Logic elements by mode	
1	-- normal mode	9697
2	-- arithmetic mode	1896
6		
7	Total registers*	12,106 / 152,165 (8 %)
1	-- Dedicated logic registers	12,106 / 149,760 (8 %)
2	-- I/O registers	0 / 2,405 (0 %)
8		

9	Total LABs: partially or completely used	1,391 / 9,360 (15 %)
10	Virtual pins	0
11	I/O pins	456 / 508 (90 %)
1	-- Clock pins	3 / 10 (30 %)
2	-- Dedicated input pins	0 / 25 (0 %)
12		
13	M9Ks	0 / 720 (0 %)
14	Total block memory bits	0 / 6,635,520 (0 %)
15	Total block memory implementation bits	0 / 6,635,520 (0 %)
16	Embedded Multiplier 9-bit elements	0 / 720 (0 %)
17	PLLs	0 / 8 (0 %)
18	Global signals	2
1	-- Global clocks	2 / 30 (7 %)
19	JTAGs	0 / 1 (0 %)
20	CRC blocks	0 / 1 (0 %)
21	ASMI blocks	0 / 1 (0 %)
22	Oscillator blocks	0 / 1 (0 %)
23	GXB Receiver channel PCSs	0 / 8 (0 %)

24	GXB Receiver channel PMAs	0 / 8 (0 %)
25	GXB Transmitter channel PCSs	0 / 8 (0 %)
26	GXB Transmitter channel PMAs	0 / 8 (0 %)
27	Impedance control blocks	0 / 3 (0 %)
28	Average interconnect usage (total/H/V)	4.5% / 3.9% / 5.2%
29	Peak interconnect usage (total/H/V)	27.3% / 25.3% / 30.3%
30	Maximum fan-out	12106
31	Highest non-global fan-out	1364
32	Total fan-out	84196
33	Average fan-out	2.89