**9-Bit Sequence Recognizer Test Vector Generation**

In the first lab, three vectors were generated as basic tests of the circuit’s operation against the requirements of the specification. All these vectors were included in the final draft of the combined vector for this circuit that was eventually submitted, although all had some minor alterations. Here their final forms will be discussed with references to why any changes were made.

The first test inputs a single string of correct bits according to the sequence in the specification. Originally, this test only clocked in the sequence to show that *MatchAll* was asserted, however, it was modified so that the last bit of the sequence was clocked in manually. This allowed the assertion of *MatchAll* to be observed in greater detail and ensured that it was asserted on the rising edge and for a single clock cycle.

The second sequence tests the robustness of the circuit to incorrect bits and false starts by applying some specifically chosen ‘random’ bits before and after a single correct sequence. These ‘random’ bits were chosen to contain some false starts and to test the circuits ability to reject incorrect sequences.

The third vector doesn’t test timing but simply inputs two correct overlapping sequences to test this functionality. The only modification to this test was to apply some random bits at the end as a test of the circuit’s robustness under these conditions.

When these vectors inputted to the chip in the first lab, they returned no errors, indicating that the circuit was operating as expected in that respect and could fulfill these basic requirements. Similarly, when these vectors were run on the original Verilog model generated from the schematic, they indicated no errors.

Since the basic operation of the circuit against the specification had been proven, the fourth vector is based on the design, specifically the ASM chart. This test works by entering each state and take every possible branch. This is achieved by working through each state in turn and taking the incorrect branch before returning to the state and taking the correct branch. The vector after an incorrect branch is for the state the circuit should have jumped to. The original draft of this test moved from each incorrect bit directly to the next test. However, this proved to be unhelpful with the lack of observability in the circuit. Therefore, the final draft takes the system through every state to provide a correct sequence and set *MatchAll* high after every incorrect branch before resetting the circuit for the next test. This allowed for any faults to be more easily and accurately identified. It also meant that any faults early in the test wouldn’t impact any subsequent tests.

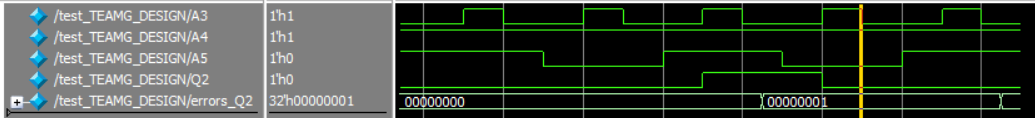


Figure X

The plot generated from simulating the state *0111* errors test vector shows that the nature of the fault is that *MatchAll* (*Q2*) is asserted two clock cycles before it should be. Observing the time between the two errors on the bottom trace shows this and since there are only two possible values, we can say without the referring to the vector that the value of *MatchAll* at each error should be inverted.

When both tests were simulated on the Verilog model, they both returned errors. The errors returned from the first of these more thorough tests indicated that the error was with state *0111* however, due to the previously mentioned flaws with this test, it was hard to determine the exact nature of the fault. This was when the files were altered as described. To get a clearer idea of the fault, I extracted the vectors which raised the errors and ran them separately in a new test, so that the faults could be debugged more easily. The result of this simulation is seen in Figure X. The errors both relate to the *MatchAll* signal being asserted two clock cycles early indicating that the circuit was two states ahead of where it should have been.

Observing the ASM chart determined that the destination state should be two states earlier than state *0111*, therefore, the circuit was staying in the same state. The differences between state *0111* and the state two previous (*0100*) are the values at the *Q1* and *Q0* flip-flops. Subsequently, the faults could be narrowed down to the next state logic for those two flip-flops.

Comparing the equation for *Q0n* to the schematic, showed that an error had been made in the first term where had been implemented as on the schematic and subsequently the layout. Working through the logic for *Q1n* determined that the error was with the term . This was a mistake in the equations where should have been and the mistake had propagated through the schematic and the layout. Both these faults were corrected in the Golden Design and simulations showed expected behaviour and returned no further errors to all tests.