User Documentation

MAXwel

MAX ii Workbench for Education and Learning

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Contents

1 Hardware

1.1 Pinmap

To access the onboard LEDs, buttons and switches, knowing the connected GPIO pin of the FPGA is necessary. An overview about the accessories placed on the board is depicted in Fig. 1.1. This picture also numbered all of them for later identification where the corresponding pinmap is given in the subsequent sections.

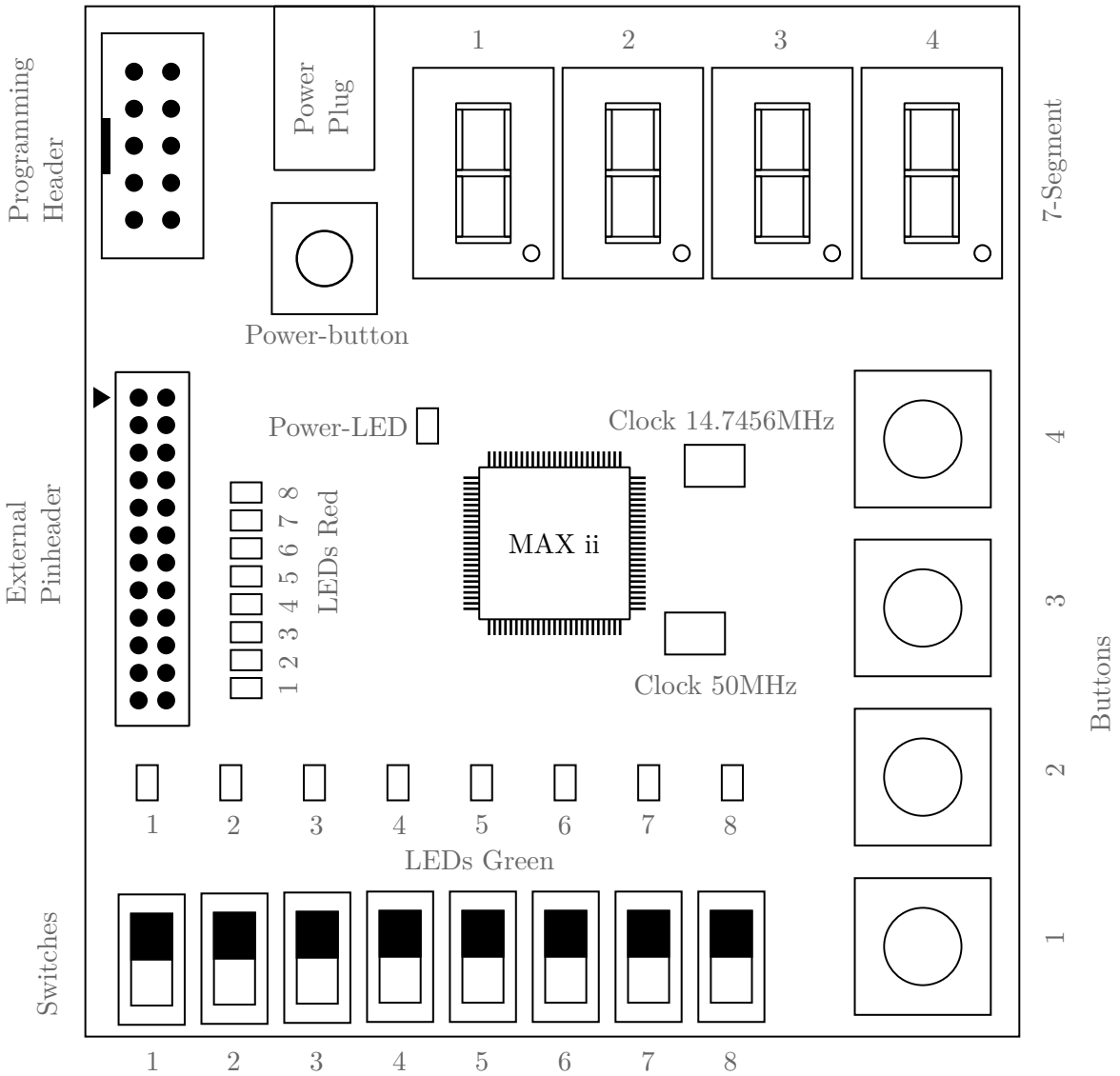

Figure 1.1: Floorplan of the MAXwel with labeled peripheral devices.

1.1.1 Power

The power supply is connected to the board via a barrel jack. A power button is placed next to the jack to turn the board on and off. To indicate the power state, a power LED is placed on the board that always lights when the board is powered.

1.1.2 Clocks

The board has two clock sources, a 50 MHz oscillator and a 14.7456 MHz oscillator. Both are connected to special GPIO pins that are dedicated for clock signals. These pins provide a low skew and jitter free clock signal and provide access to the internal global clock network of the FPGA.

Clock	FPGA Pin
50 MHz	PIN_12
14.7456 MHz	PIN_14

1.1.3 LEDs

The board has 16 LEDs, 8 green and 8 red, that can be controlled by the FPGA. To turn an LED on the corresponding pin has to be set to high.

LED number	LED Green FPGA Pin	LED Red FPGA Pin
1	PIN_61	PIN_86
2	PIN_58	PIN_85
3	PIN_57	PIN_84
4	PIN_56	PIN_51
5	PIN_55	PIN_50
6	PIN_54	PIN_49
7	PIN_53	PIN_48
8	PIN_52	PIN_47

1.1.4 Buttons and Switches

The board is equipped with 4 buttons and 8 switches. The buttons are debounced with a 8 kHz low pass filter and should drive the input pin to high when pressed.

Button number	FPGA Pin
1	PIN_97
2	PIN_98
3	PIN_99
4	PIN_100

The switches are also debounced with a 8 kHz low pass filter and should drive the input pin to high when the switch is in the upper position.

Switch number	FPGA Pin
1	PIN_87
2	PIN_88
3	PIN_89
4	PIN_90
5	PIN_91
6	PIN_92
7	PIN_95
8	PIN_96

1.1.5 Seven Segment Display

The MAXwel is equipped with a four digit seven segment display. The seven segment displays have a common anode: to turn on a segment the corresponding pin has to be set to high. The labels for the segments are depicted in Fig. 1.2.

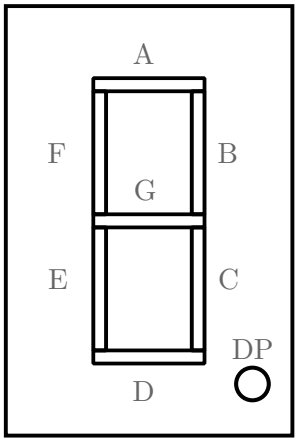

Figure 1.2: Seven segment display with labeled segments.

Segment Name	Segment 1	Segment 2	Segment 3	Segment 4
A	PIN_40	PIN_30	PIN_18	PIN_4
B	PIN_41	PIN_33	PIN_19	PIN_5
C	PIN_42	PIN_34	PIN_20	PIN_6
D	PIN_37	PIN_27	PIN_15	PIN_1
E	PIN_38	PIN_28	PIN_16	PIN_2
F	PIN_39	PIN_29	PIN_17	PIN_3
G	PIN_44	PIN_36	PIN_26	PIN_8
DP	PIN_43	PIN_35	PIN_21	PIN_7

1.1.6 External pin header

The orientation of the external pin header is determined by the reference triangle. All Pins on the pin header are connected directly to the GPIO pins of the FPGA so take care when connecting external devices to the board. Do not exceed the voltage range of 0 V to 3.3 V and do not draw too much current from the pins. The pin header is depicted in Fig. 1.3.

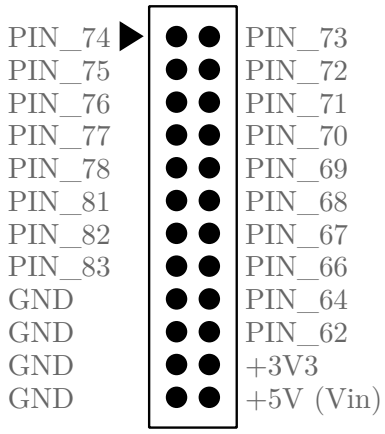

Figure 1.3: External pin header with labeled pins.

1.1.7 Programming header

The programming header is used to program the FPGA with a JTAG programmer. The pinout of the programming header is depicted in Fig. 1.4. The *TCK* pin is connected to a 10 kΩ pull down resistor and the *TDI*, *TMS* and *TDO* pins are connected to a 10 kΩ pull up resistor.

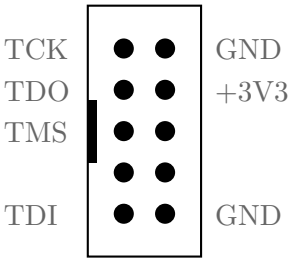

Figure 1.4: Programming header with labeled pins.