CS-211

Processor Design – Lab Report

Three and Four stage pipeline processor

Name: Mithun P

Roll No: 2203314

Three Staged Pipelined Implementation of R and I-type(addi) 32 bit CPU:

Instruction set:

00000000 00000000

00000001 05031000 //SUb $2,$8,$3

00000002 00430800 //Add $1,$2,$3

00000003 0901F000 //AND $30, $8,$1

00000004 1502F800 //MUL $31,$8,$2

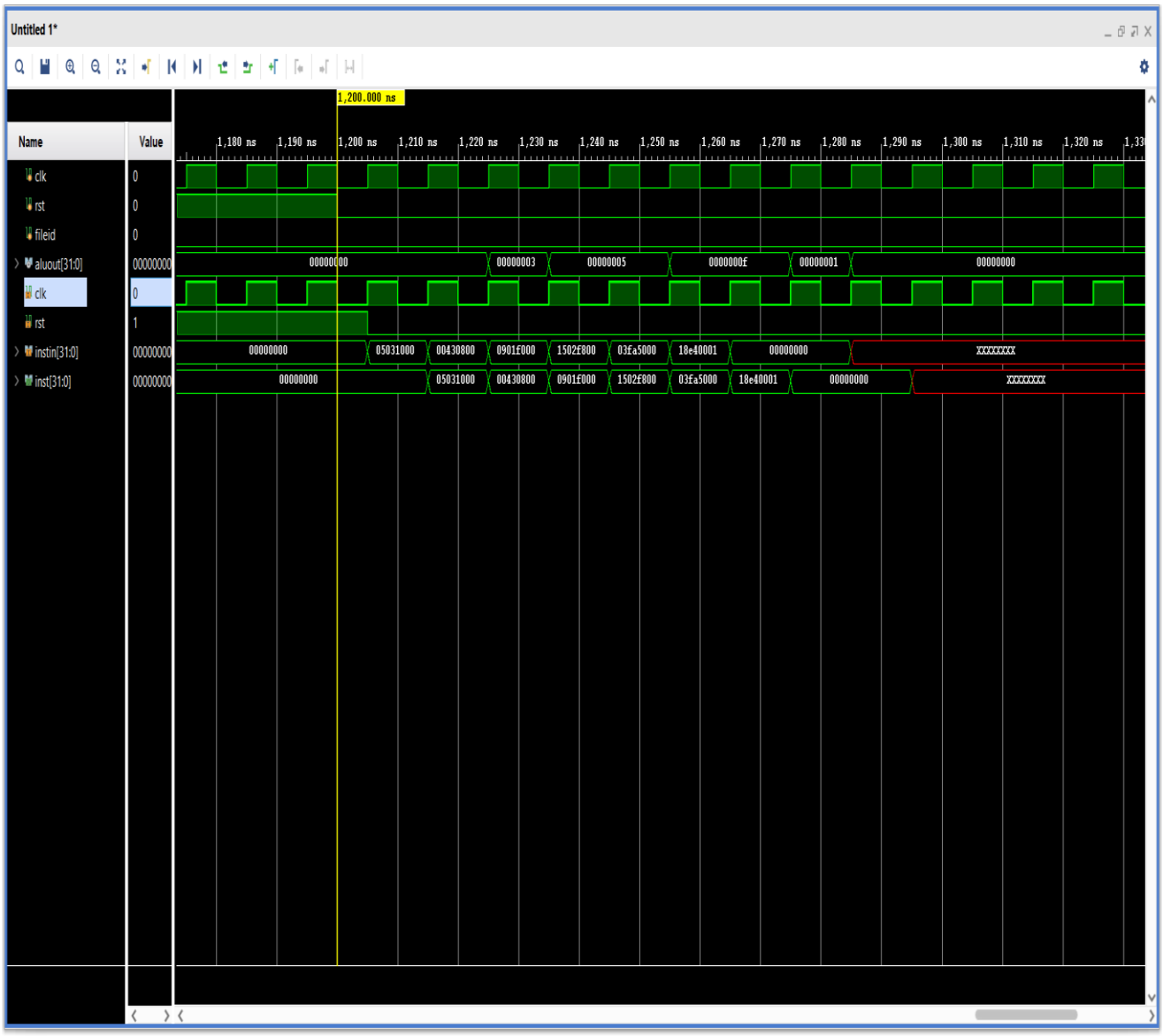
00000005 03fa5000 //ADD $10, $31,$26

00000006 18E40001 //ADDI $4,$7,1

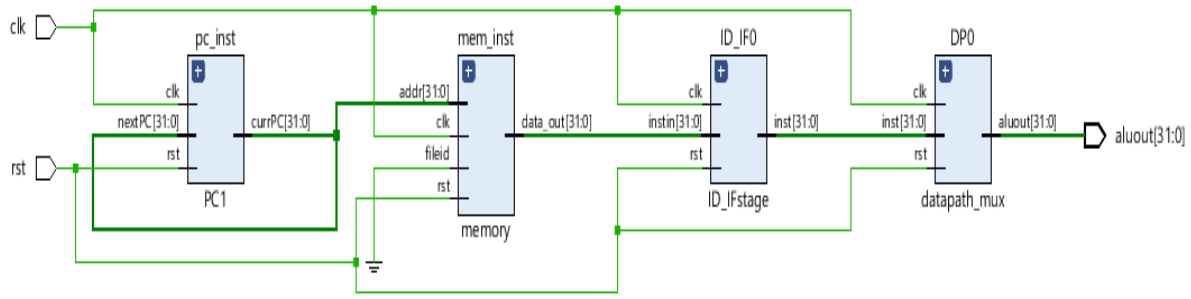
00000007 00000000 //NOP

00000008 00000000

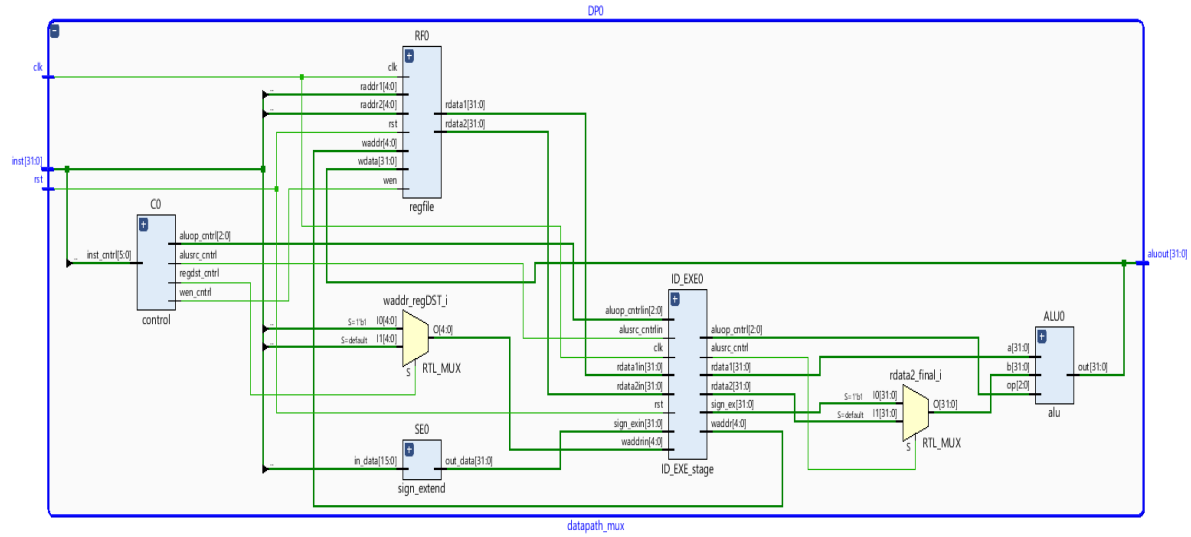
Simulation Waveform:



RTL Schematic:

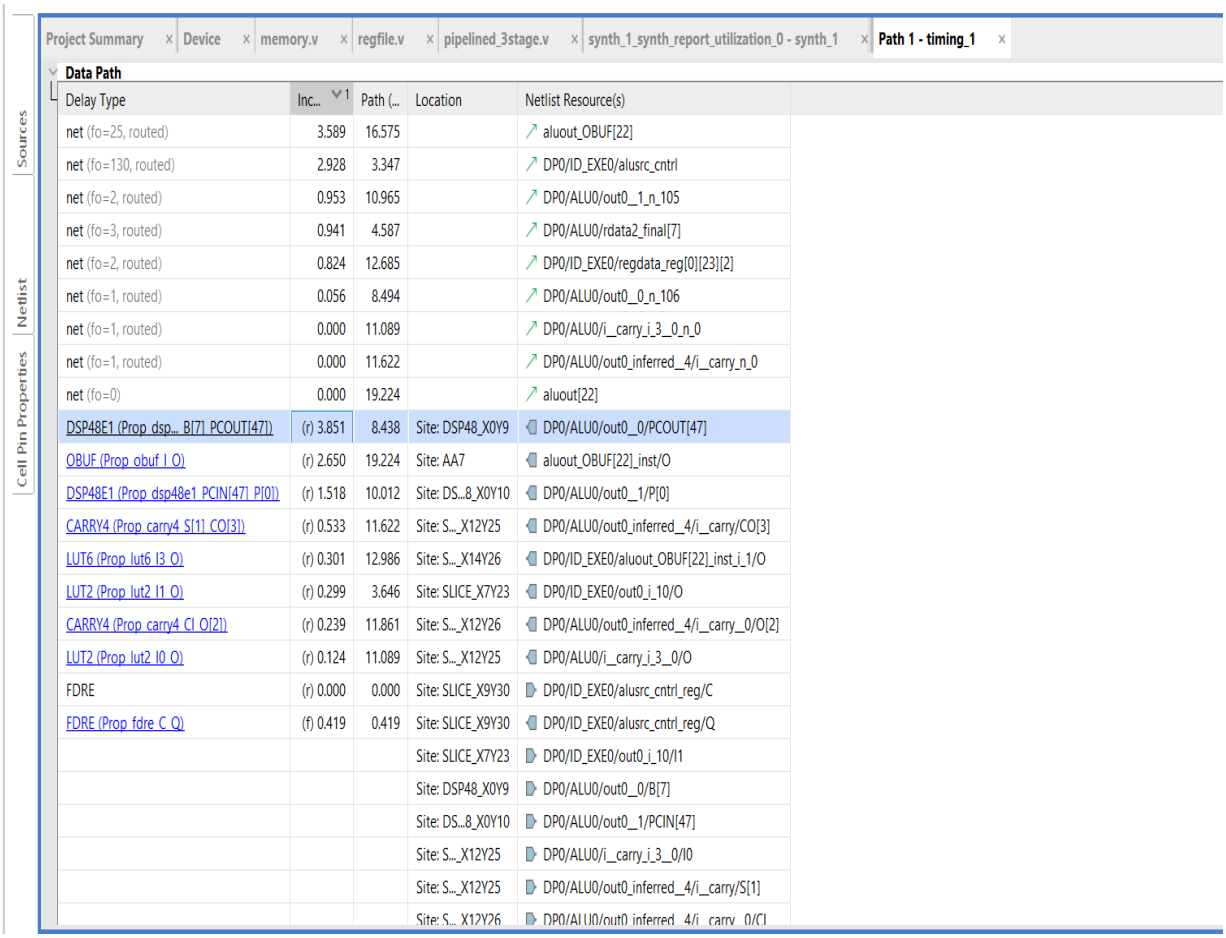


RTL schematic for the datapath_mux:



Area (LUT, FF, Slice utilization):

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	580	0	53200	1.09
LUT as Logic	580	0	53200	1.09
LUT as Memory	0	0	17400	0.00
Slice Registers	869	0	106400	0.82
Register as Flip Flop	869	0	106400	0.82
Register as Latch	0	0	106400	0.00
F7 Muxes	129	0	26600	0.48
F8 Muxes	64	0	13300	0.48



No. of LUTs used: 580

No. of registers as FF used: 869

Slice Utilization: 1.09(For LUTs), 0.82(For registers)

Maximum operating Frequency: 0.2596 (ns)^-1

Four Staged Pipelined Implementation of R and I-type(addi) 32 bit CPU:

Instruction set before adding NOPs:

00000000 00000000

00000001 05031000 //SUb $2,$8,$3

00000002 00430800 //Add $1,$2,$3

00000003 0901F000 //AND $30, $8,$1

00000004 1502F800 //MUL $31,$8,$2

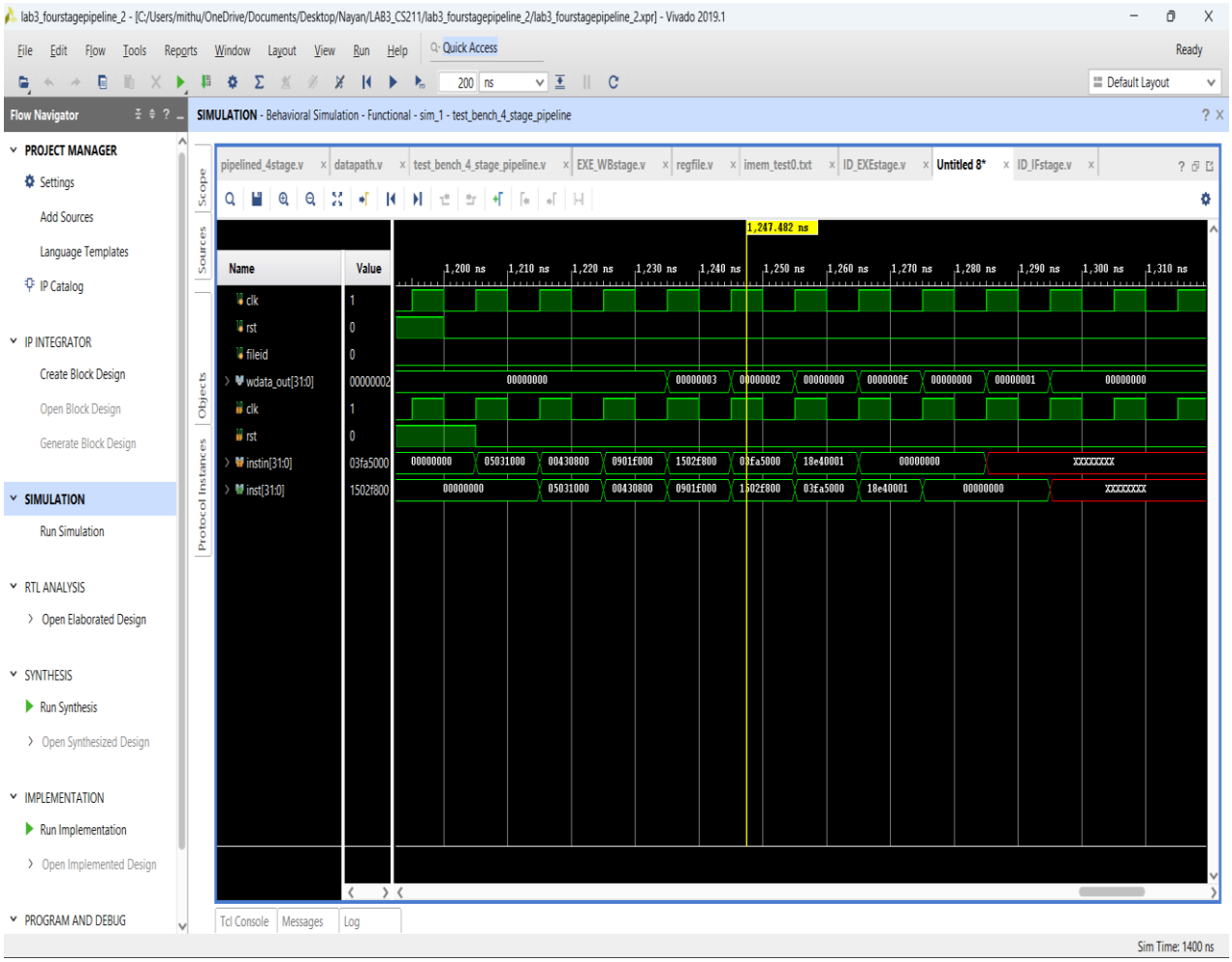
00000005 03fa5000 //ADD $10, $31,$26

00000006 18E40001 //ADDI $4,$7,1

00000007 00000000 //NOP

00000008 00000000

Simulation Waveform:



As we can see above, we find that Instruction1 depends on Instruction2, and Instruction2 depends on Instruction3, and Instruction4 depends on Instruction5[RAW data dependency]. Therefore, we need to add a NOP(null operation) instruction in between them to prevent getting the wrong answers.

Instruction set after adding NOPs:

00000000 00000000

00000001 05031000 //SUb $2,$8,$3

00000002 00000000 //NOP

00000003 00430800 //Add $1,$2,$3

00000004 00000000 //NOP

00000005 0901F000 //AND $30, $8,$1

00000006 1502F800 //MUL $31,$8,$2

00000007 00000000 //NOP

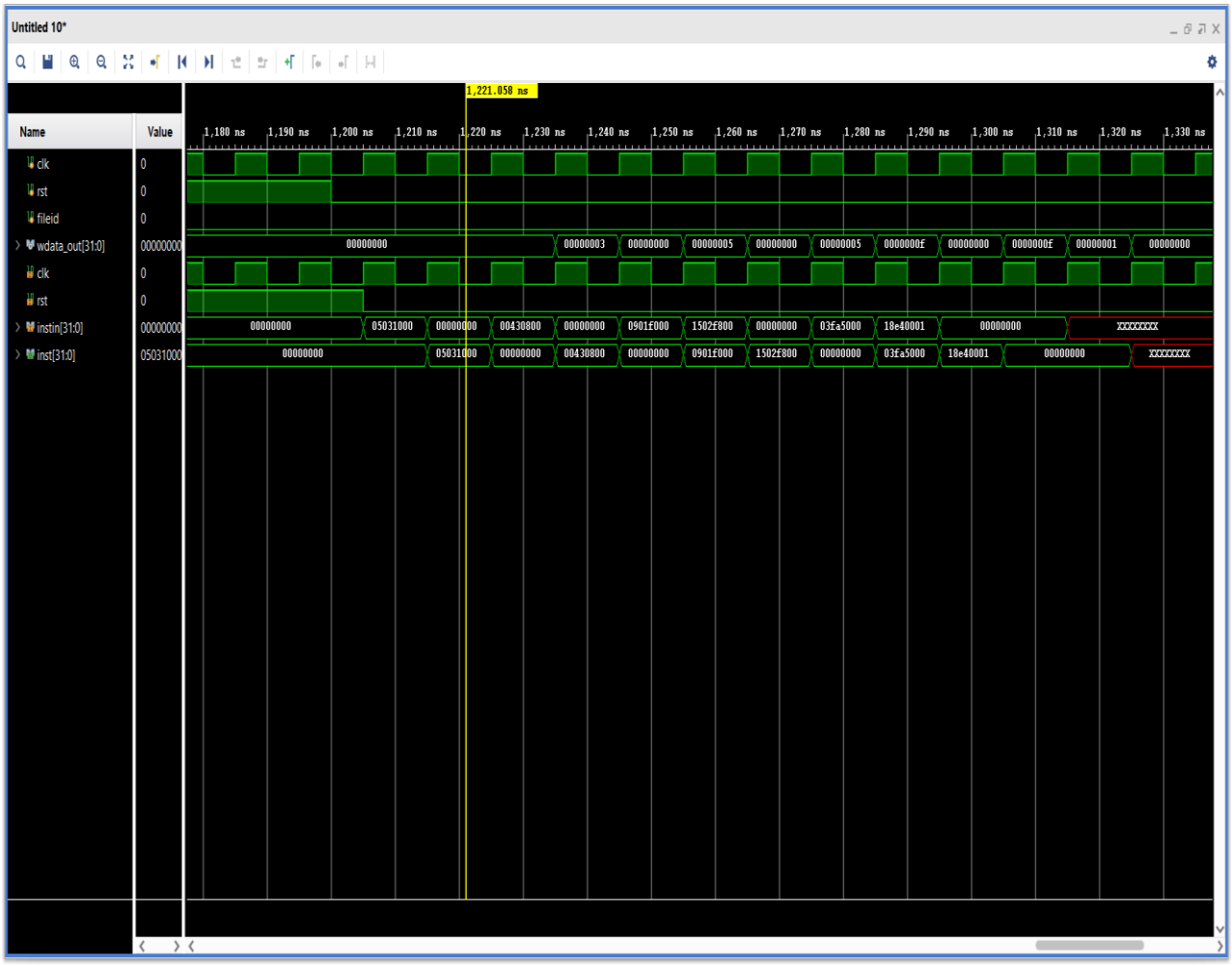
00000008 03fa5000 //ADD $10, $31,$26

00000009 18E40001 //ADDI $4,$7,1

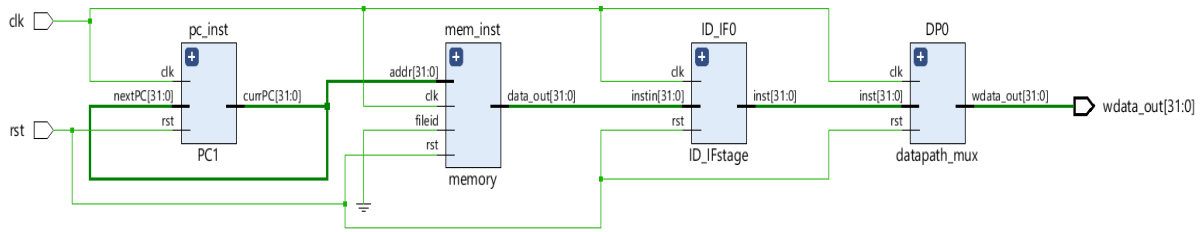
0000000a 00000000 //NOP

0000000b 00000000

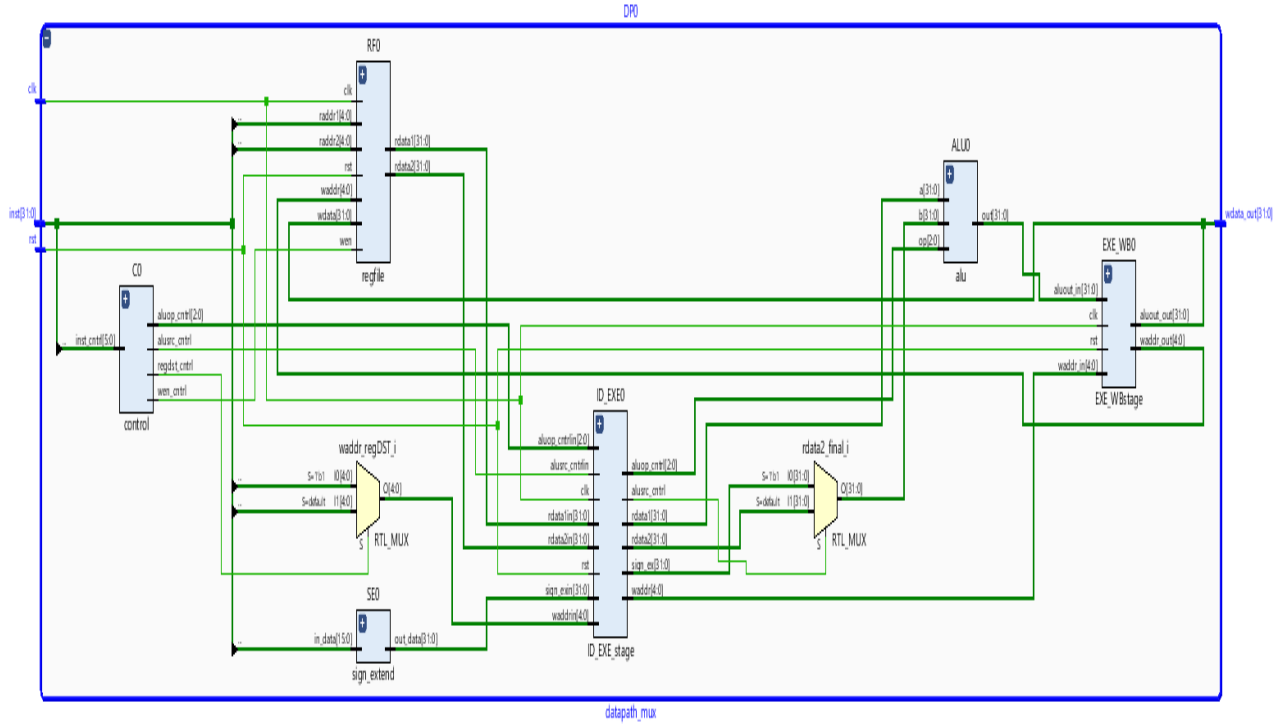
Simulation Waveform:



RTL Schematic:



RTL schematic for the datapath_mux:



Area (LUT, FF, Slice utilization):

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	551	0	53200	1.04
LUT as Logic	551	0	53200	1.04
LUT as Memory	0	0	17400	0.00
Slice Registers	906	0	106400	0.85
Register as Flip Flop	906	0	106400	0.85
Register as Latch	0	0	106400	0.00
F7 Muxes	160	0	26600	0.60
F8 Muxes	0	0	13300	0.00

Logic Levels 10 (CARRY4=3 DSP48E1=2 FDRE=1 LUT2=1 LUT3=1 LUT4=1 MUXF7=1)

Data Path

Delay Type	Inc...	Path (...	Location	Netlist Resource(s)
net (fo=138, routed)	2.105	2.561		DP0/ID_EXE0/alusrc_cntrl
net (fo=2, routed)	1.329	10.612		DP0/ALU0/out0__1_n_103
net (fo=2, routed)	1.274	14.076		DP0/EXE_WB0/aluout_out_reg[31]_1[24]
net (fo=5, routed)	1.227	3.912		DP0/ALU0/rdata2_final[15]
net (fo=1, routed)	0.815	12.289		DP0/ID_EXE0/aluout_out_reg[27][0]
net (fo=1, routed)	0.002	7.765		DP0/ALU0/out0__0_n_106
net (fo=1, routed)	0.000	10.736		DP0/ALU0/i__carry_i_1__0_n_0
net (fo=1, routed)	0.000	11.137		DP0/ALU0/out0_inferred__4/i__carry_n_0
net (fo=1, routed)	0.000	11.251		DP0/ALU0/out0_inferred__4/i__carry__0_n_0
net (fo=1, routed)	0.000	12.588		DP0/ID_EXE0/aluout_out[24]_i_3_n_0
DSP48E1 (Prop_dsp... B[15]_PCOUT[47])	(r) 3.851	7.763	Site: DSP48_X0Y2	DP0/ALU0/out0__0/PCOUT[47]
DSP48E1 (Prop_dsp48e1_PCIN[47]_P[2])	(r) 1.518	9.283	Site: DSP48_X0Y3	DP0/ALU0/out0__1/P[2]
FDRE (Prop_fdre_C_Q)	(r) 0.456	0.456	Site: SLICE_X5Y4	DP0/ID_EXE0/alusrc_cntrl_reg/Q
CARRY4 (Prop_carry4_S[3]_CO[3])	(r) 0.401	11.137	Site: SLICE_X11Y9	DP0/ALU0/out0_inferred__4/i__carry/CO[3]
LUT4 (Prop_lut4_I3_O)	(r) 0.299	12.588	Site: S..._X12Y11	DP0/ID_EXE0/aluout_out[24]_i_3/O
CARRY4 (Prop_carry4_CI_O[0])	(r) 0.222	11.473	Site: S..._X11Y11	DP0/ALU0/out0_inferred__4/i__carry__1/O[0]
MUXF7 (Prop_muxf7_I1_O)	(r) 0.214	12.802	Site: S..._X12Y11	DP0/ID_EXE0/aluout_out_reg[24]_i_1/O
LUT3 (Prop_lut3_I2_O)	(r) 0.124	2.685	Site: SLICE_X7Y8	DP0/ID_EXE0/out0_i_2/O
LUT2 (Prop_lut2_I0_O)	(r) 0.124	10.736	Site: SLICE_X11Y9	DP0/ALU0/i__carry_i_1__0/O
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.114	11.251	Site: S..._X11Y10	DP0/ALU0/out0_inferred__4/i__carry__0/CO[3]
FDRE	(r) 0.000	0.000	Site: SLICE_X5Y4	DP0/ID_EXE0/alusrc_cntrl_reg/C
			Site: SLICE_X7Y8	DP0/ID_EXE0/out0_i_2/I2
			Site: DSP48_X0Y2	DP0/ALU0/out0__0/B[15]

No. of LUTs used: 551

No. of registers as FF used: 906

Slice Utilization: 1.04(for LUTs), 0.85(for registers)

Maximum operating Frequency: 0.2596 (ns)^-1

The delay for four staged pipeline is relatively less compared to that of three staged pipeline.