

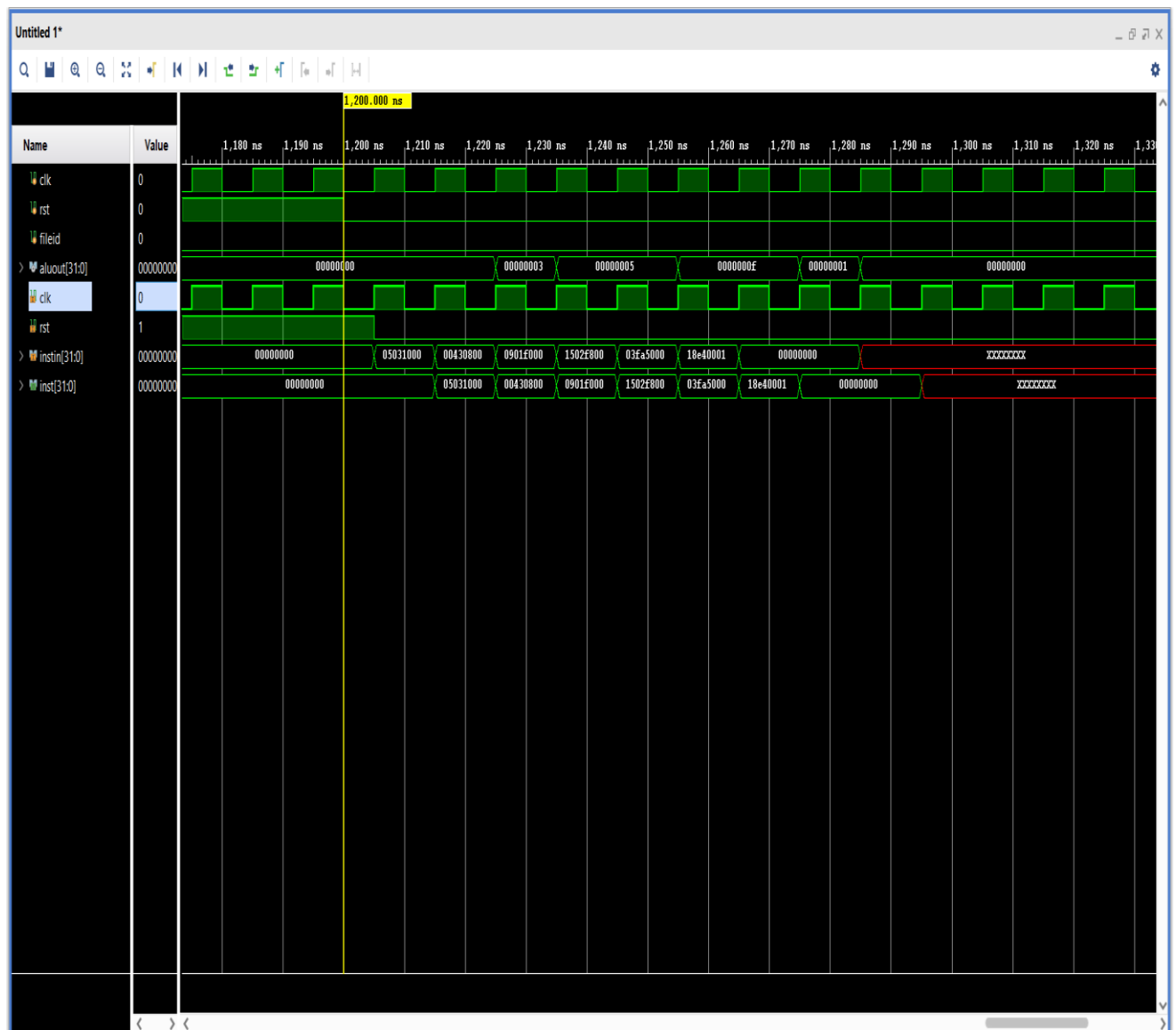
CS-211

Processor Design – Lab Report

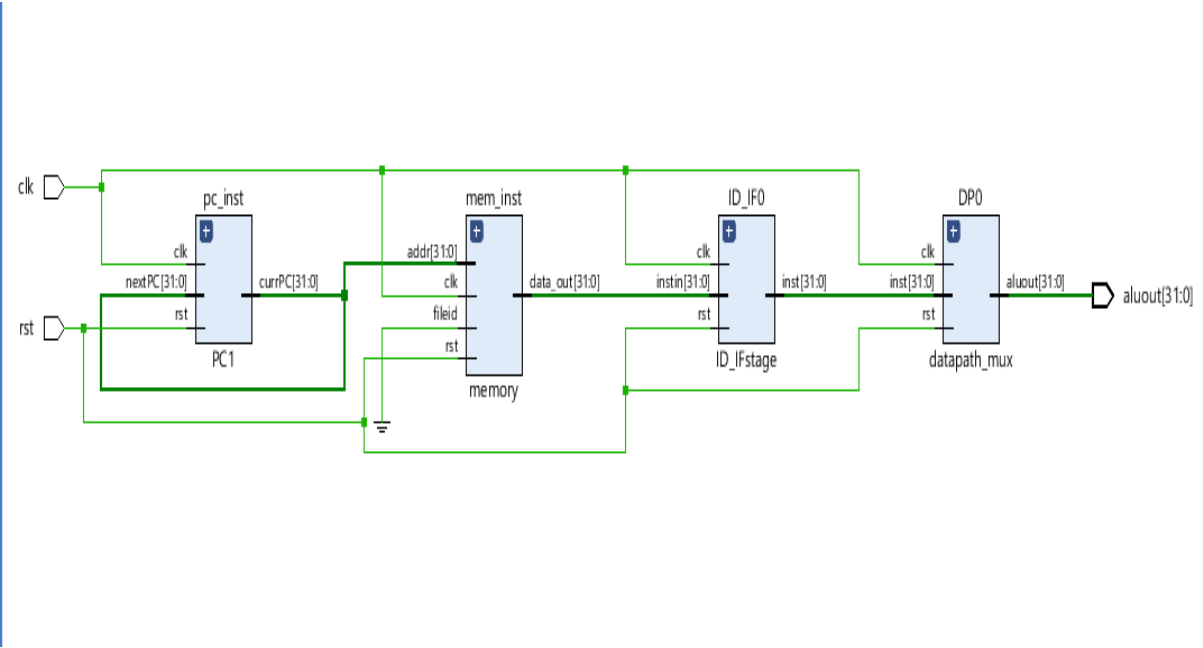
Three and Four stage pipeline processor

Name: Mithun P

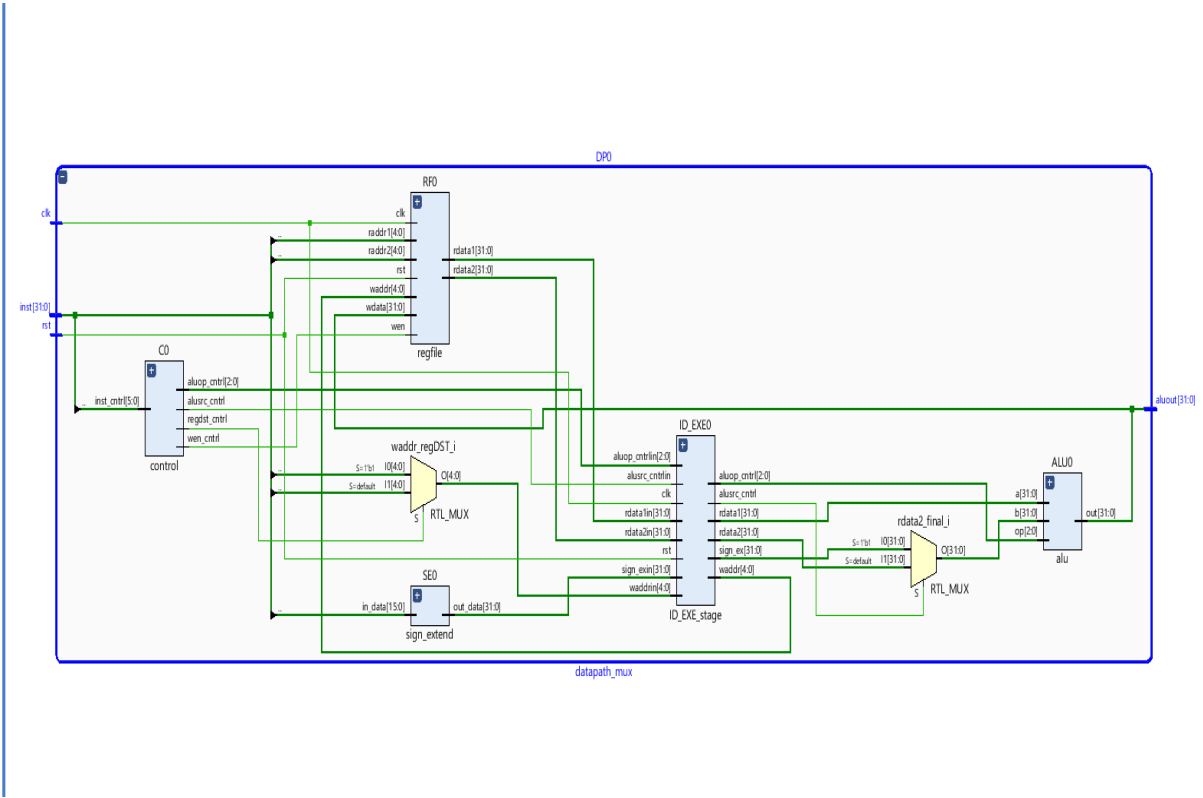
Roll No: 2203314



RTL Schematic:



RTL schematic for the datapath_mux:



Area (LUT, FF, Slice utilization):

| Site Type | Used | Fixed | Available | Util% |
|-----------------------|------|-------|-----------|-------|
| Slice LUTs* | 580 | 0 | 53200 | 1.09 |
| LUT as Logic | 580 | 0 | 53200 | 1.09 |
| LUT as Memory | 0 | 0 | 17400 | 0.00 |
| Slice Registers | 869 | 0 | 106400 | 0.82 |
| Register as Flip Flop | 869 | 0 | 106400 | 0.82 |
| Register as Latch | 0 | 0 | 106400 | 0.00 |
| F7 Muxes | 129 | 0 | 26600 | 0.48 |
| F8 Muxes | 64 | 0 | 13300 | 0.48 |

| | | | | | |
|---|-----------|------------|--------------------|---|--|
| Project Summary x Device x memory.v x regfile.v x pipelined_3stage.v x synth_1_synth_report_utilization_0 - synth_1 x Path 1 - timing_1 x | | | | | |
| Data Path | | | | | |
| Delay Type | Inc... | Path (...) | Location | Netlist Resource(s) | |
| net (fo=25, routed) | 3.589 | 16.575 | | aluout_OBUF[22] | |
| net (fo=130, routed) | 2.928 | 3.347 | | DP0/ID_EXE0/alusrc_cntrl | |
| net (fo=2, routed) | 0.953 | 10.965 | | DP0/ALU0/out0_1_n_105 | |
| net (fo=3, routed) | 0.941 | 4.587 | | DP0/ALU0/rdata2_final[7] | |
| net (fo=2, routed) | 0.824 | 12.685 | | DP0/ID_EXE0/regdata_reg[0][23][2] | |
| net (fo=1, routed) | 0.056 | 8.494 | | DP0/ALU0/out0_0_n_106 | |
| net (fo=1, routed) | 0.000 | 11.089 | | DP0/ALU0/i_carry_i_3_0_n_0 | |
| net (fo=1, routed) | 0.000 | 11.622 | | DP0/ALU0/out0_inferred_4/i_carry_n_0 | |
| net (fo=0) | 0.000 | 19.224 | | aluout[22] | |
| DSP48E1 (Prop dsp... B[7] PCOUT[47]) | (r) 3.851 | 8.438 | Site: DSP48_X0Y9 | DP0/ALU0/out0_0/PCOUT[47] | |
| OBUF (Prop obuf I O) | (r) 2.650 | 19.224 | Site: AA7 | aluout_OBUF[22].inst/O | |
| DSP48E1 (Prop dsp48e1 PCIN[47] P[0]) | (r) 1.518 | 10.012 | Site: DS...8_X0Y10 | DP0/ALU0/out0_1/P[0] | |
| CARRY4 (Prop carry4 S[1] CO[3]) | (r) 0.533 | 11.622 | Site: S...X12Y25 | DP0/ALU0/out0_inferred_4/i_carry/CO[3] | |
| LUT6 (Prop lut6 I3 O) | (r) 0.301 | 12.986 | Site: S...X14Y26 | DP0/ID_EXE0/aluout_OBUF[22].inst_i_1/O | |
| LUT2 (Prop lut2 I1 O) | (r) 0.299 | 3.646 | Site: SLICE_X7Y23 | DP0/ID_EXE0/out0_i_10/O | |
| CARRY4 (Prop carry4 CI O[2]) | (r) 0.239 | 11.861 | Site: S...X12Y26 | DP0/ALU0/out0_inferred_4/i_carry_0/O[2] | |
| LUT2 (Prop lut2 IO O) | (r) 0.124 | 11.089 | Site: S...X12Y25 | DP0/ALU0/i_carry_i_3_0/O | |
| FDRE | (r) 0.000 | 0.000 | Site: SLICE_X9Y30 | DP0/ID_EXE0/alusrc_cntrl_reg/C | |
| FDRE (Prop fdre C Q) | (f) 0.419 | 0.419 | Site: SLICE_X9Y30 | DP0/ID_EXE0/alusrc_cntrl_reg/Q | |
| | | | Site: SLICE_X7Y23 | DP0/ID_EXE0/out0_i_10/I1 | |
| | | | Site: DSP48_X0Y9 | DP0/ALU0/out0_0/B[7] | |
| | | | Site: DS...8_X0Y10 | DP0/ALU0/out0_1/PCIN[47] | |
| | | | Site: S...X12Y25 | DP0/ALU0/i_carry_i_3_0/I0 | |
| | | | Site: S...X12Y25 | DP0/ALU0/out0_inferred_4/i_carry/S[1] | |
| | | | Site: S...X12Y26 | DP0/ALU0/out0_inferred_4/i_carry_0/C1 | |

No. of LUTs used: 580

No. of registers as FF used: 869

Slice Utilization: 1.09(For LUTs), 0.82(For registers)

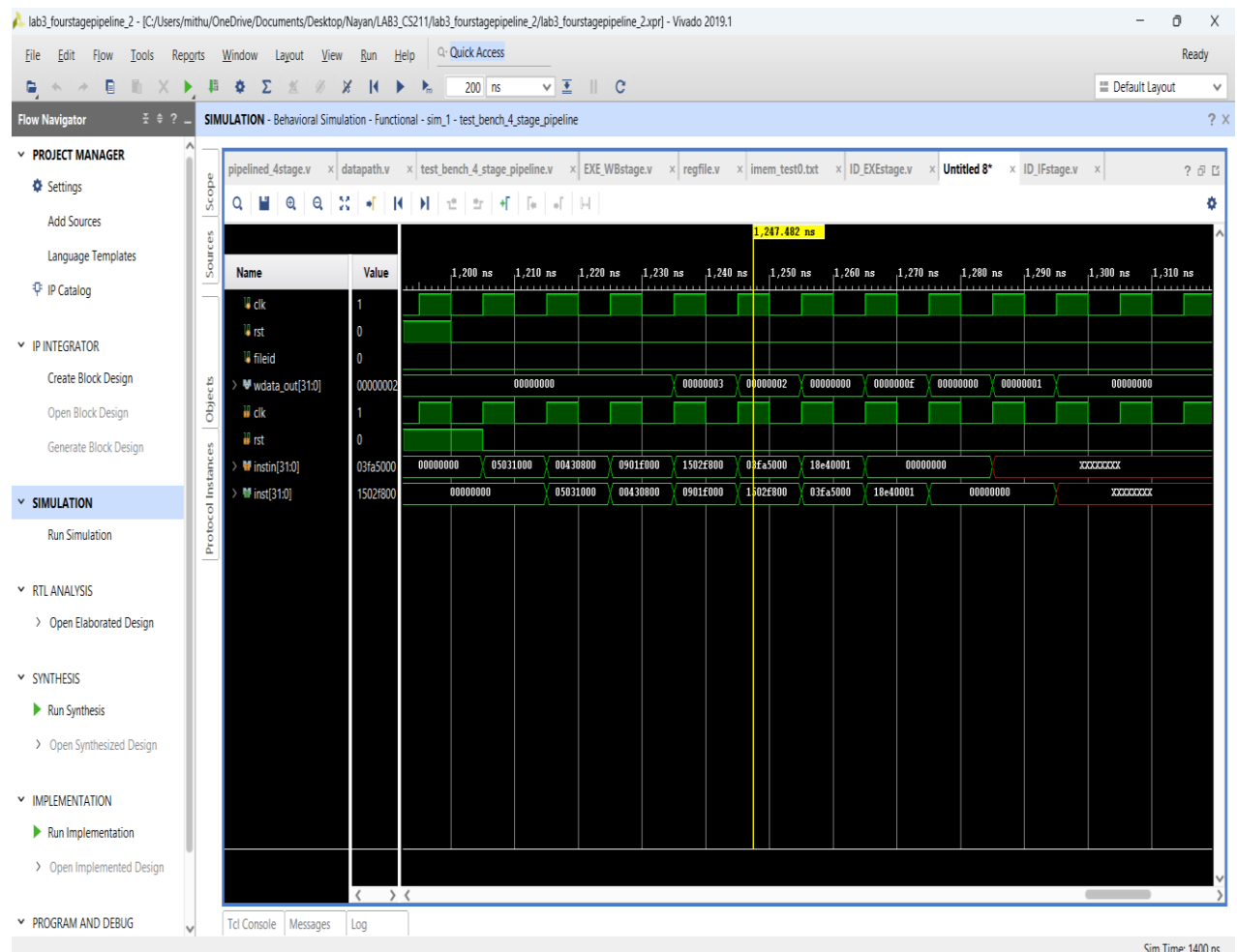
Maximum operating Frequency: 0.2596 (ns)^-1

Four Staged Pipelined Implementation of R and I-type(addi) 32 bit CPU:

Instruction set before adding NOPs:

```
00000000 00000000
00000001 05031000 //Sub $2,$8,$3
00000002 00430800 //Add $1,$2,$3
00000003 0901F000 //AND $30, $8,$1
00000004 1502F800 //MUL $31,$8,$2
00000005 03fa5000 //ADD $10, $31,$26
00000006 18E40001 //ADDI $4,$7,1
00000007 00000000 //NOP
00000008 00000000
```

Simulation Waveform:



As we can see above, we find that Instruction1 depends on Instruction2, and Instruction2 depends on Instruction3, and Instruction4 depends on Instruction5[RAW data dependency]. Therefore, we need to add a NOP(null operation) instruction in between them to prevent getting the wrong answers.

Instruction set after adding NOPs:

00000000 00000000

00000001 05031000 //SUB \$2,\$8,\$3

00000002 00000000 //NOP

00000003 00430800 //Add \$1,\$2,\$3

00000004 00000000 //NOP

00000005 0901F000 //AND \$30, \$8,\$1

00000006 1502F800 //MUL \$31,\$8,\$2

00000007 00000000 //NOP

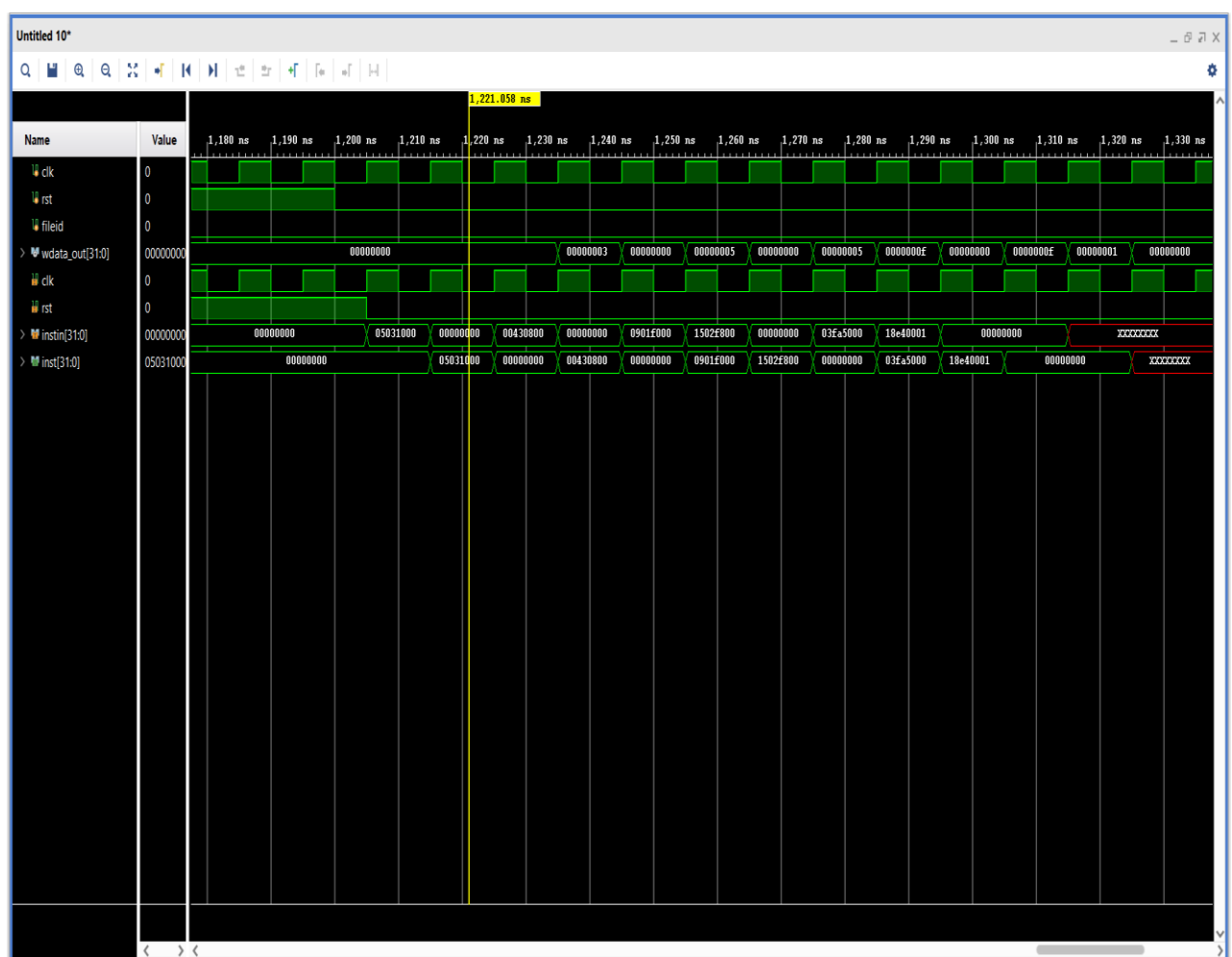
00000008 03fa5000 //ADD \$10, \$31,\$26

00000009 18E40001 //ADDI \$4,\$7,1

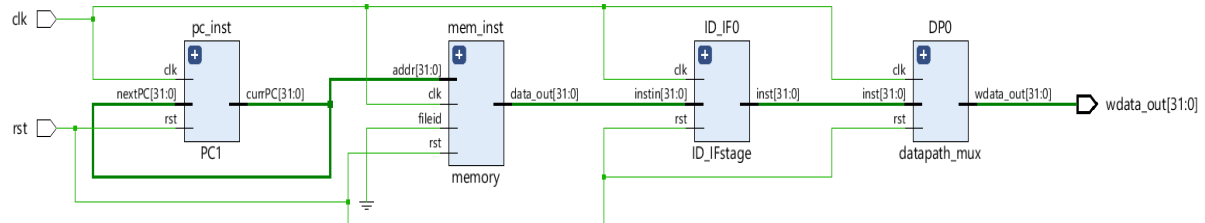
0000000a 00000000 //NOP

0000000b 00000000

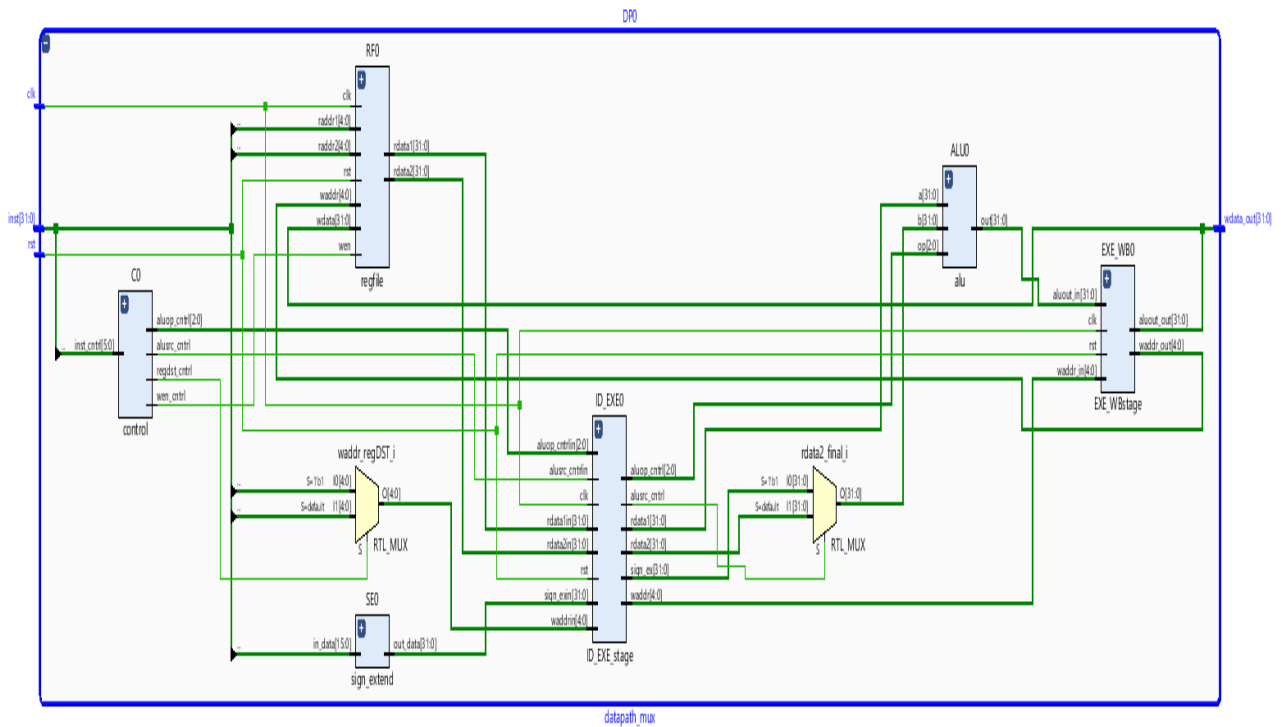
Simulation Waveform:



RTL Schematic:



RTL schematic for the datapath_mux:



Area (LUT, FF, Slice utilization):

| Site Type | Used | Fixed | Available | Util% |
|-----------------------|------|-------|-----------|-------|
| Slice LUTs* | 551 | 0 | 53200 | 1.04 |
| LUT as Logic | 551 | 0 | 53200 | 1.04 |
| LUT as Memory | 0 | 0 | 17400 | 0.00 |
| Slice Registers | 906 | 0 | 106400 | 0.85 |
| Register as Flip Flop | 906 | 0 | 106400 | 0.85 |
| Register as Latch | 0 | 0 | 106400 | 0.00 |
| F7 Muxes | 160 | 0 | 26600 | 0.60 |
| F8 Muxes | 0 | 0 | 13300 | 0.00 |

| | | | | | |
|---------------------------------------|---|------------|-------------------|--|--|
| Logic Levels | 10 (CARRY4=3 DSP48E1=2 FDRE=1 LUT2=1 LUT3=1 LUT4=1 MUXF7=1) | | | | |
| Data Path | | | | | |
| Delay Type | Inc... | Path (...) | Location | Netlist Resource(s) | |
| net (fo=138, routed) | 2.105 | 2.561 | | DP0/ID_EXE0/alusrc_cntrl | |
| net (fo=2, routed) | 1.329 | 10.612 | | DP0/ALU0/out0_1_n_103 | |
| net (fo=2, routed) | 1.274 | 14.076 | | DP0/EXE_WB0/aluout_out_reg[31]_1[24] | |
| net (fo=5, routed) | 1.227 | 3.912 | | DP0/ALU0/rdata2_final[15] | |
| net (fo=1, routed) | 0.815 | 12.289 | | DP0/ID_EXE0/aluout_out_reg[27][0] | |
| net (fo=1, routed) | 0.002 | 7.765 | | DP0/ALU0/out0_0_n_106 | |
| net (fo=1, routed) | 0.000 | 10.736 | | DP0/ALU0/i_carry_i_1_0_n_0 | |
| net (fo=1, routed) | 0.000 | 11.137 | | DP0/ALU0/out0_inferred_4/i_carry_n_0 | |
| net (fo=1, routed) | 0.000 | 11.251 | | DP0/ALU0/out0_inferred_4/i_carry_0_n_0 | |
| net (fo=1, routed) | 0.000 | 12.588 | | DP0/ID_EXE0/aluout_out[24]_i_3_n_0 | |
| DSP48E1 (Prop dsp... B[15] PCOUT[47]) | (r) 3.851 | 7.763 | Site: DSP48_X0Y2 | DP0/ALU0/out0_0/PCOUT[47] | |
| DSP48E1 (Prop dsp48e1 PCIN[47] PI[2]) | (r) 1.518 | 9.283 | Site: DSP48_X0Y3 | DP0/ALU0/out0_1/P[2] | |
| FDRE (Prop fdre C Q) | (r) 0.456 | 0.456 | Site: SLICE_X5Y4 | DP0/ID_EXE0/alusrc_cntrl_reg/Q | |
| CARRY4 (Prop carry4 S[3] CO[3]) | (r) 0.401 | 11.137 | Site: SLICE_X11Y9 | DP0/ALU0/out0_inferred_4/i_carry/CO[3] | |
| LUT4 (Prop lut4 I3 O) | (r) 0.299 | 12.588 | Site: S...X12Y11 | DP0/ID_EXE0/aluout_out[24]_i_3/O | |
| CARRY4 (Prop carry4 CI O[0]) | (r) 0.222 | 11.473 | Site: S...X11Y11 | DP0/ALU0/out0_inferred_4/i_carry_1/O[0] | |
| MUXF7 (Prop muxf7 I1 O) | (r) 0.214 | 12.802 | Site: S...X12Y11 | DP0/ID_EXE0/aluout_out_reg[24]_i_1/O | |
| LUT3 (Prop lut3 I2 O) | (r) 0.124 | 2.685 | Site: SLICE_X7Y8 | DP0/ID_EXE0/out0_i_2/O | |
| LUT2 (Prop lut2 I0 O) | (r) 0.124 | 10.736 | Site: SLICE_X11Y9 | DP0/ALU0/i_carry_i_1_0/O | |
| CARRY4 (Prop carry4 CI CO[3]) | (r) 0.114 | 11.251 | Site: S...X11Y10 | DP0/ALU0/out0_inferred_4/i_carry_0/CO[3] | |
| FDRE | (r) 0.000 | 0.000 | Site: SLICE_X5Y4 | DP0/ID_EXE0/alusrc_cntrl_reg/C | |
| | | | Site: SLICE_X7Y8 | DP0/ID_EXE0/out0_i_2/I2 | |
| | | | Site: DSP48_X0Y2 | DP0/ALU0/out0_0/B[15] | |

No. of LUTs used: 551

No. of registers as FF used: 906

Slice Utilization: 1.04(for LUTs), 0.85(for registers)

Maximum operating Frequency: 0.2596 (ns)⁻¹

The delay for four staged pipeline is relatively less compared to that of three staged pipeline.