TASK -3

Design a chain of two input NAND gates for a minimum delay.

Objectives:

1. **To find input capacitance of two input NAND gate.**
2. **Finding delay of stages of NAND gates using linear delay model.**
3. **Finding optimum number of stages for less delay through linear delay model.**

Software Used: Cadence Virtuoso

Experimental Procedure:

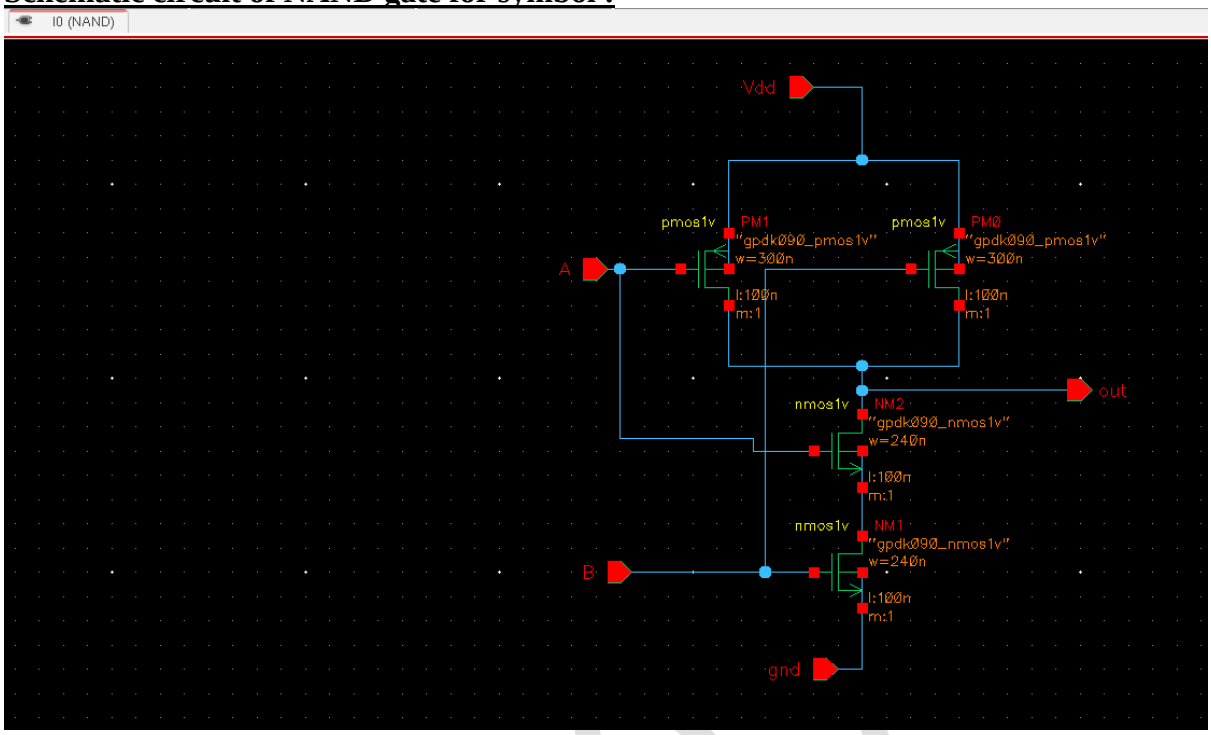
Part a) To find input capacitance of NAND gate.

1. Create a symbol for two input NAND gate.
2. To find the input capacitance of the of the NAND gate , invoke the symbol you have created and connect a piece wise linear source to inputs of NAND gate and perform transient analysis..
3. Plot the input voltage(net) and input current(node).
4. Integrate the output plot i.e current plot from 0ns to time period the wave(10ns).
5. Find input capacitance using the formulae $C_{in} = \frac{\int i\,dt}{v_C(t)}$.
6. Find load capacitance = 64x(Cin).

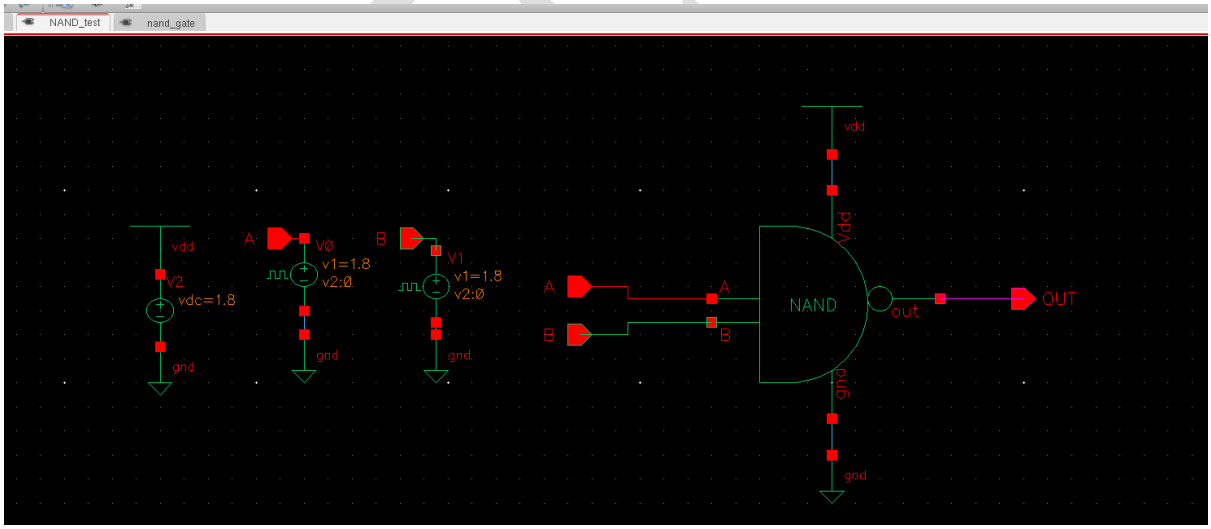
Part b) To find number of stage of chain of nand gates that gives less delay.

1. Create a chain of NAND gates i.e 1 stage, 2 stage, 3 stage, 4 stage with load capacitance calculated in above part.
2. Do Sizing of pull up network and pull down network accordingly.
3. Find delay between input and output and check which stage has less delay.

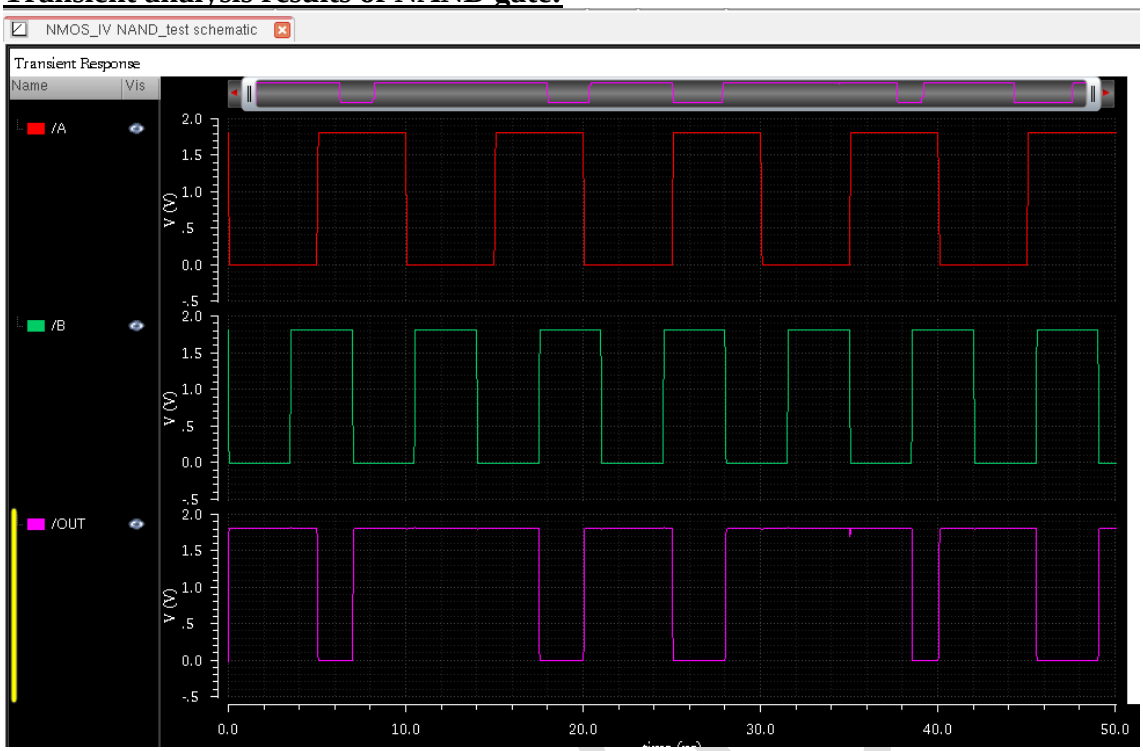
Schematic circuit of NAND gate for symbol :



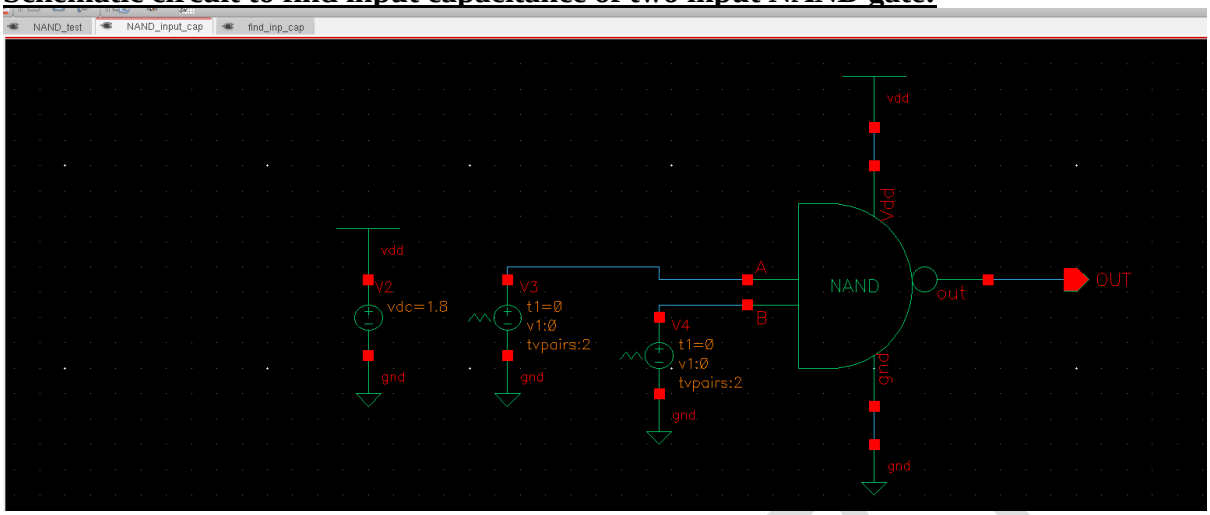
Schematic circuit to test the NAND gate:



Transient analysis results of NAND gate:

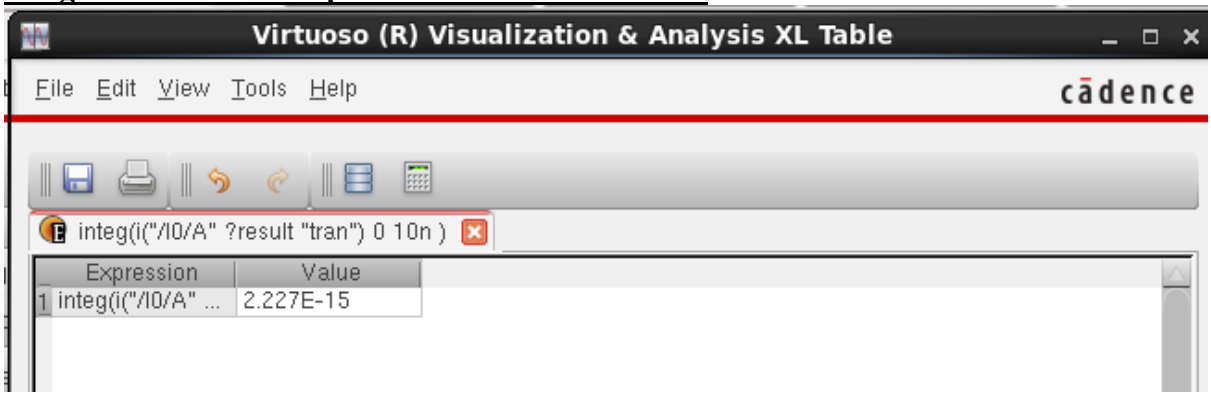


Schematic circuit to find input capacitance of two input NAND gate:

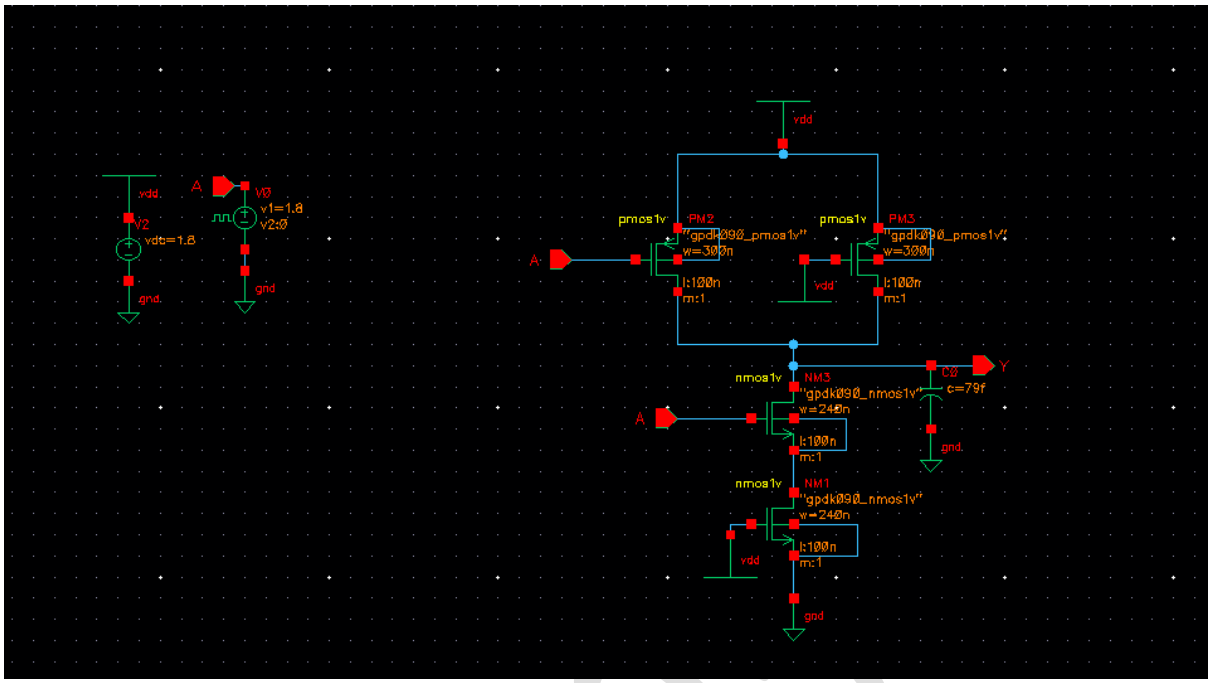


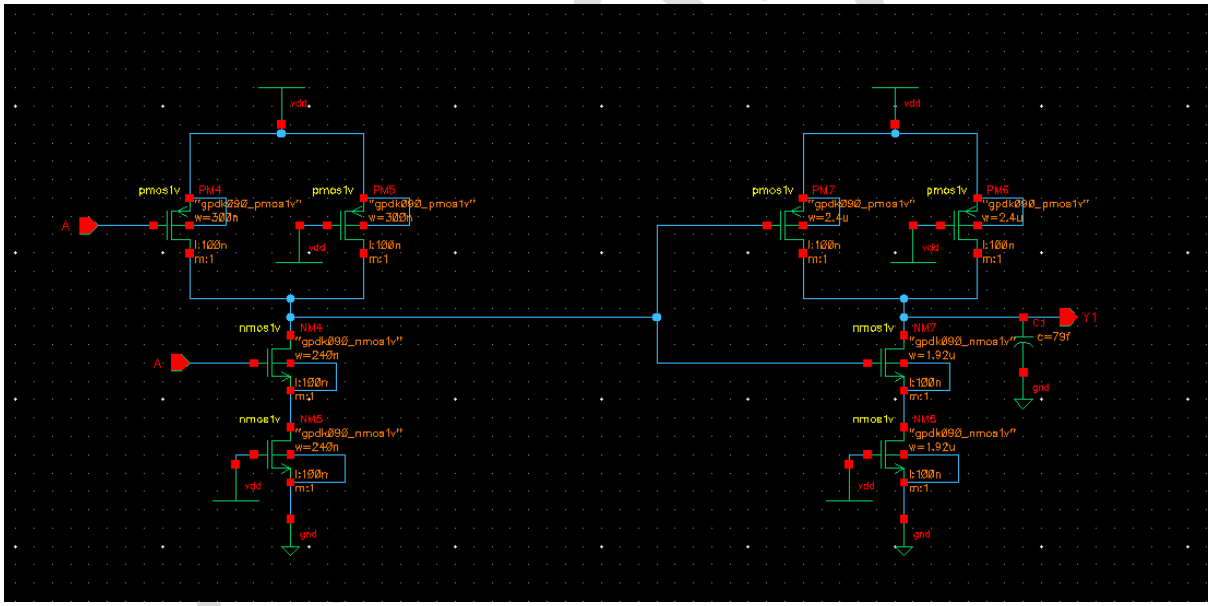
Output plot of input current vs input voltage:

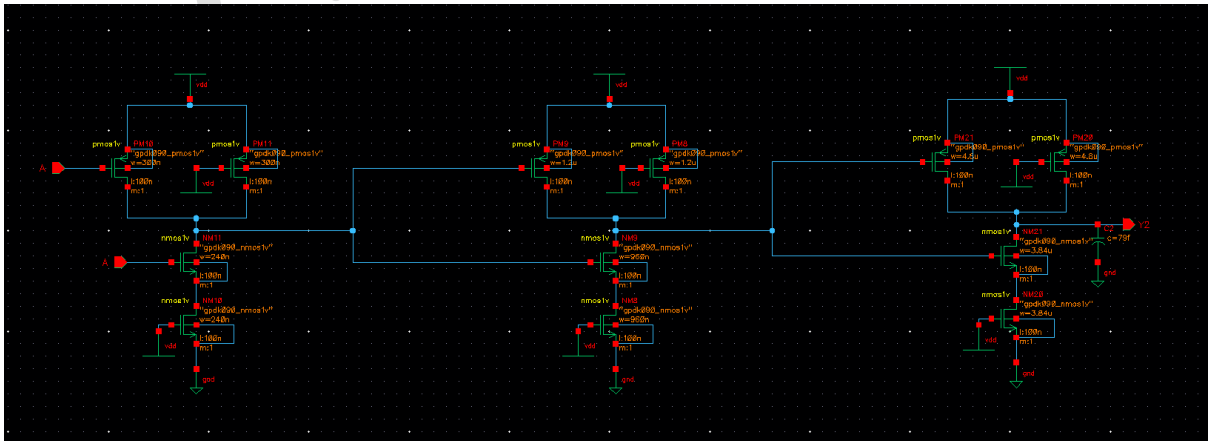
Integration results of input current from 0 to 10ns:

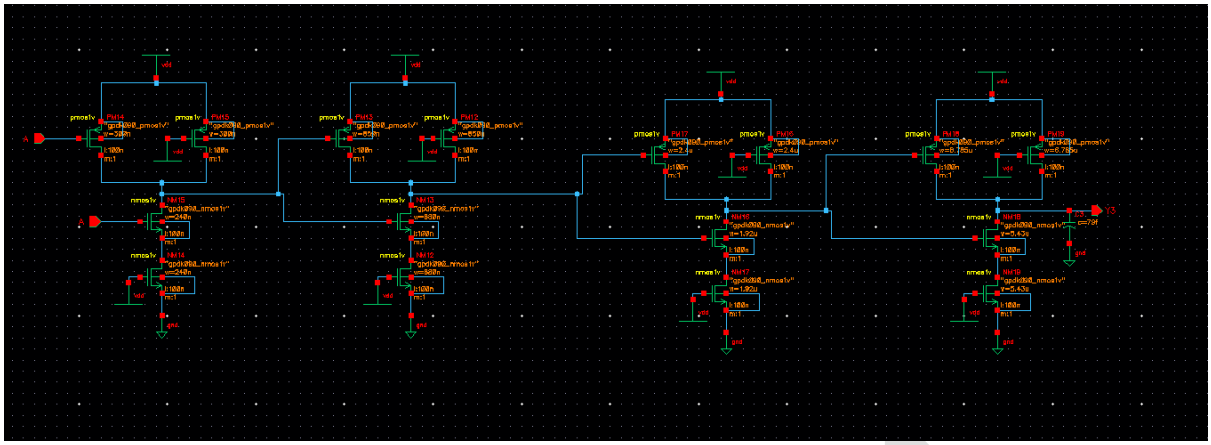


Schematics of chain of NAND gates with B input as VDD.

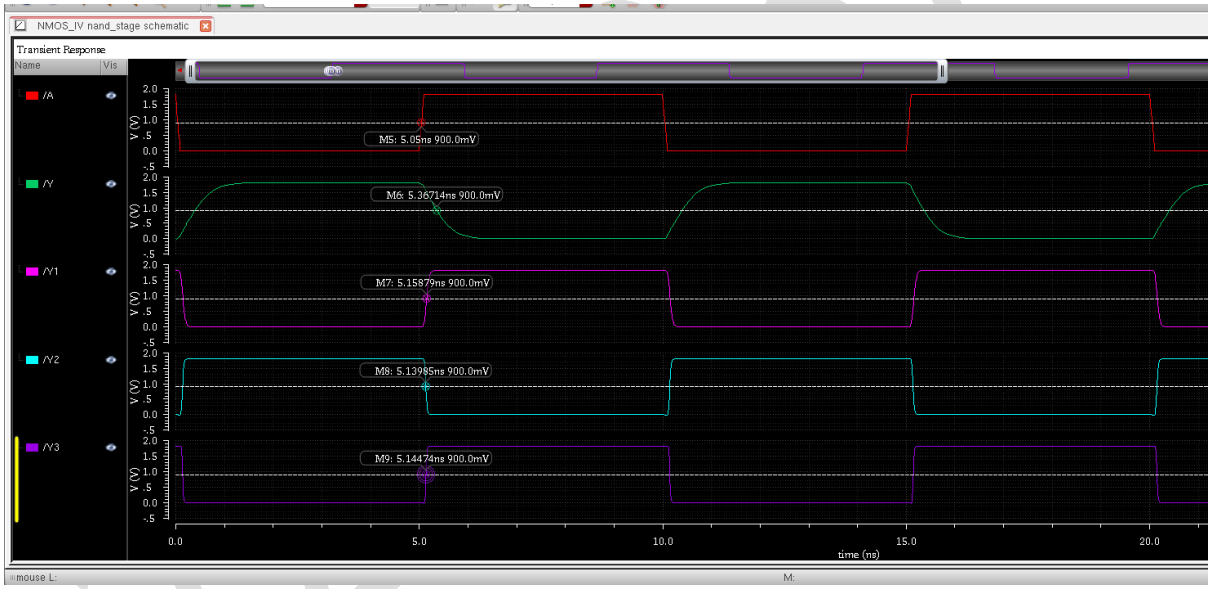




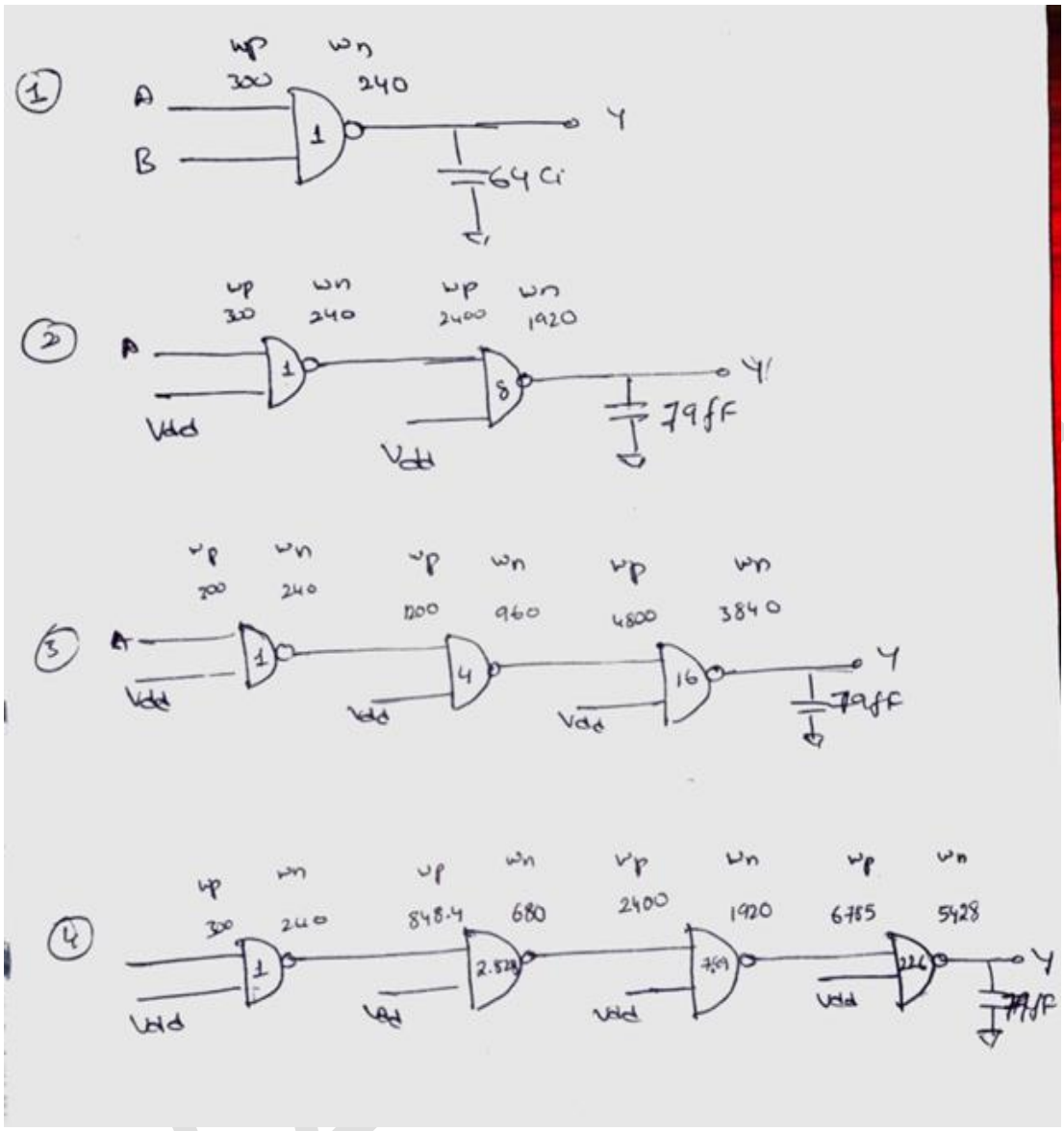




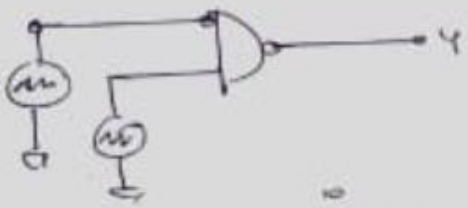
Output of all stages.



Theoretical Calculations:



To find input capacitance :-



$$C_{in} = \frac{\int_0^{10} i\,dt}{V(t)} = \frac{2.227\times10^{-15}}{1.8} = 1.237\,fF$$

$$C_{out} = 64 \times 1.237\,fF$$

$$= 79.168\,fF \approx 79\,fF$$

1. $D = nf+1p$ $\quad F = \frac{4}{5}\times64$

$= 85.33+2$ $\quad = 85.33$

$= 87.33$

2. $D = 2(10.66)+4$ $\quad F = \left(\frac{4}{3}\right)^2\times64$

$= 25.32$ $\quad = 113.77$

3. $D = 3(3.33+6$ $\quad F = \left(\frac{4}{3}\right)^3\times64$

$= 22.22$ $\quad = 151.7$

4. $D = 4\times(3.77)+8$ $\quad F = \left(\frac{4}{3}\right)^4\times64$

$= 23.08$ $\quad = 202.27$

Results and Analysis:

1. Input capacitance has been calculated and Cin=1.237fF.
2. Load capacitance has been calculated and Cload=79fF.
3. Symbol of NAND gate has been tested and working properly.

4. Finding delays in Stages:

No of Stages	Output Signal	T(L-H) in ns	T(H-L) in ns	Tpdr (ns)	Tpdf (ns)	Tpd avg= (Tpdr+tpdf)/2
	A	5.05	10.05			
1	Y1	5.3671	10.3963	0.3171	0.3463	0.3317
2	Y2	5.15879	10.155	0.10877	0.105	0.106885
3	Y3	5.13985	10.1471	0.08985	0.0971	0.093475
4	Y4	5.14479	10.1471	0.09474	0.09771	0.096225

From the above calculations we can clearly observe that three stages gives the minimum delay which matches theoretically.