Experiment -5

To create a layout of a CMOS inverter and perform the post layout simulations.

Objectives:

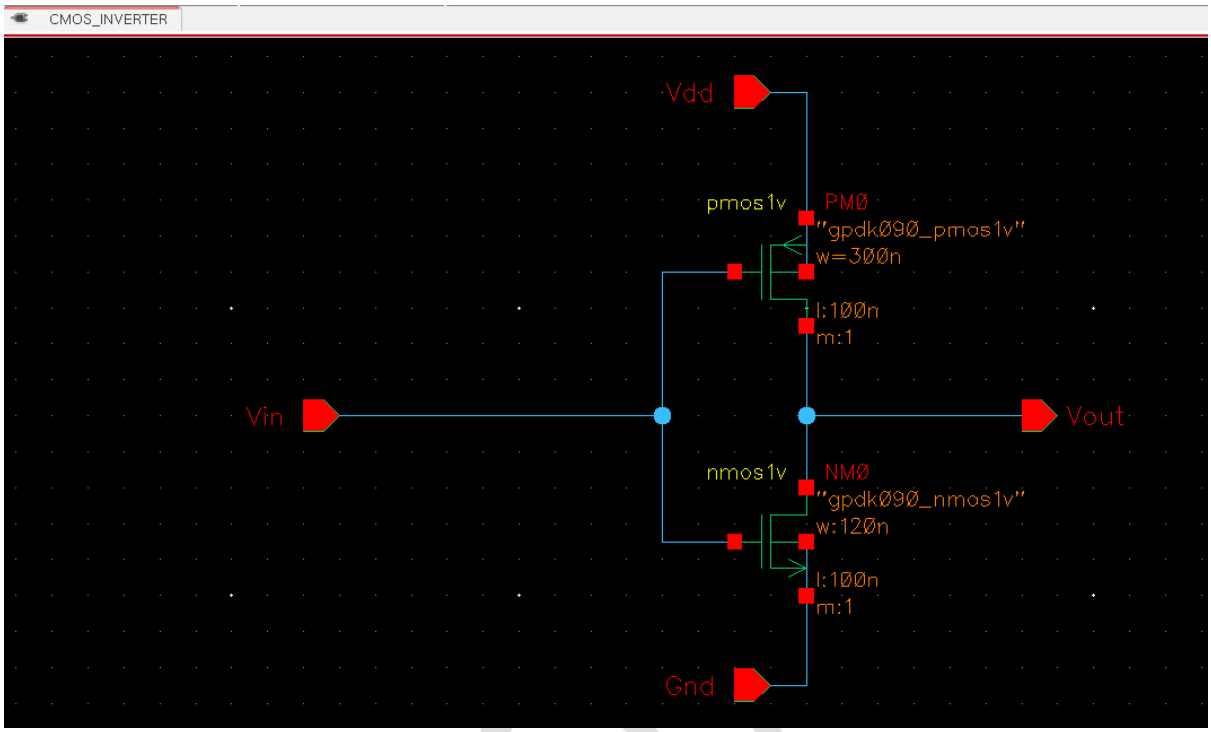
1. **To Create a layout of inverter and perform Pre-layout and Post-layout simulation.**
2. **Analyze the propagation delay of schematic and layout.**

Software Used: Cadence Virtuoso

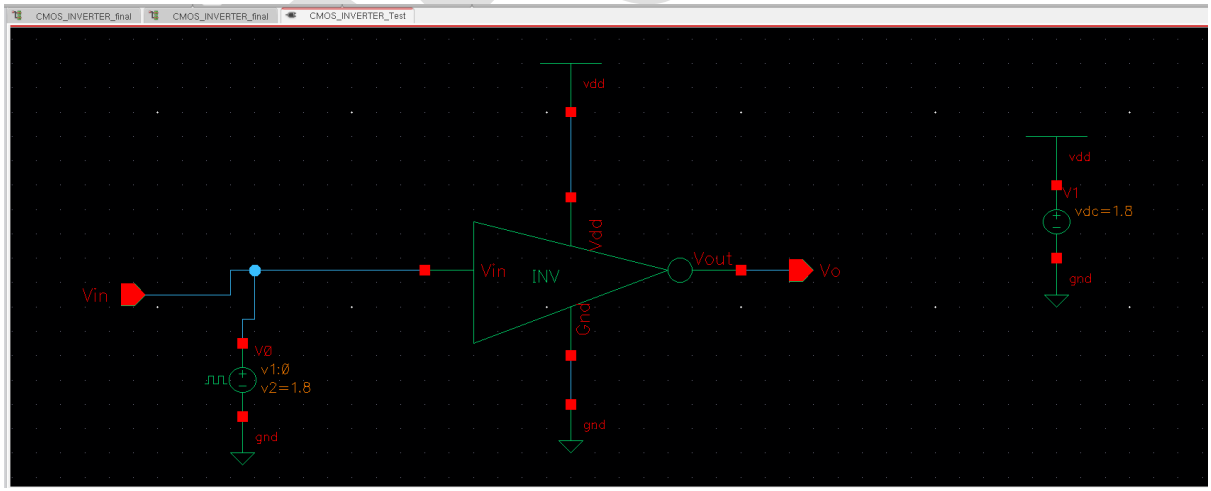
Experimental Procedure:

1. Create a schematic of CMOS Inverter gate.
2. Create a testbench of it and verify its functionality by create a symbol.
3. Create a layout of CMOS Inverter and perform
   d. Design Rule Check (DRC)
   e. Layout Vs Schematic(LVS)
   f. RC extraction.
4. Create a configuration file with same of the schematic of CMOS Inverter _TEST that you have created for verifying functionality of schematic.
5. Perform Transient analysis of AV Extracted View of layout from configuration window.
6. Compare propagation delays of Schematic and Layout and analyze the results.

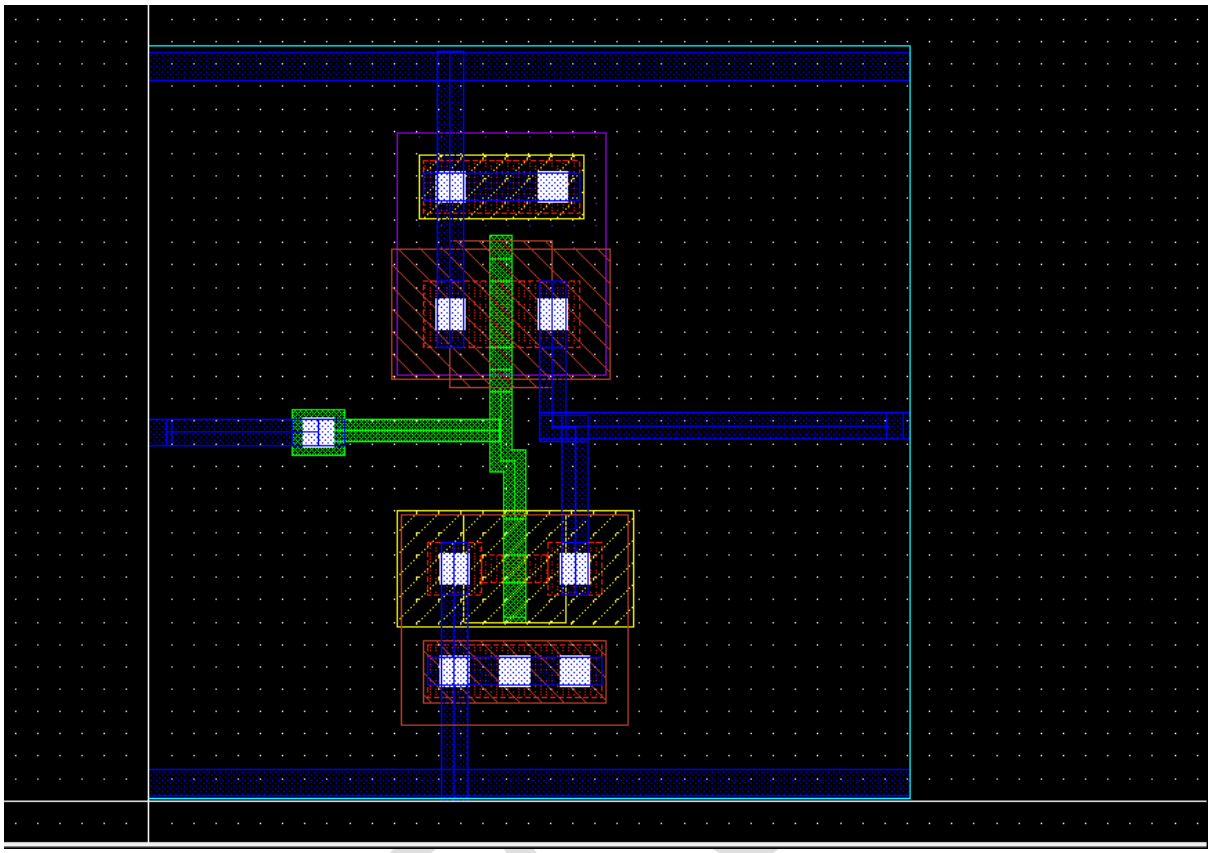
Schematic circuit of CMOS Inverter for symbol :



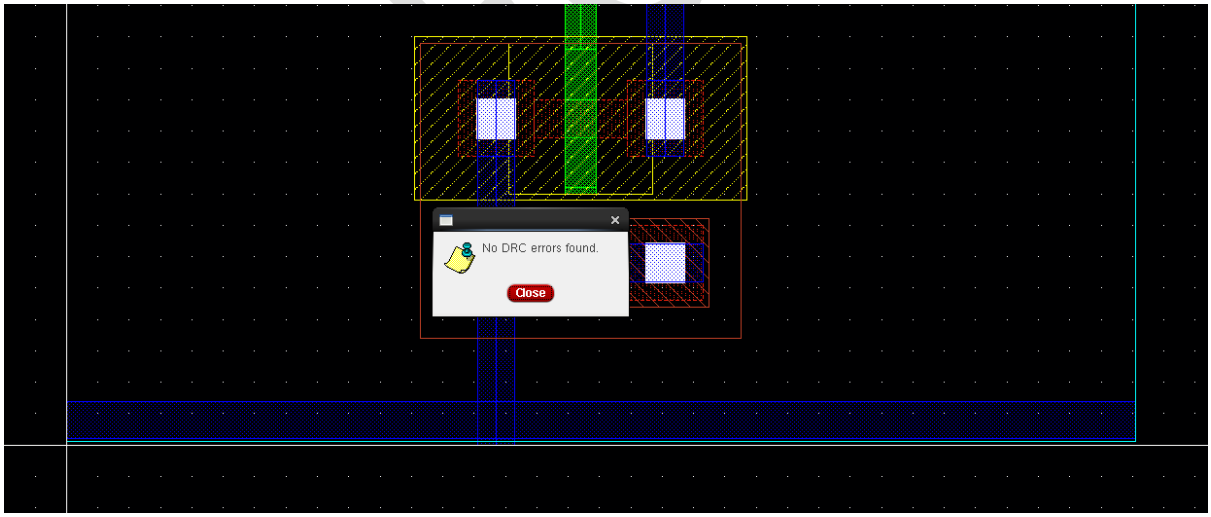
Schematic circuit to test the CMOS Inverter gate:



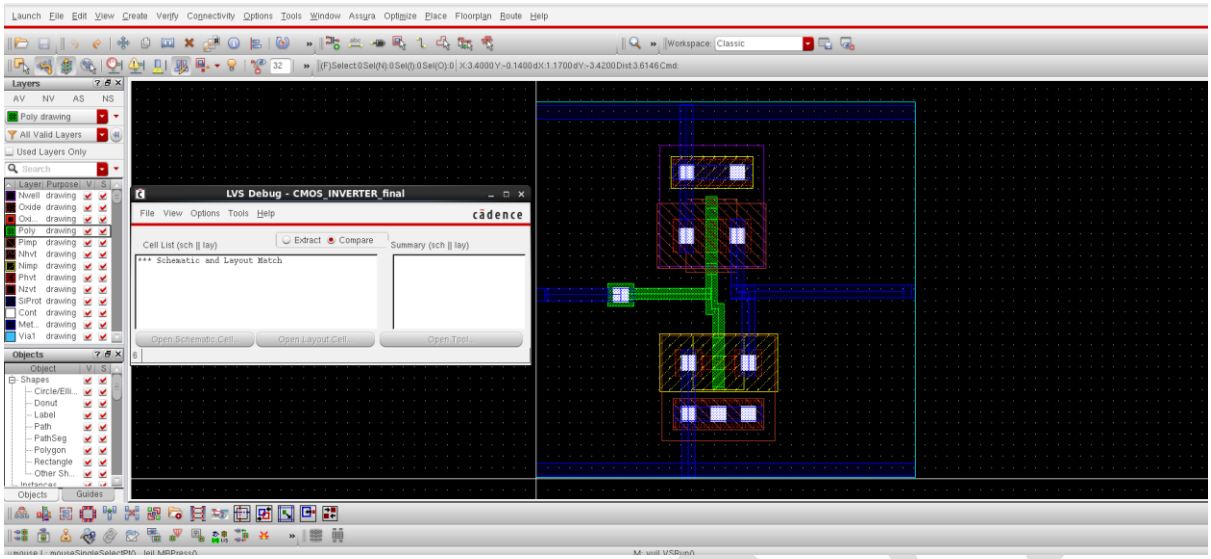
Layout of CMOS Inverter:



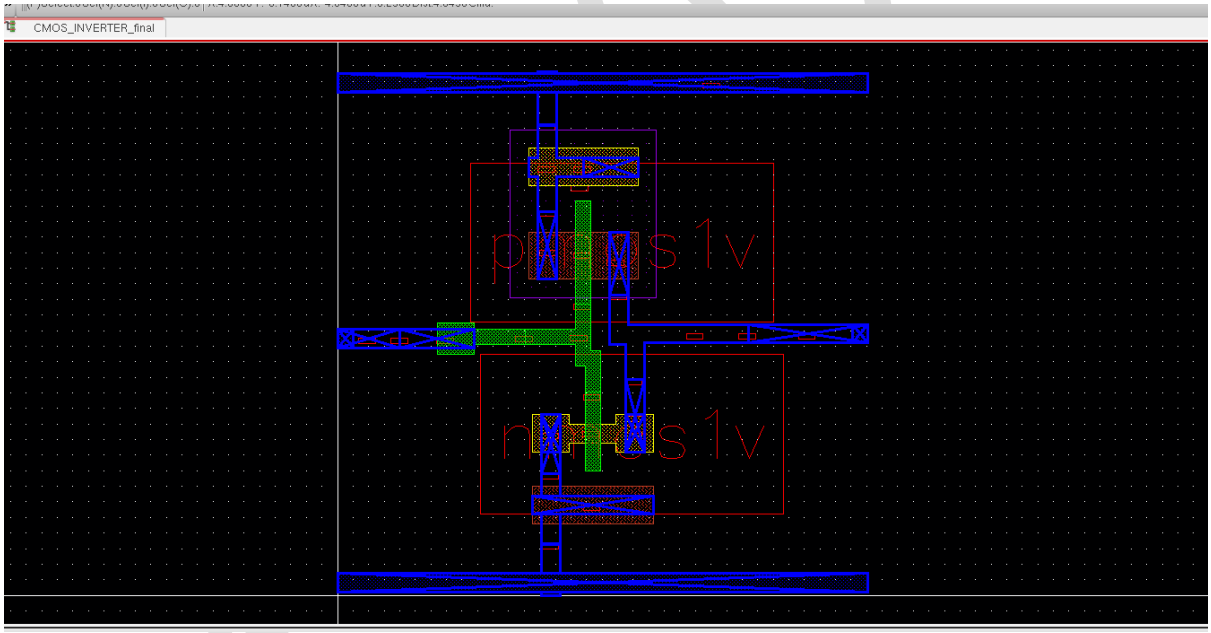
Design Rule Check for created layout:



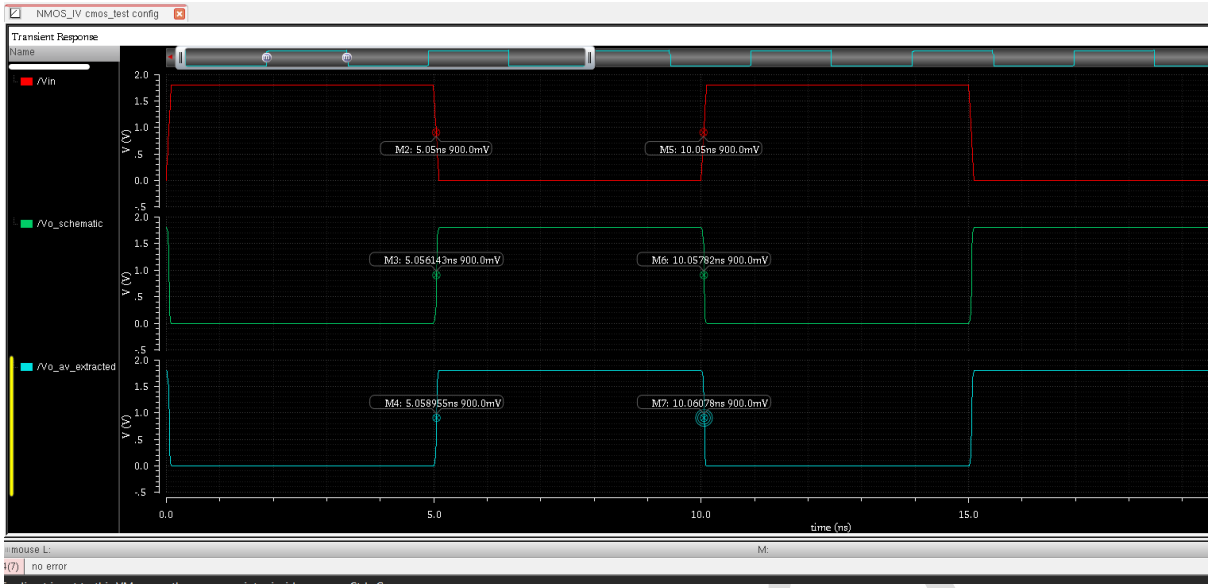
Layout Vs Schematic Check:



AV- Extracted view:



Output graph of Pre-layout and Post-layout simulation:



Results and Analysis:

Finding Propagation delay:

Output Signal	T(L-H)	T(H-L)	Tpdr	Tpdf	Tpd avg= (Tpdr+Tpdf)/2
A	10.05 ns	5.05 ns			
Output of Schematic	10.05782 ns	5.056143 ns	7.82 (ps)	6.143 (ps)	6.9815 ps
Output of Layout	10.06078 ns	5.058955 ns	10.78 (ps)	8.955 (ps)	9.8675 ps

From the above calculations, we can clearly observe that the delay in the post-layout simulation of the inverter gate is greater than the delay in the pre-layout simulation.

Analysis:

In the post-layout (AV extracted) view, additional internal parasitics, such as resistance and capacitance, are introduced. These parasitics contribute to increased delay as they affect signal propagation through the layout.

******* **THANK YOU*******