TASK -5

To create a layout of a 2 input CMOS NAND Gate and perform the post layout simulations.

Objectives:

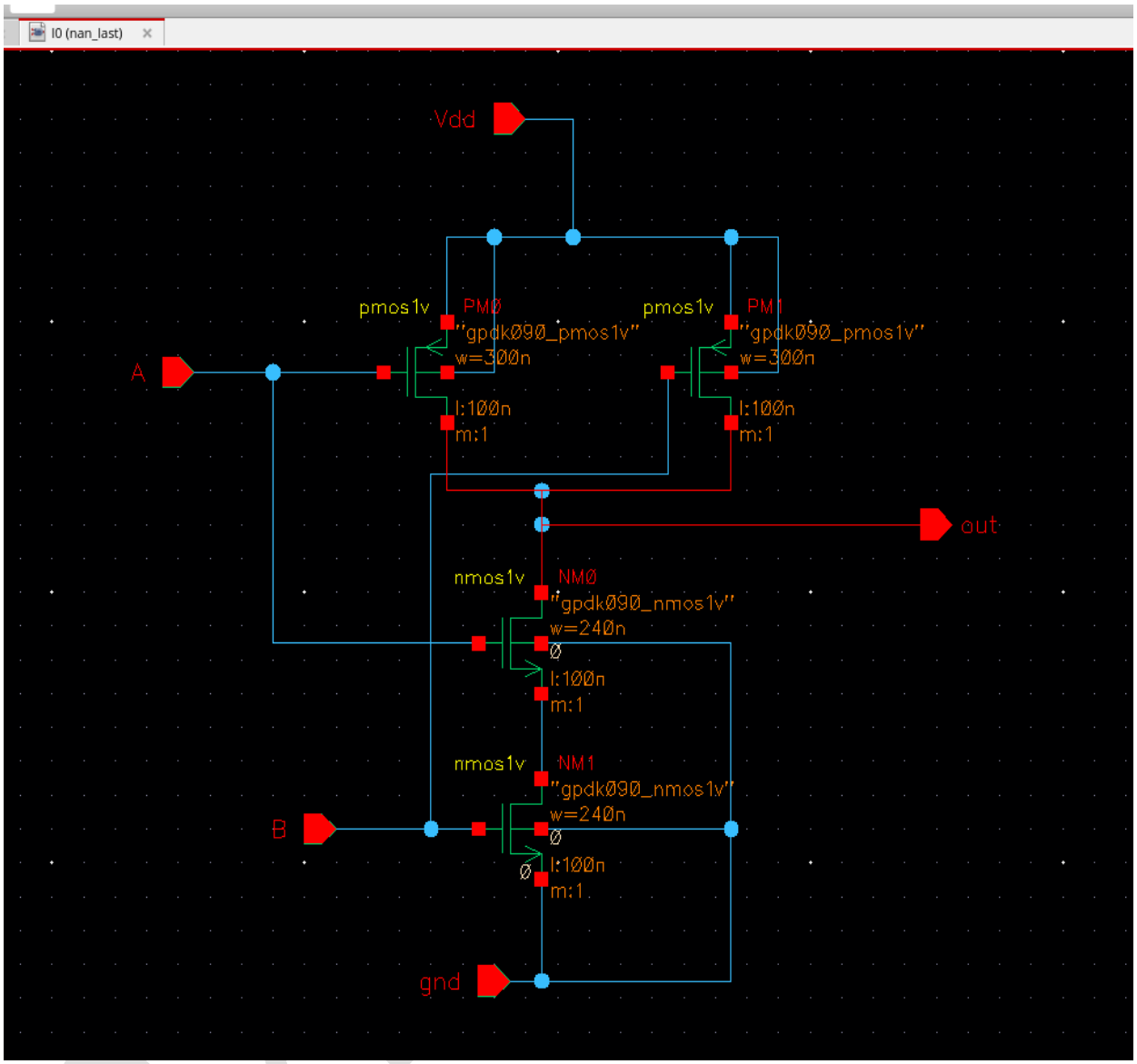
1. **To Create a layout of two input Nand Gate and perform Pre-layout and Post-layout simulation.**
2. **Analyze the propagation delay of schematic and layout.**

Software Used: Cadence Virtuoso

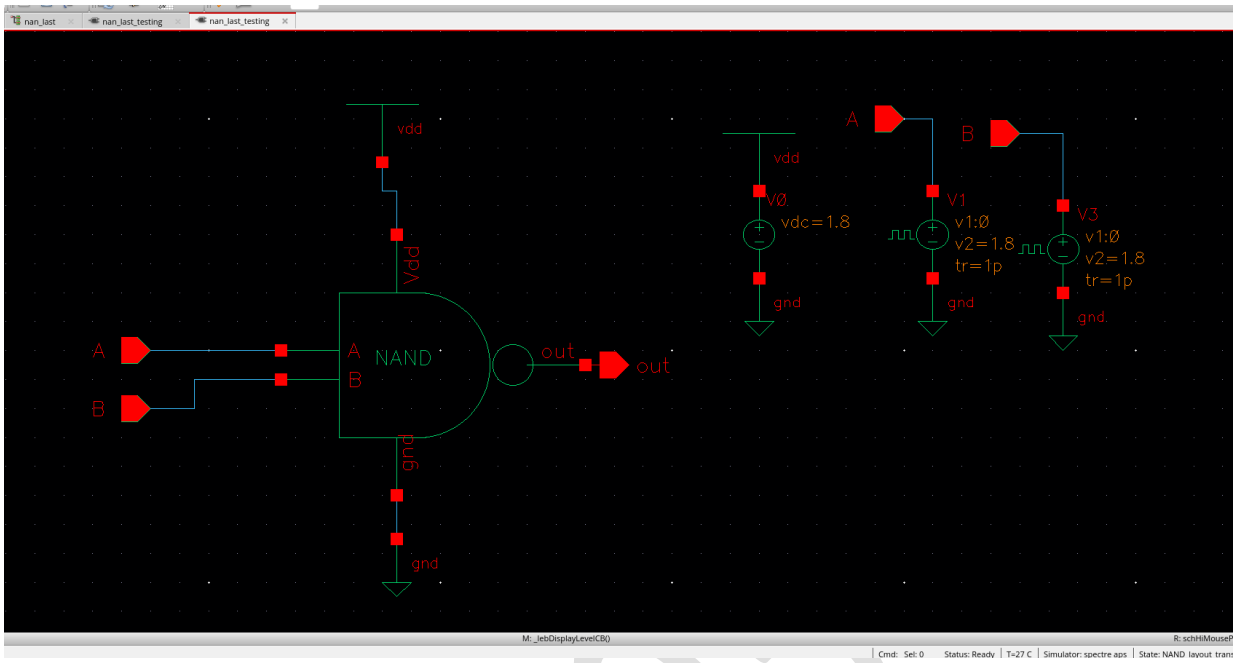
Experimental Procedure:

1. Create a schematic of two input NAND gate.
2. Create a testbench of it and verify its functionality by create a symbol.
3. Create a layout of NAND gate and perform
   a. Design Rule Check (DRC)
   b. Layout Vs Schematic(LVS)
   c. RC extraction.
4. Create a configuration file with same of the schematic of NAND_TEST that you have created for verifying functionality of schematic.
5. Perform Transient analysis of AV Extracted View of layout from configuration window.
6. Compare propagation delays of Schematic and Layout and analyze the results.

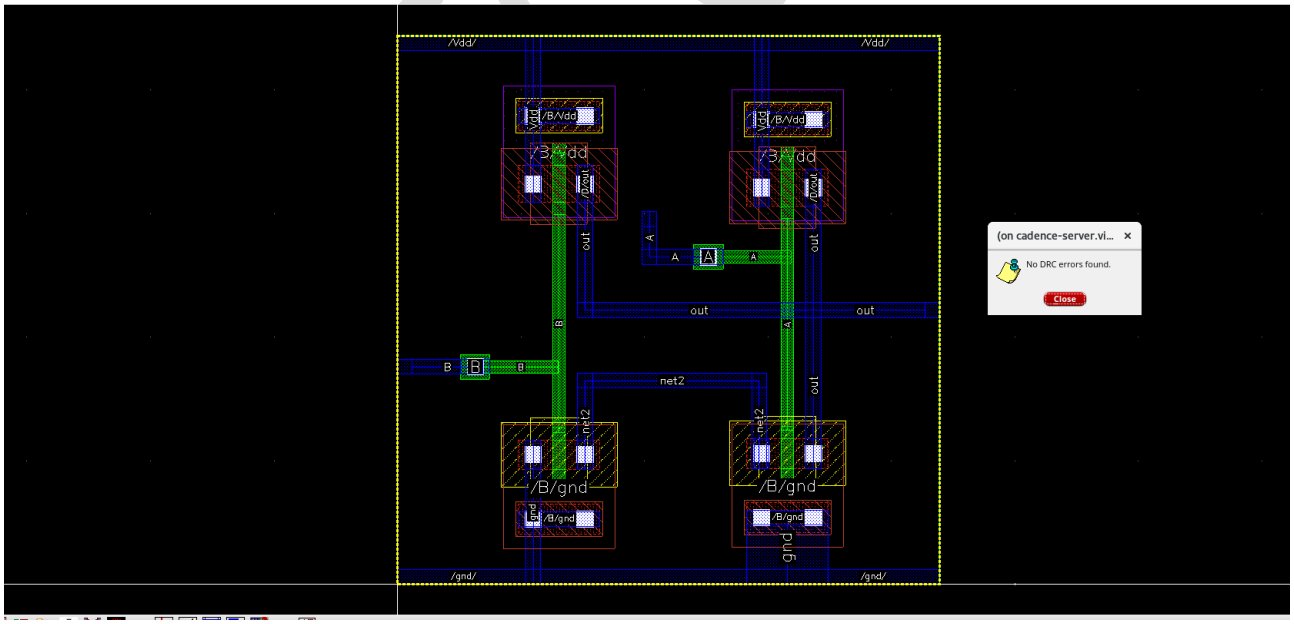
Schematic circuit of NAND gate for symbol :



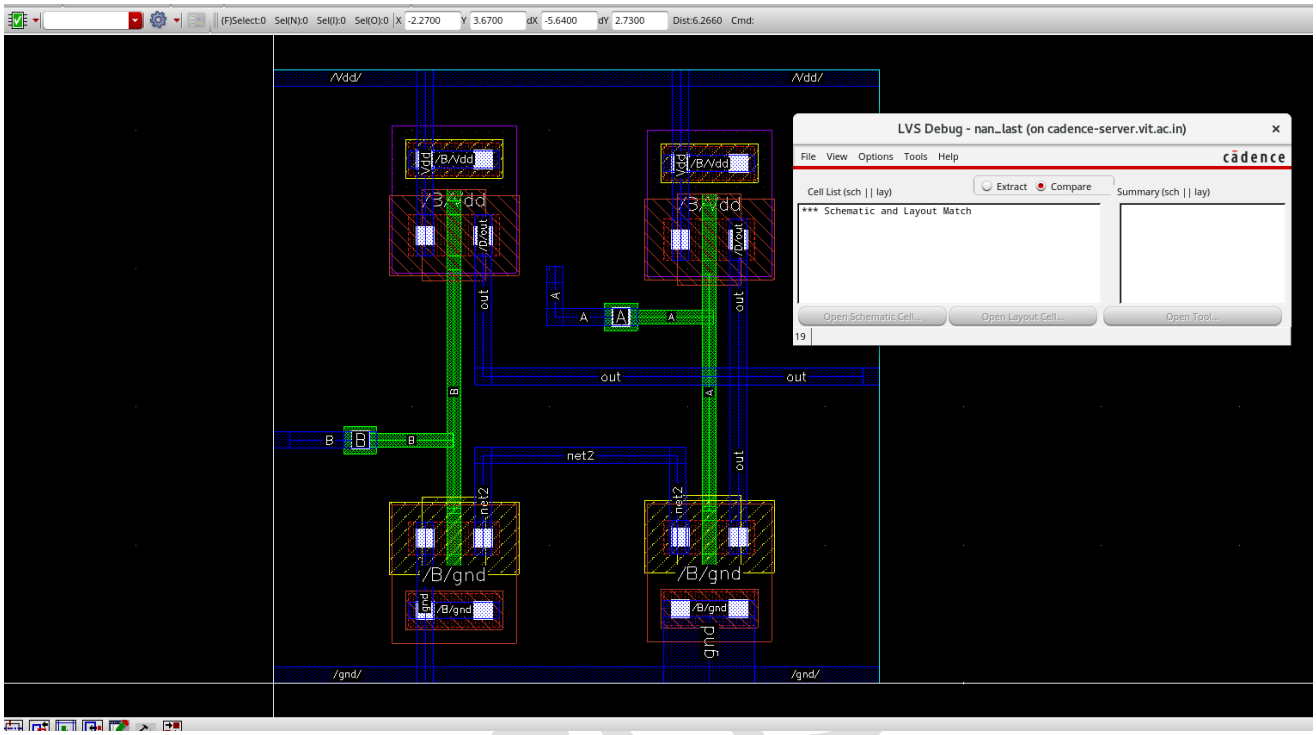
Schematic circuit to test the NAND gate:



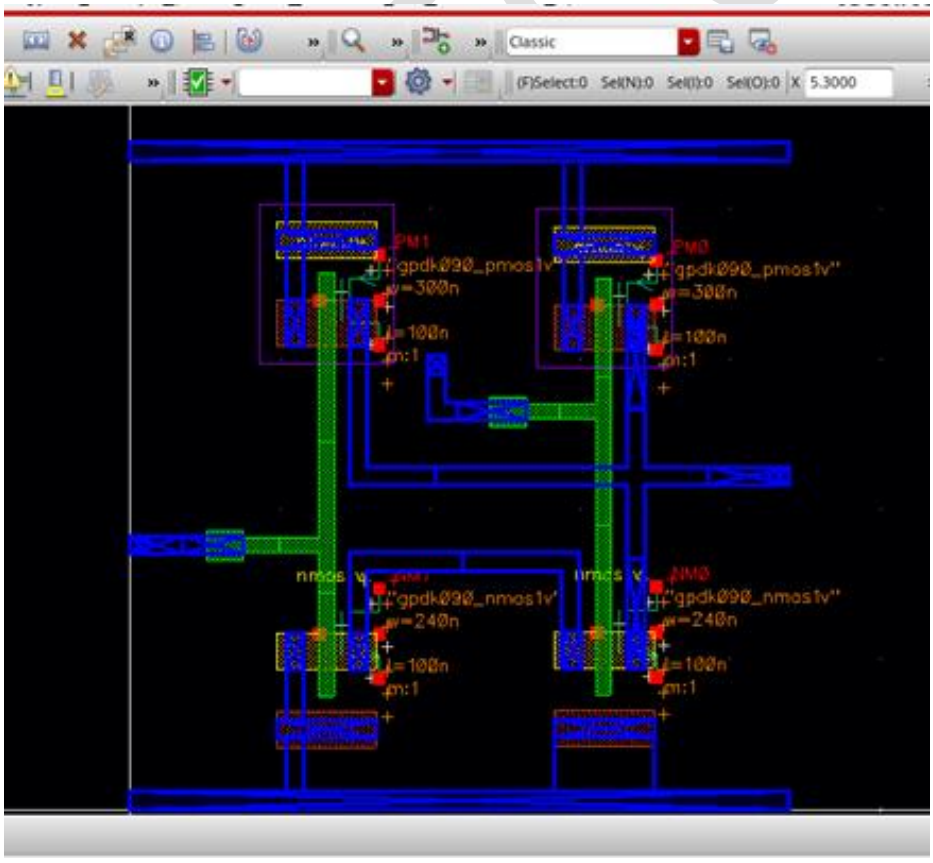
Design Rule Check for created layout:



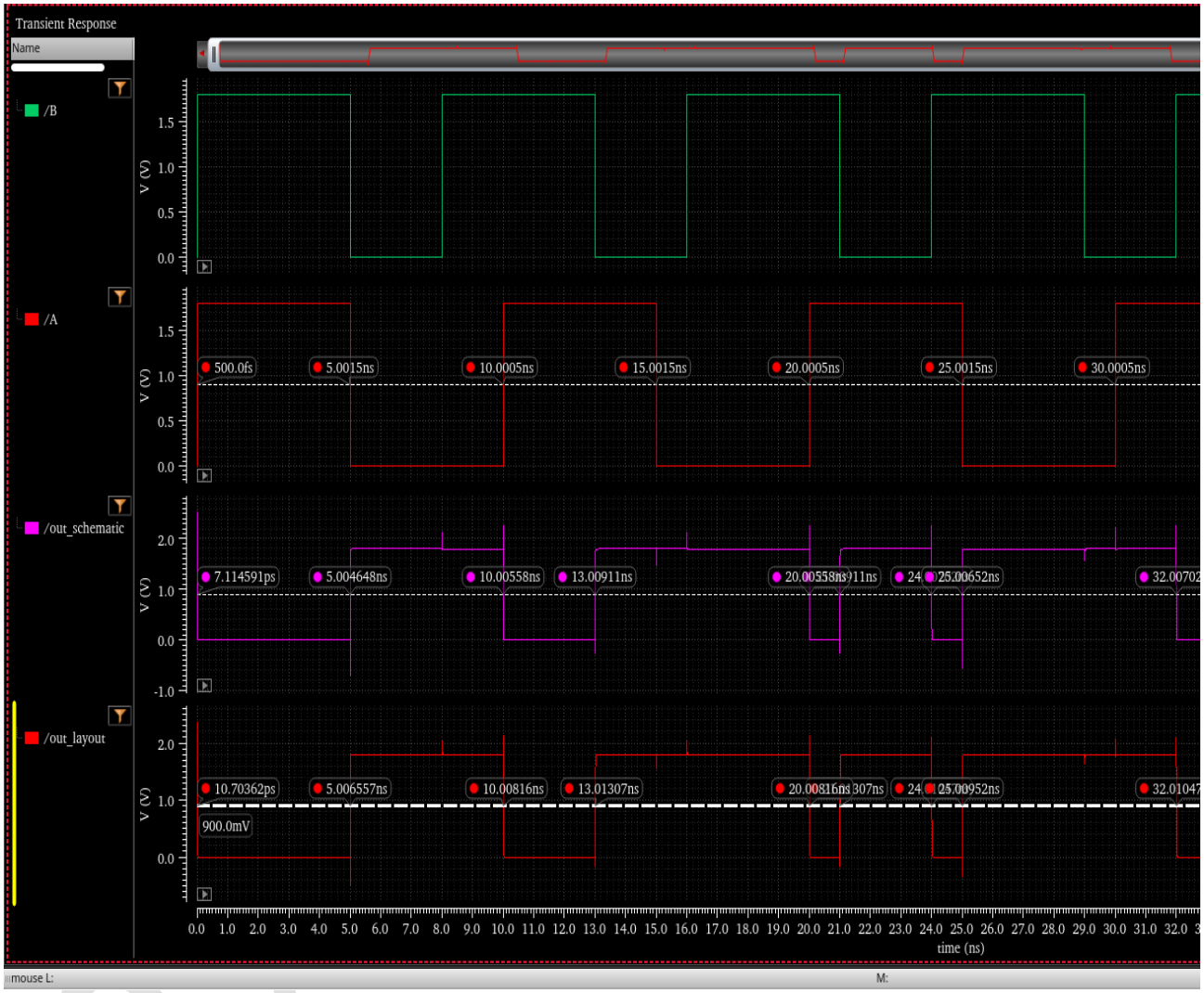
Layout Vs Schematic Check:



AV- Extracted view:



Output graph of Pre-layout and Post-layout simulation:



Results and Analysis:

1. Finding Propagation delay:

Output Signal	T(L-H)	T(H-L)	Tpdr	Tpdf	Tpd avg= (Tpdr+Tpdf)/2
A	5.0015ns	10.0005 ns			
Output of Schematic	5.004648	10.00558	3.148ps	5.08ps	4.114ps
Output of Layout	5.006557	10.00816	5.057ps	7.66ps	6.3585ps

From the above calculations, we can clearly observe that the delay in the post-layout simulation of the NAND gate is greater than the delay in the pre-layout simulation.

Analysis:

In the post-layout (AV extracted) view, additional internal parasitics, such as resistance and capacitance, are introduced. These parasitics contribute to increased delay as they affect signal propagation through the layout.