Experiment -2
Design and Analysis of 2 input NAND Gate

Objectives:

1. To do DC analysis of NAND Gate.
2. Do Transient analysis of NAND Gate with different input combinations and prove that delay is input dependent.

Experimental Procedure:

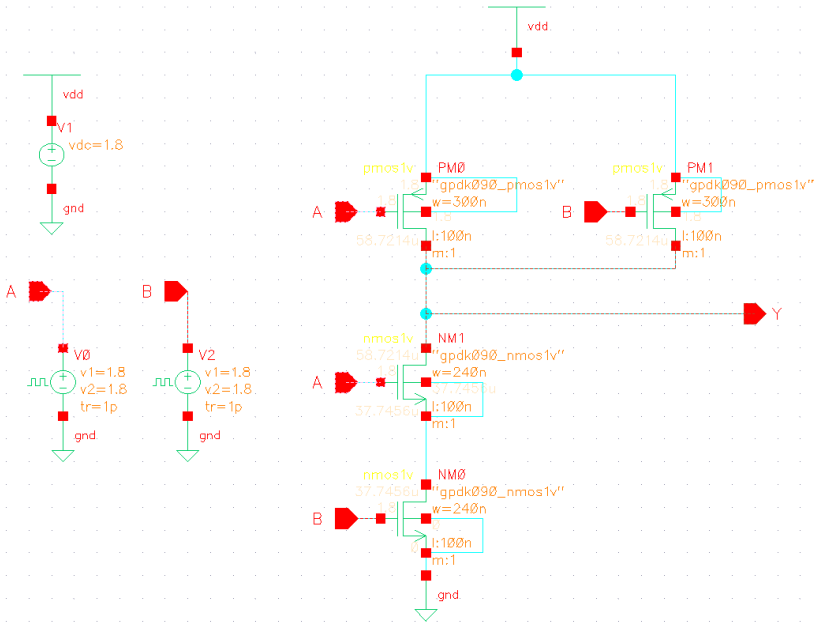
1. Invoke Cadence Virtuoso tool

2. Construct the schematic as shown in Fig.

3. Invoke ADEL and perform DC analysis to plot VTC curve for different input transitions

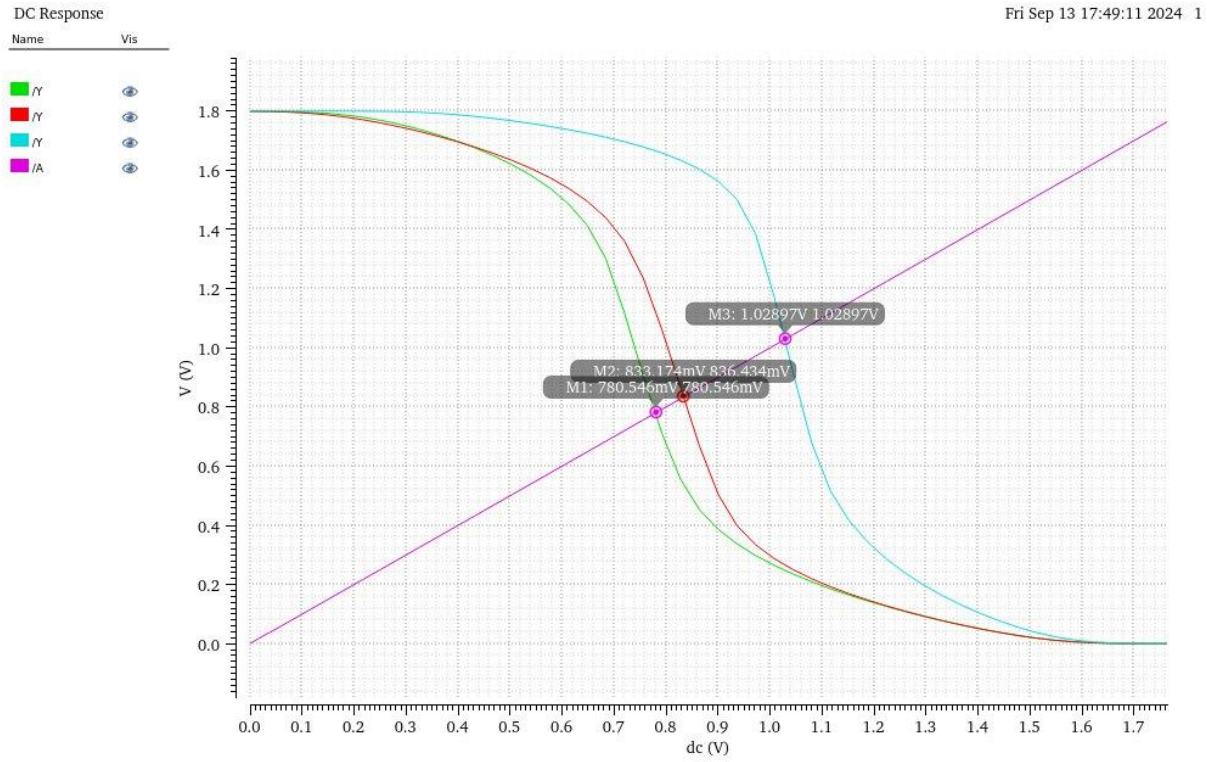
4. Perform Transient analysis and calculate the propagation delays for different input transitions shown in tabulation section.

Schematic Circuit of NAND gate:



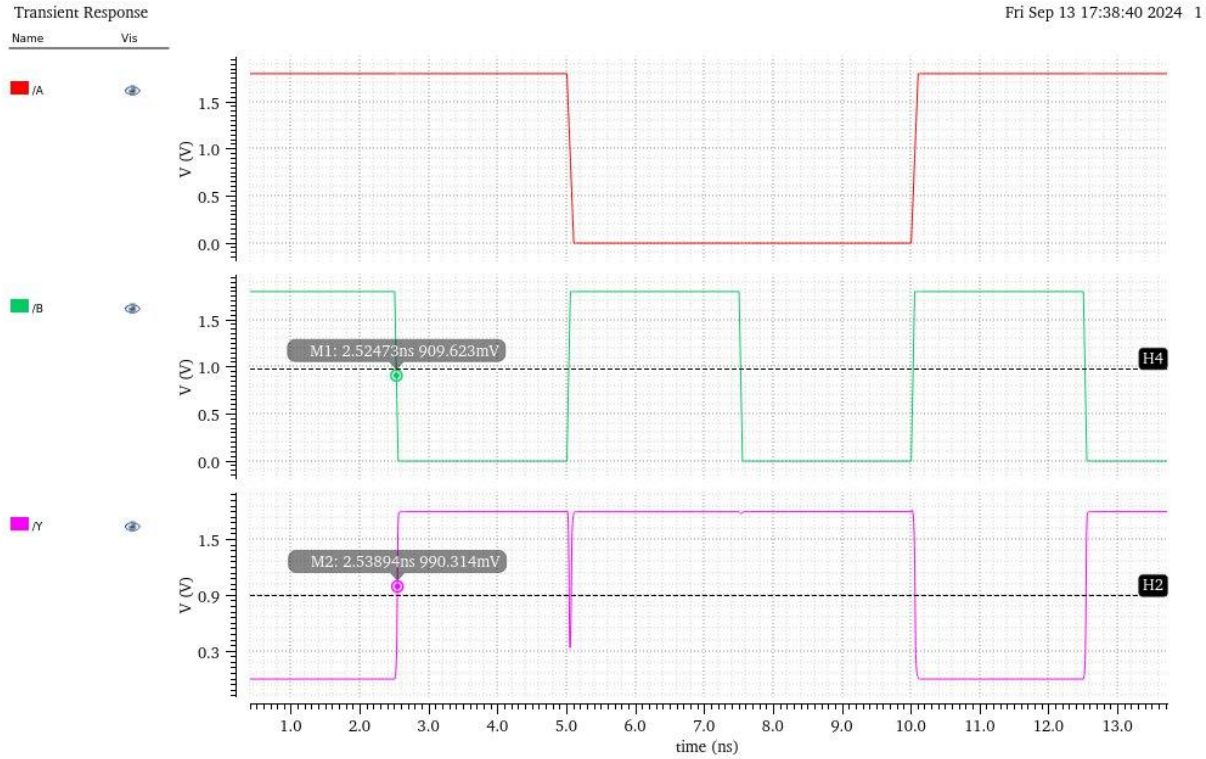
Results and Analysis:

1. DC analysis and finding Threshold point for inputs A,B.



Green Curve represents output Y and component parameter B and Threshold Point is 781.027 mV .
Red Curve represents output Y and component parameter A and Threshold Point is 832.7801 mV.
Blue Curve represents output Y and short both inputs A,B and Threshold Point is 1.0289V.

2. Finding Delays with Transient response:



Analysing Delays.

Input A	Input B	Output Y	Delay
1	1 to 0 2.525ns	0 to 1 Tplh = 2.53795ns	Td =12.94ps
1	0 to 1 3.015ns	1 to 0 Tphl = 3.021ns	Td= 6ps
0 to 1 3.015ns	1	1 to 0 Tphl = 3.021ns	Td= 6ps
1 to 0 2.525ns	1	0 to 1 Tplh = 2.535 ns	Td =10ps
0 to 1	0 to 1 10.05 ns	1 to 0 Tphl = 10.06691ns	Td= 16.9ps
1 to 0	1 to 0 10.05ns	0 to 1 Tplh = 10.049676ns	Td= 0.324ps

TASK -1
Design and Analysis of 2 input NOR Gate

Objectives:

1. To do DC analysis of NOR Gate.
2. Do Transient analysis of NOR Gate with different input combinations and prove that delay is input dependent.

Experimental Procedure:

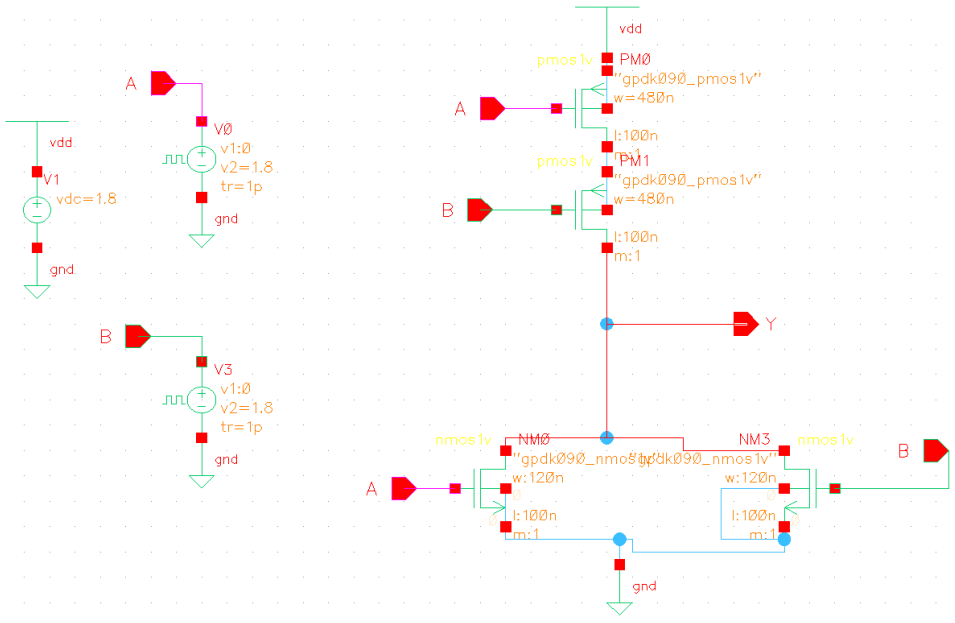
1. Invoke Cadence Virtuoso tool

2. Construct the schematic as shown in Fig.

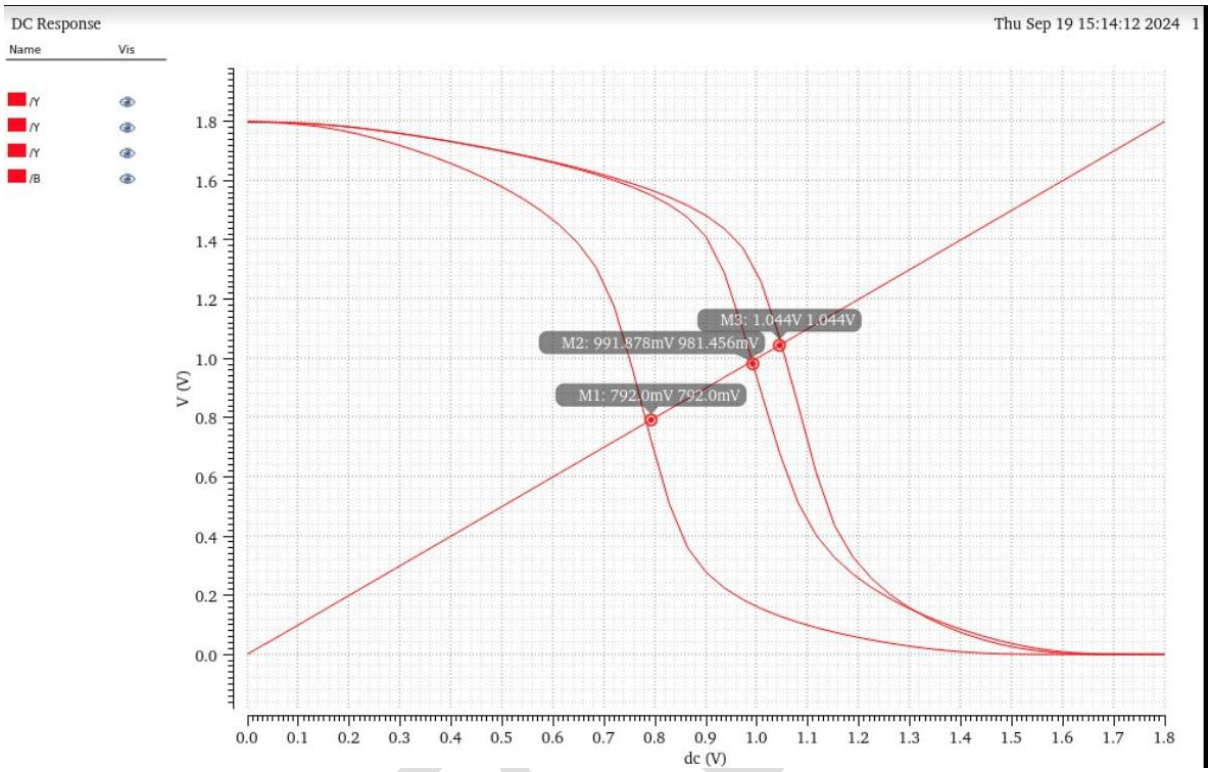
3. Invoke ADEL and perform DC analysis to plot VTC curve for different input transitions

4. Perform Transient analysis and calculate the propagation delays for different input transitions shown in tabulation section.

Schematic Circuit of NOR gate:

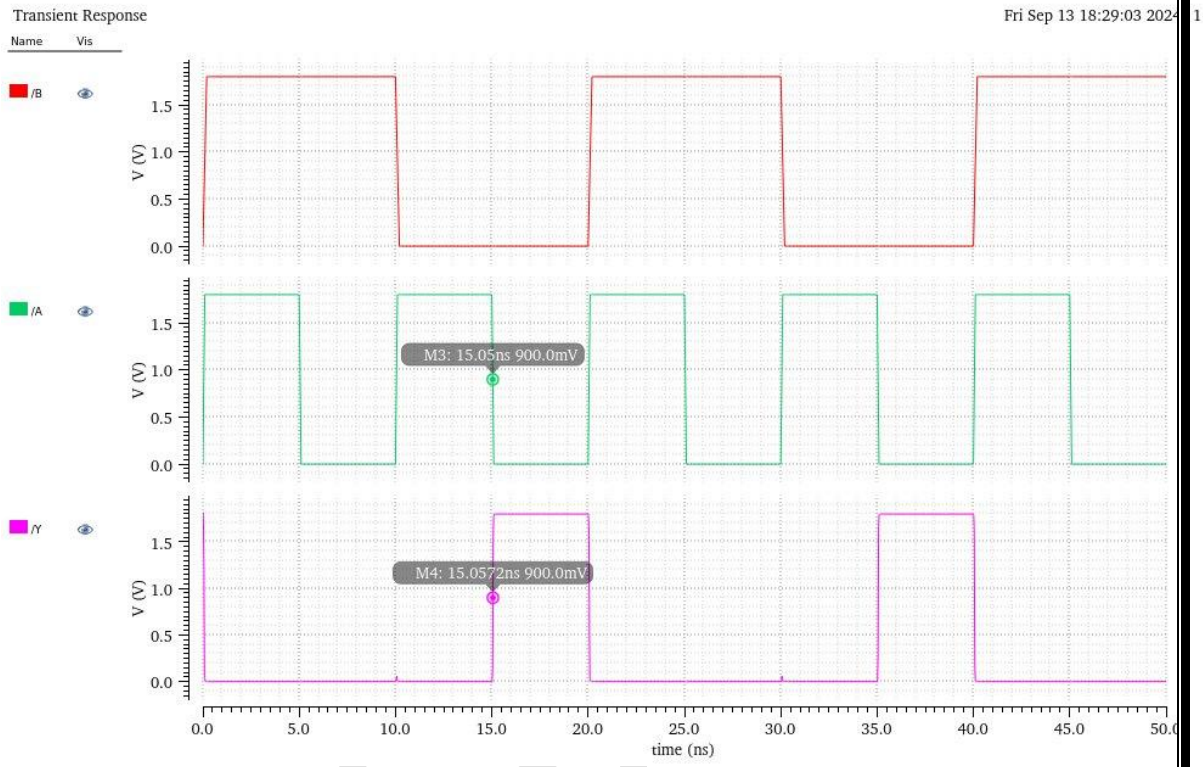


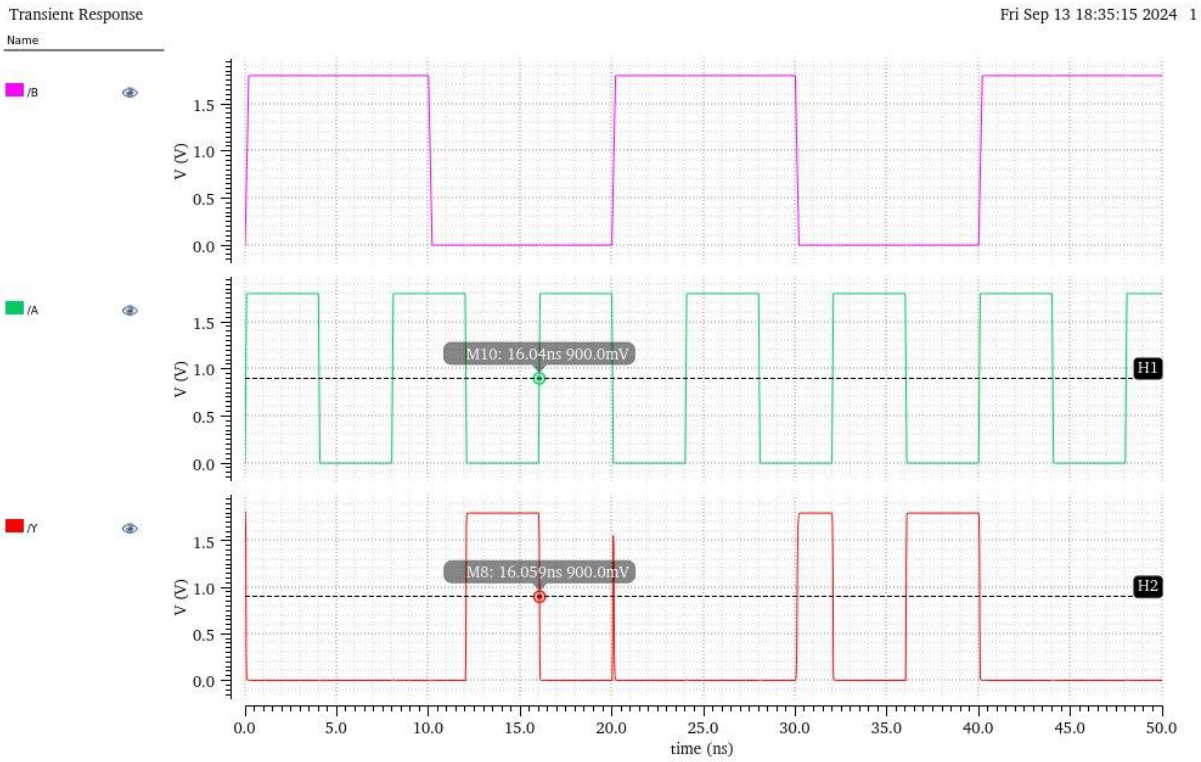
1. DC analysis

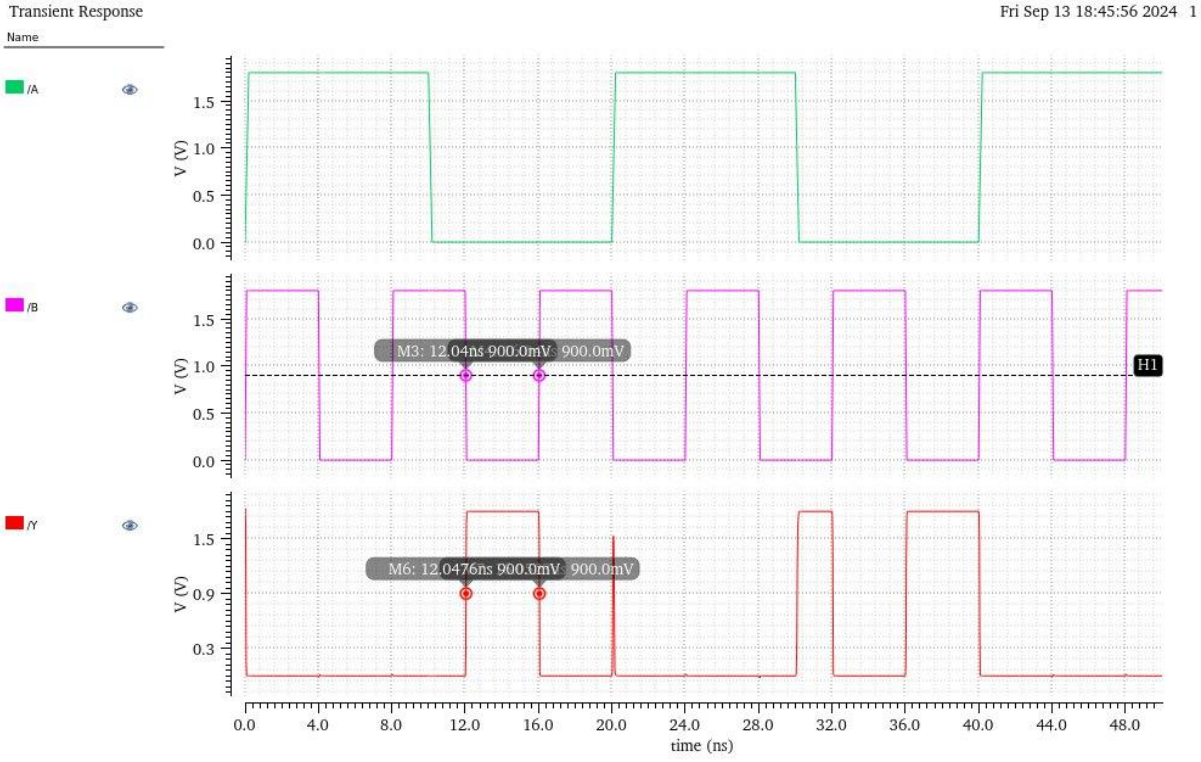


1. Output Y and component parameter B and Threshold Point is 990.2 mV .
2. Output Y and component parameter A and Threshold Point is 1.049 V.
3. Output Y and short both inputs A,B and Threshold Point is 792 mV.

2. . Finding Delays with Transient response:




Transient Response
Fri Sep 13 18:35:15 2024 1
Name
/B
/A
/Y
V (V)
M10: 16.04ns 900.0mV
H1
M8: 16.059ns 900.0mV
H2
time (ns)


Transient Response
Fri Sep 13 18:45:56 2024 1
Name
/A
/B
/Y
V (V)
M3: 12.04ns 900.0mV
900.0mV
H1
M6: 12.0476ns 900.0mV
900.0mV
time (ns)

Analysing Delays.

Input A	Input B	Output Y	Delay
0 to 1 16.04 ns	0	1 to 0 Tphl = 16.059 ns	Td =19ps
1 to 0 15.05 ns	0	0 to 1 Tplh = 15.0572 ns	Td= 7.2ps
0	0 to 1 16.04ns	1 to 0 Tphl = 16.0523 ns	Td= 12.3 ps
0	1 to 0 12.04ns	0 to 1 Tplh = 12.0476 ns	Td =7.6ps
0 to 1	0 to 1 20.06ns	1 to 0 Tphl=20.0654ns	Td=5.4ps
1 to 0	1 to 0 20.02ns	0 to 1 Tplh= 20.0313ns	Td=11ps

TASK -2
Design and Analysis of 1 Bit Comparator

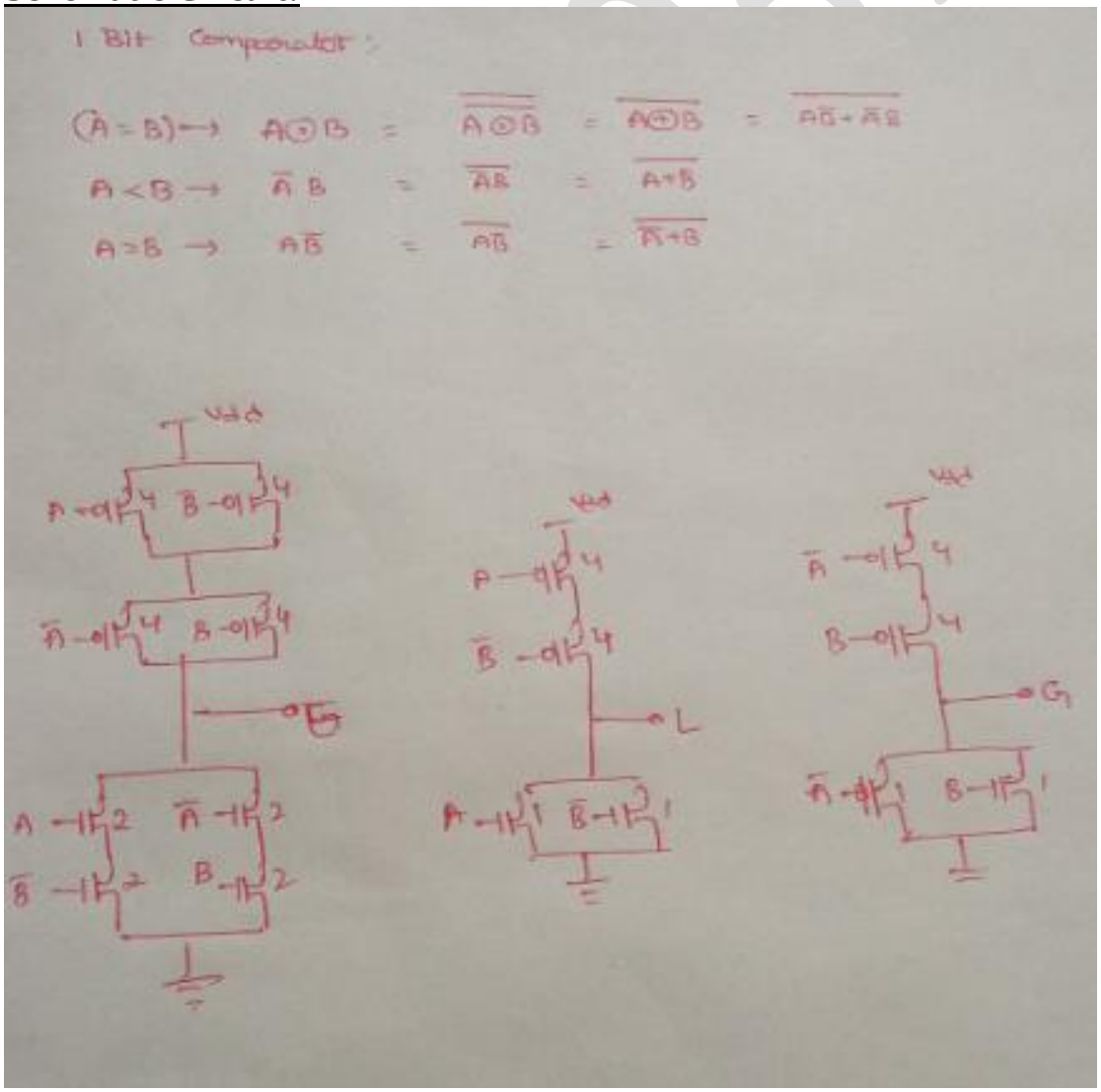
Objectives:

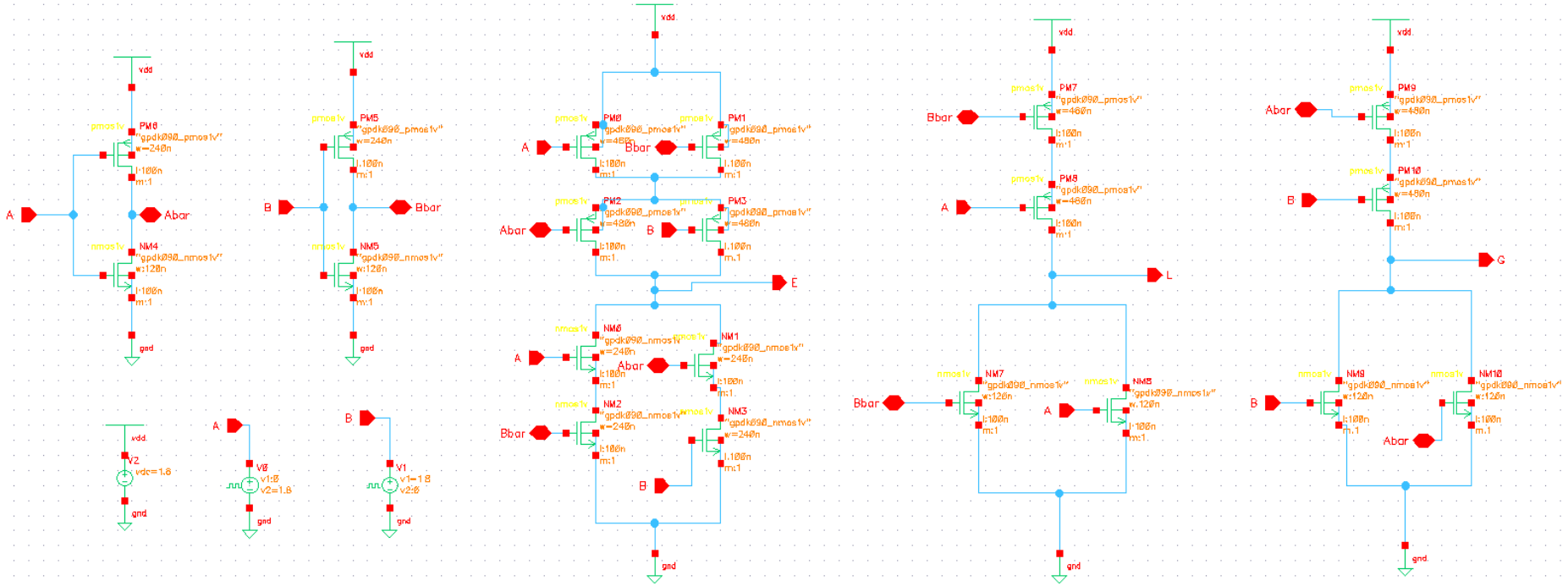
Design a 1 Bit Comparator using
a) CMOS logic or b) Transmission gate logic and plot its transient response. Verify the truth table.

Experimental Procedure:

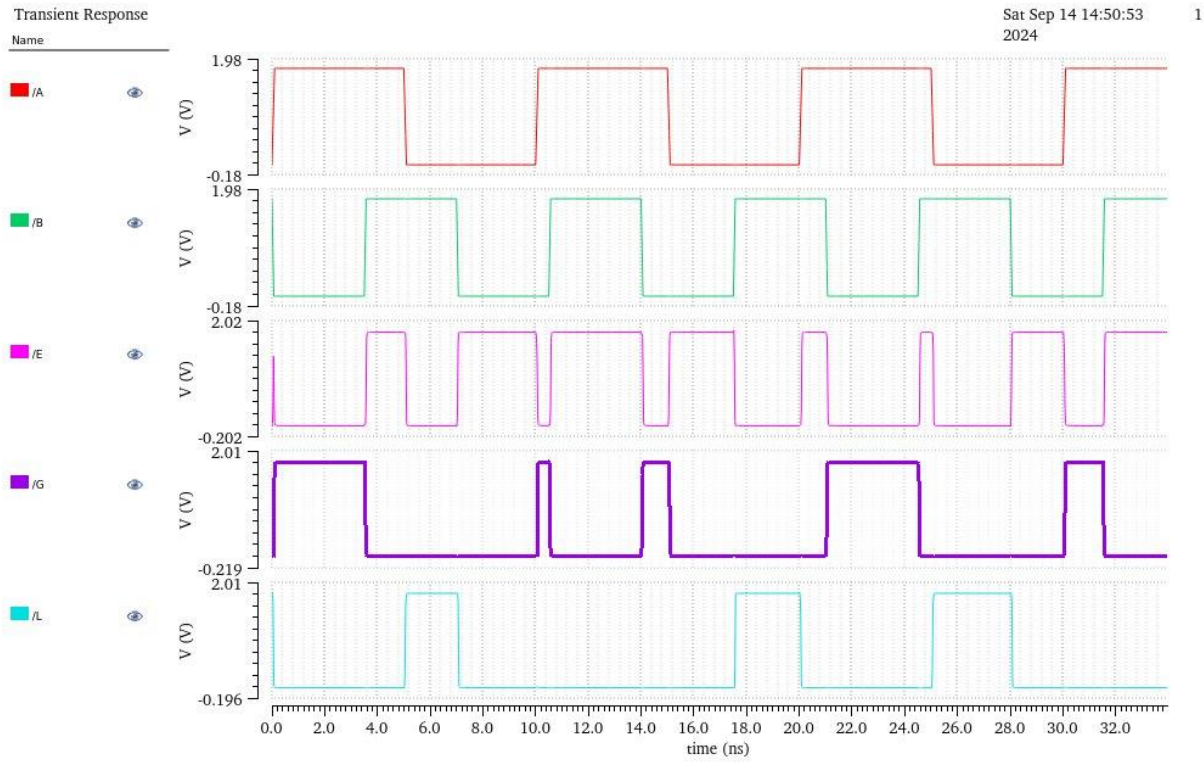
1. Invoke Cadence Virtuoso tool.
2. Construct the schematic as shown in Fig.
3. Perform Transient analysis and verify its functionality.

Schematic Circuit:




vdd
A
Abar
B
Bbar
E
L
G
gnd
PM0
PM1
PM2
PM3
PM4
PM5
PM7
PM8
PM9
PM10
NM0
NM1
NM2
NM3
NM4
NM5
NM7
NM8
NM9
NM10
pmos1v
nmos1v
V2
vdc=1.8
V0
v1:0
v2=1.8
V1
v1=1.8
v2:0

Output analysis:



A	B	G (A>B)	L(A<B)	E(A=B)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Results and Analysis:

From the output graph of our comparator we can successfully verify that

1. Input a = Input b Output E=1, G=0, L=0.
2. Input a > Input b Output G=1, G=0, L=0.
3. Input a < Input b Output L=1, G=0, L=0.

******* **THANK YOU*******