Experiment -8

Setup and Hold time analysis of a CMOS Based D-flip flop.

Objectives:

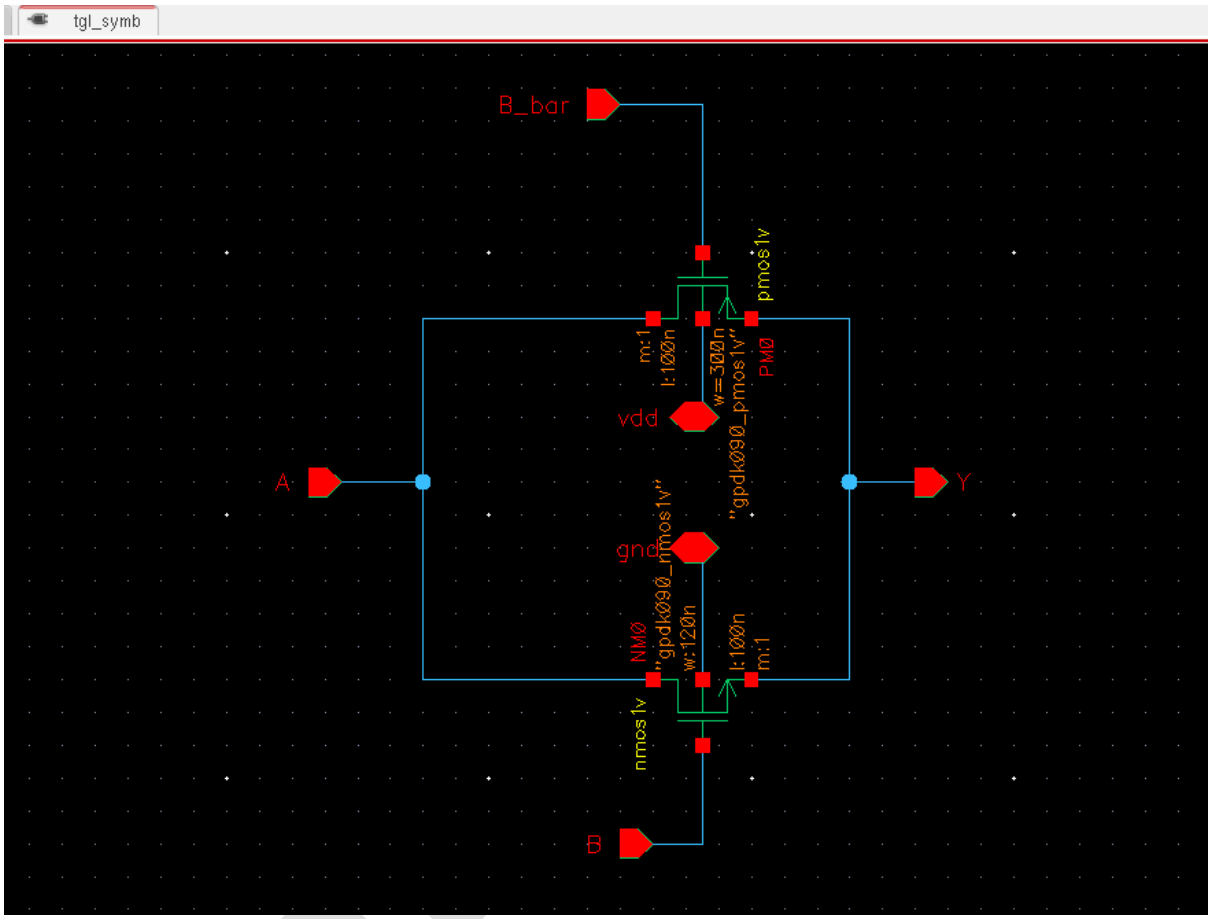
1. To find Setup and Hold time of D-Flip Flop.

Software Used: Cadence Virtuoso

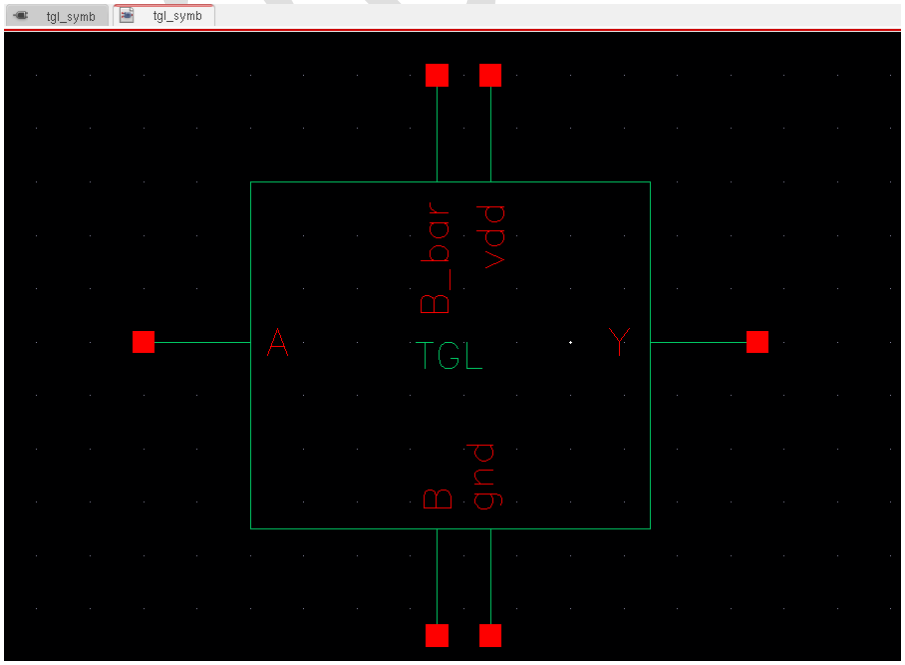
Experimental Procedure:

1. **Create a Symbol for the Inverter**: Design a CMOS inverter schematic with PMOS and NMOS transistors. Generate a symbol for the inverter to make it reusable in other designs.
2. **Design a Transmission Gate Latch (TGL)** Schematic and Symbol: Build a TGL schematic using an NMOS and PMOS in parallel, controlled by the clock signal and its complement. Create a symbol for this TGL for use in the flip-flop design.
3. **Construct a Positive Edge-Triggered D Flip-Flop**: Use a master-slave configuration with a negative-edge latch (master) and a positive-edge latch (slave) to construct a D flip-flop. This setup ensures data is captured on the positive clock edge.
4. **Verify Functionality with Transient Analysis**: Perform a transient analysis to check the D flip-flop's correct operation, confirming that the output follows the input only on the clock's rising edge.
5. **Parametric Analysis for Setup and Hold Time**: Set up a parametric analysis by keeping the clock period as `x` and pulse width as `x/2 ns`. Adjust the input transition timing and observe any deviation in output timing.
6. **Check for Output Deviation:** Identify the point at which the output begins to deviate from the expected value as setup time and hold time requirements are stressed.
7. **Determine Setup Time:** Locate the clock edge where the output starts deviating. Place markers at 0.9 V on both the data and clock waveforms; the time difference between these markers is the setup time.
8. **Determine Hold Time**: After the clock's rising edge, locate where the data causes output deviation. Similarly, mark the transition on data and clock to find the hold time as the time difference between markers.

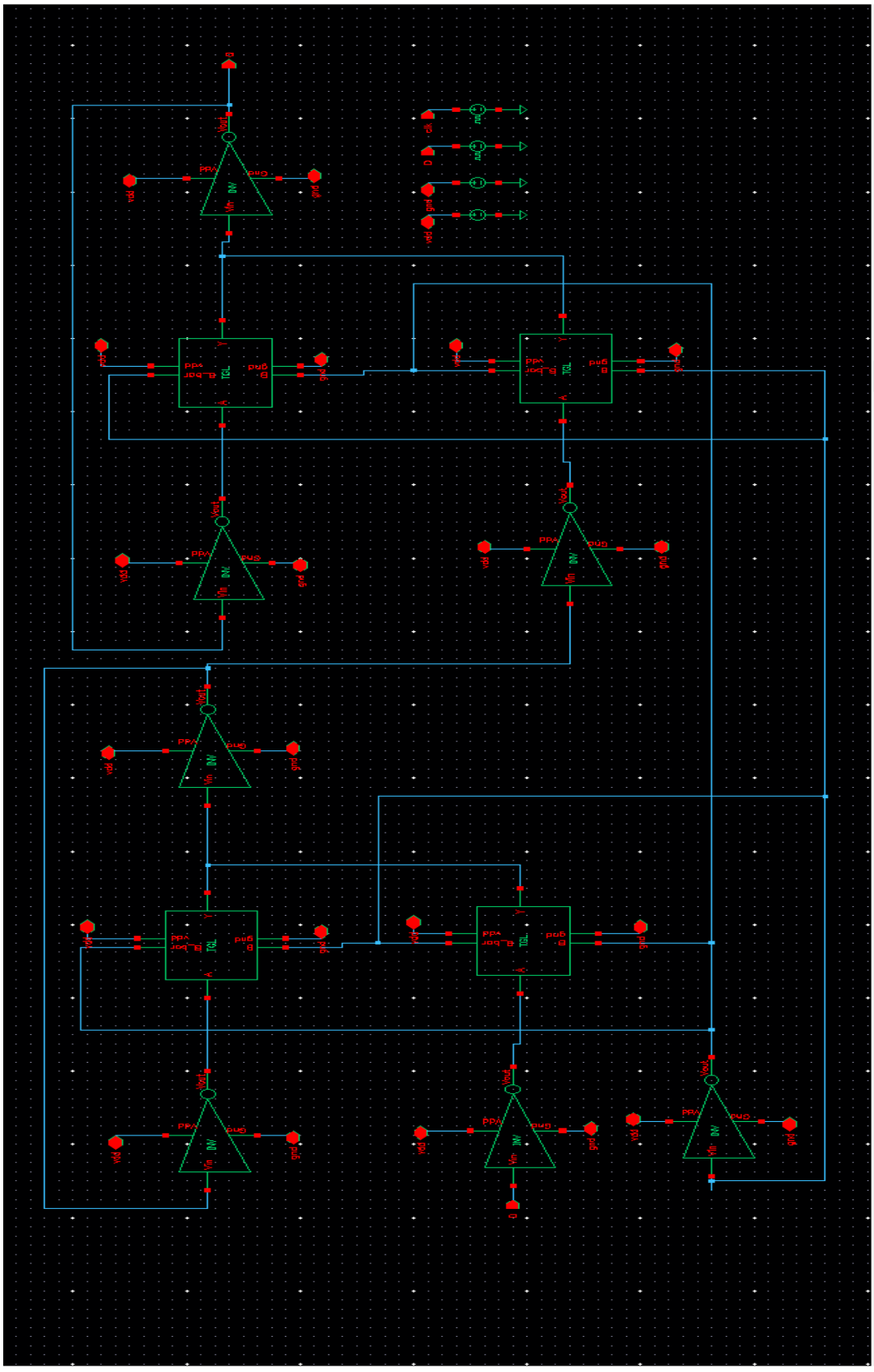
Schematic circuit TGL :



Symbol of TGL:

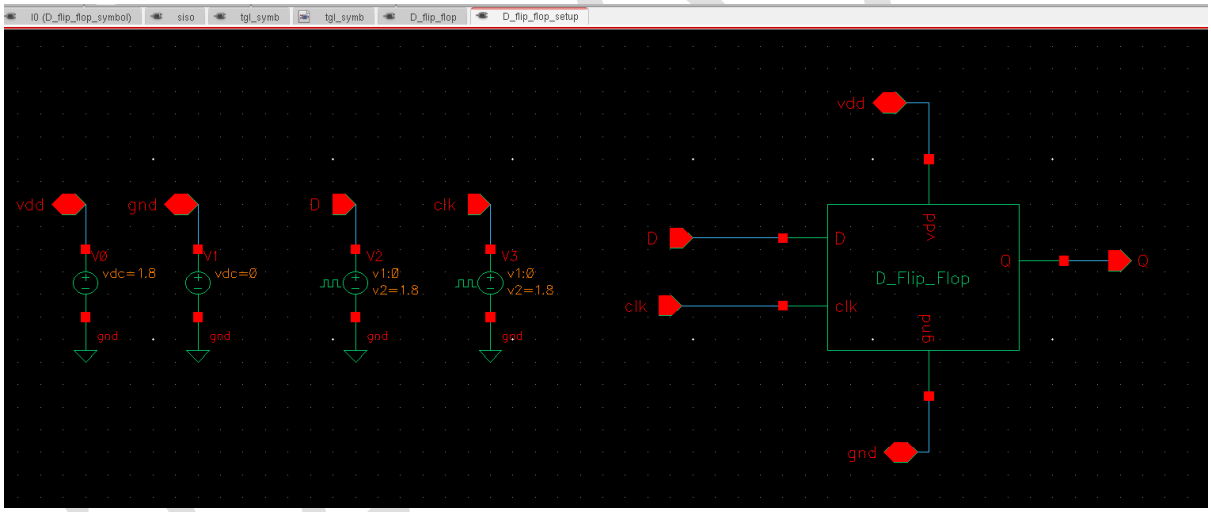


Schematic of D_Flip Flop:

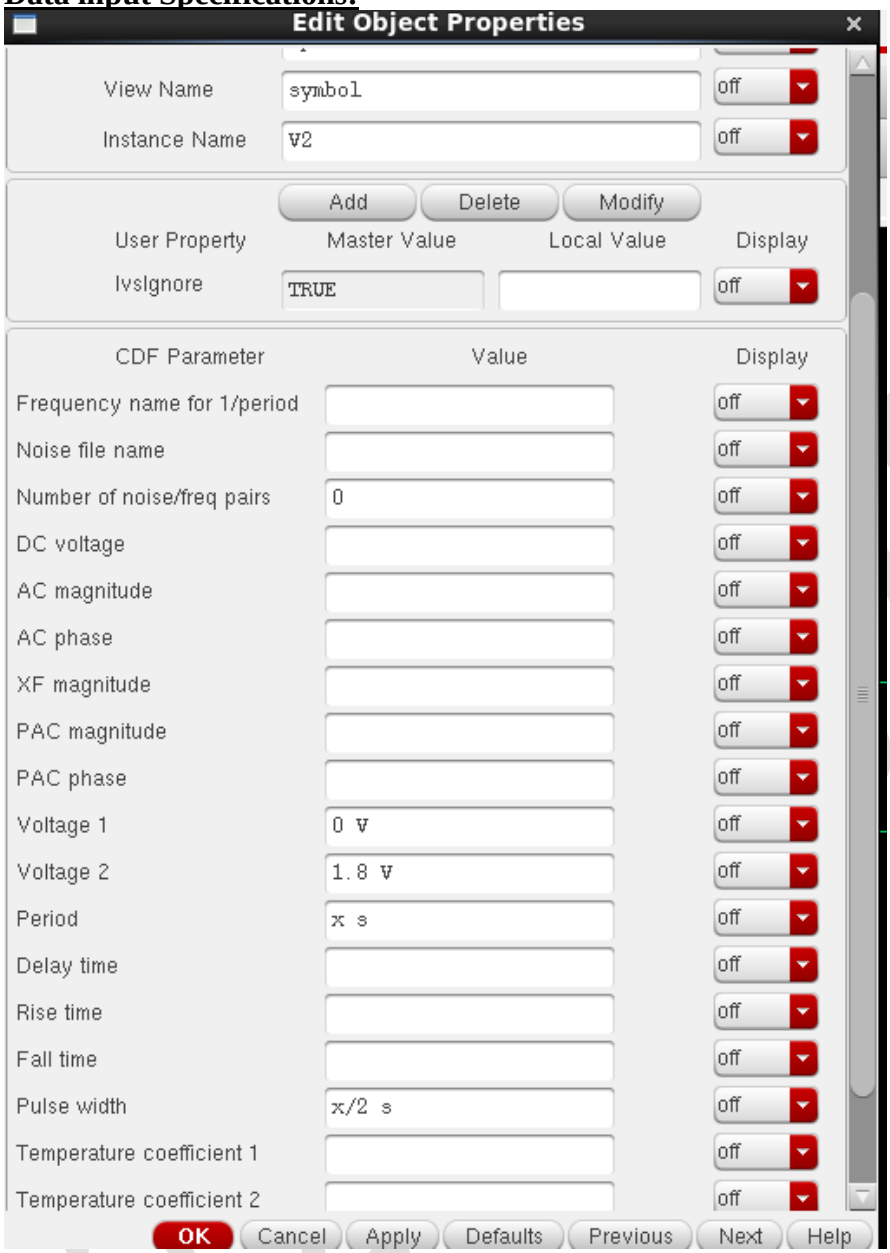


Transient analysis of D-Flip Flop:

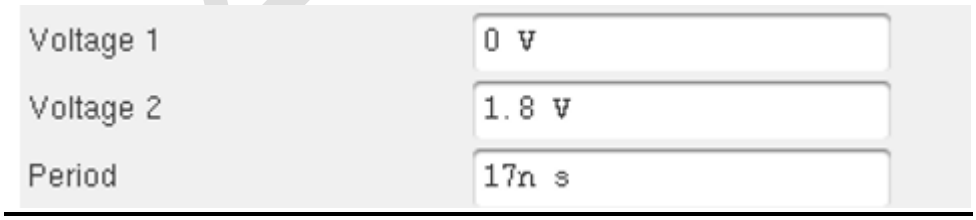
Schematic to find Setup time and hold time:



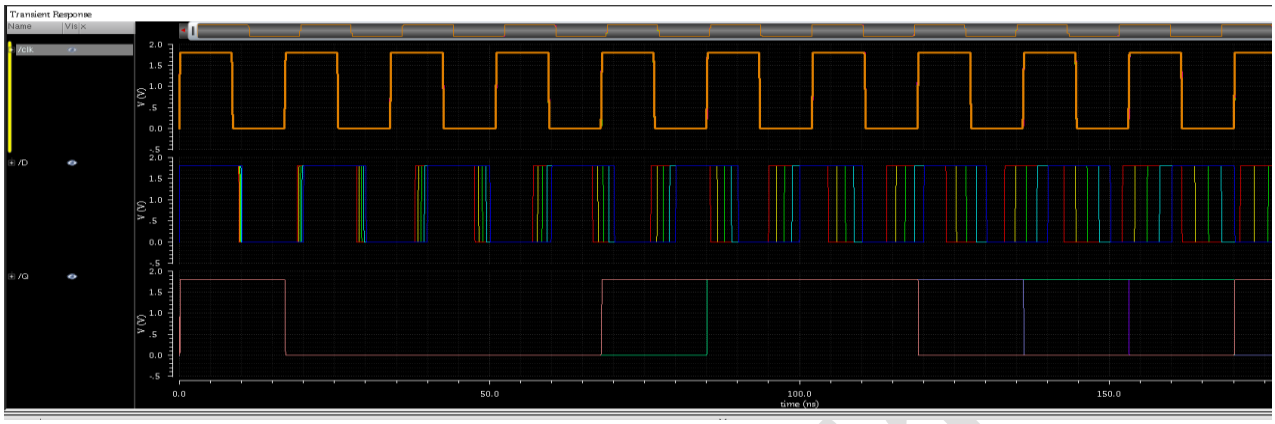
Data input Specifications:



Clock Specifications:

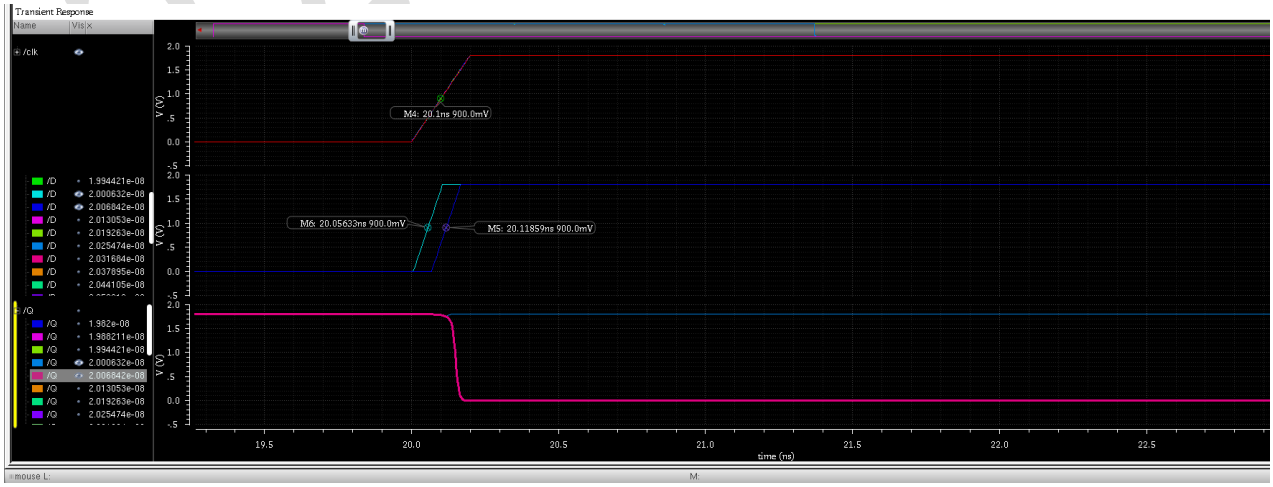


Output of parametric analysis of D-Flip Flop:



For Setup Time:

For Hold Time:



Results and Analysis:

1. **Setup Time:**
   Setup time is the minimum amount of time the data signal should be held steady before the clock event so that the data are reliably sampled by the clock.

   T >= Tcq + Tplogic+ Tsu

   Tsetup = 119.085ns-119.05169ns

T setup =0.03331ns

2. **Hold time:**
   It is the minimum amount of time the data signal should be held steady after the clock event so that the data are reliably sampled.

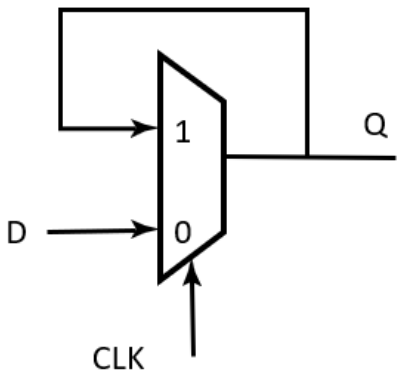
   Thold<= Tcdregister + Tcd_logic

   Thold = 20.11859ns-20.1ns

Thold = 0.01859ns

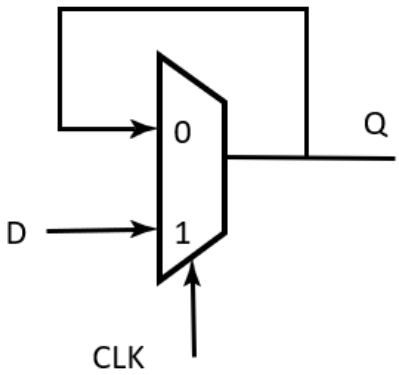
3. Mux_Based Latches:

Negative latch
(transparent when CLK= 0)



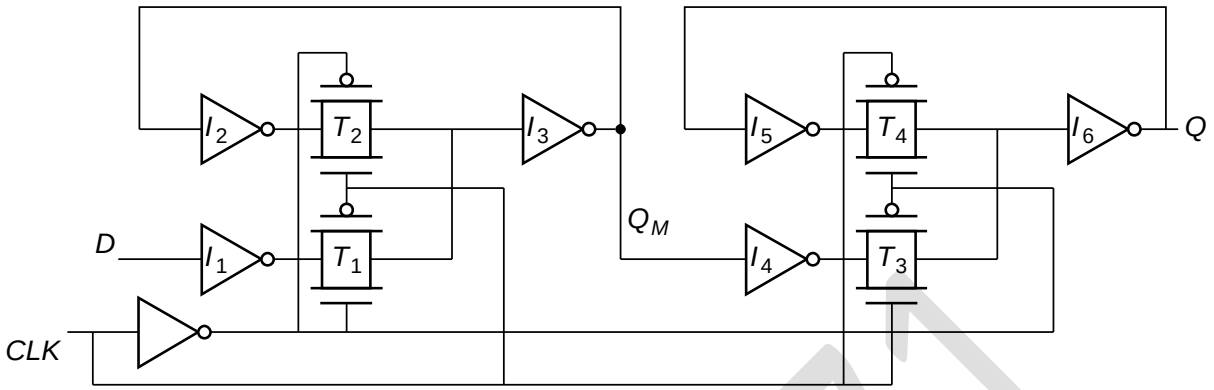
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Positive latch
(transparent when CLK= 1)



$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Master slave configuration of D_Flip Flop:



Set up time – I1-T1-I3-I2
Tsetup: 3tpd_inv+tpd_tx.

Propagation delay T3-I6
tc-q=tpd_inv+tpd_tx

******* **THANK YOU*******