TASK -4

Design a 4 bit SISO shift register and obtain its transient response

Objectives:

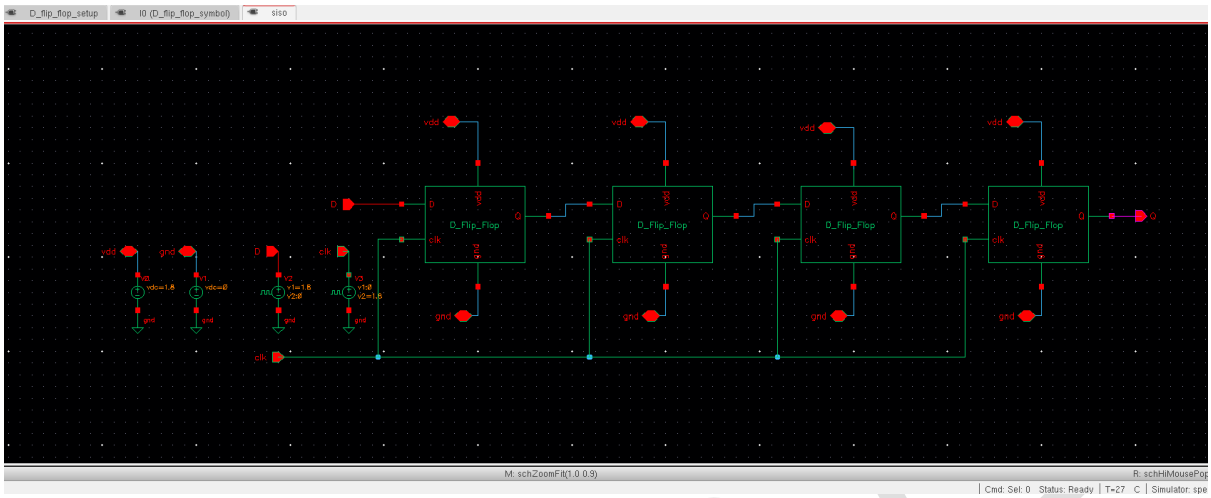
1. To create a 4 Bit SISO shift register and obtain its transient response.

Software Used: Cadence Virtuoso

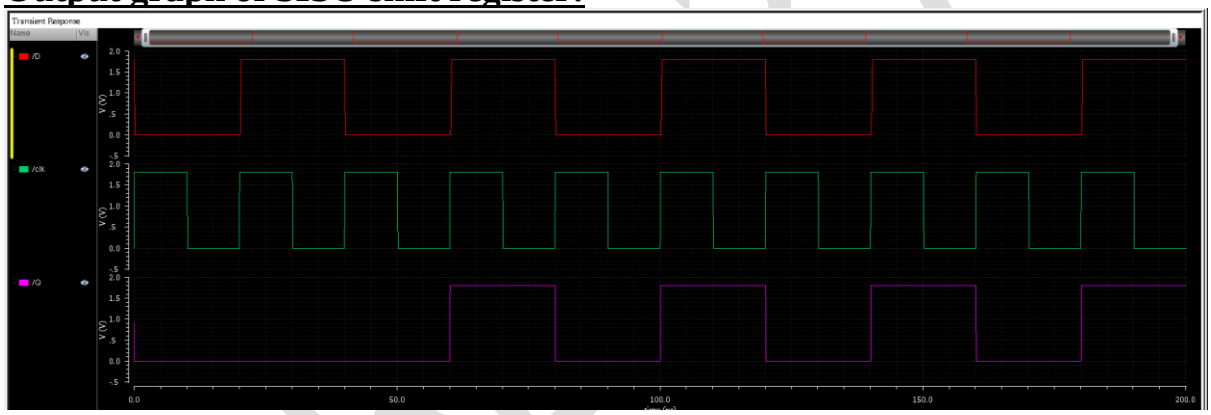
Experimental Procedure:

1. Create a symbol for the inverter by designing the CMOS inverter schematic and generating its symbol for reuse.
2. Design a transmission gate latch (TGL) schematic and create its symbol.
3. Construct a positive edge-triggered D flip-flop using a master-slave configuration with a negative-edge latch as the master and a positive-edge latch as the slave.
4. Generate a symbol for the D flip-flop schematic.
5. Connect four D flip-flops in series, with the output of each feeding into the next; apply the input to the first flip-flop and take the output from the last.
6. Connect a common clock to all flip-flops and perform transient analysis to observe the data shifting through the register with each clock cycle.

Schematic circuit of Serial In Serial Out shift register :



Output graph of SISO shift register:



Results and Analysis:

Clock Cycle	Input	Q0	Q1	Q2	Q3	Output
0 (Initial)	-	0	0	0	0	0
1	1	1	0	0	0	0
2	0	0	1	0	0	0
3	1	1	0	1	0	0
4	0	0	1	0	1	**1**
5	1	1	0	1	0	0
6	0	0	1	0	1	1
7	1	1	0	1	0	0
8	0	0	1	0	1	1

For a 4-bit shift register, the results can be analyzed as follows

1. Output Delay Due to Clock Cycles: Since the shift register has four flip-flops, the input data takes four clock cycles to propagate through all stages of the register.

2. Serial Output After Four Cycles: After the 4th clock cycle, the input data begins to appear at the output in a serial manner. This is due to each flip-flop passing its data to the next stage on each clock pulse.

3. Input and Output Sequence: Given an input sequence of `101010`, after the 4th clock
cycle, the output sequence will also be `101010`. This means that after four cycles, the shift register accurately reflects the input sequence, outputting the bits in the same order they were entered.