EXPERIMENT -1

Analysis of Voltage Transfer characteristics (VTC), Delay and Power calculation of CMOS Inverter.

Objectives:

1. **To do DC analysis of CMOS Inverter.**
2. **Find Threshold point using DC analysis.**
3. **Find Noise Margin.**
4. **Perform Transient Analysis and find Delay.**
5. **Power Analysis using different load capacitances and find average power.**

Software Used: Cadence Virtuoso

Experimental Procedure:

1. Invoke Cadence Virtuoso tool
2. Construct the schematic as shown in Fig.
3. Invoke ADEL and perform DC analysis to plot VTC curve.
4. Perform parametric analysis and analyse the VTC curve for different aspect ratios (W/L)
5. Using VTC curve to calculate the Low and High Noise Margins (NML and NMH) using the formula given below.

   NMH=VOH-VIH
   NML=VIL-VOL
6. Perform Transient analysis to calculate the propagation delay (Tpd)

   TPHL is the delay when output switches from high-to-low, after input switches from low-to-high.

   TPLH is the delay when output switches from high-to-low, after input switches from low-to-high.

$$Tpd = \frac{T_{PHL} + T_{PLH}}{2}$$

7. Perform the transient analysis to calculate the power consumption.

Why Are we sizing the inverter?

1. Effective Resistance:
   Transistor sizing impacts the effective resistance, which is crucial for optimizing delay and performance. The RC delay model treats a transistor as a switch in series with a resistor, where the effective resistance is the ratio of the drain-to-source voltage (Vds) to the drain current (Ids) averaged across the switching interval.

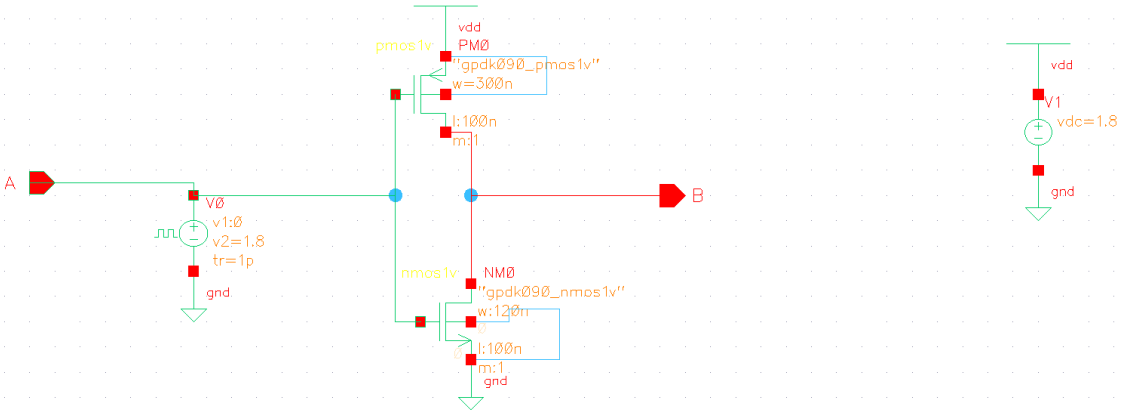
2. Nmos Transistor Resistance:
   A unit nMOS transistor is defined to have an effective resistance R. When the width of an nMOS transistor is increased by a factor of k, the resistance decreases to R/k, as the transistor delivers k times more current.

3. Pmos Transistor Resistance:
   A unit pMOS transistor generally has a higher resistance, typically around 2R, due to its lower carrier mobility compared to nMOS transistors. This means that to match the driving strength of an nMOS, the pMOS needs to be sized larger.

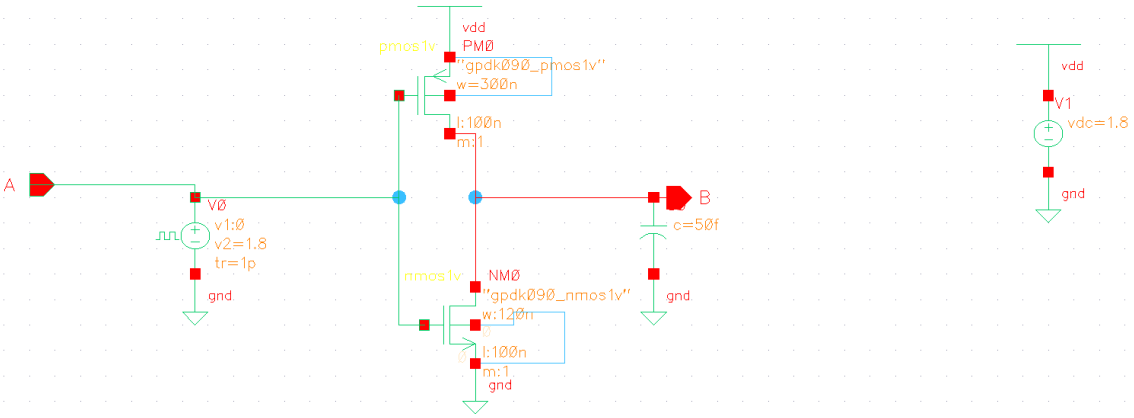
4. Therefore we size inverter because to balance the effective resistance of both the pull-up (pMOS) and pull-down (nMOS) networks in a CMOS inverter or logic gate

5. We make Width of Pmos = 2.5 * Width of Nmos.

Schematic circuit of CMOS Inverter without Capacitance :

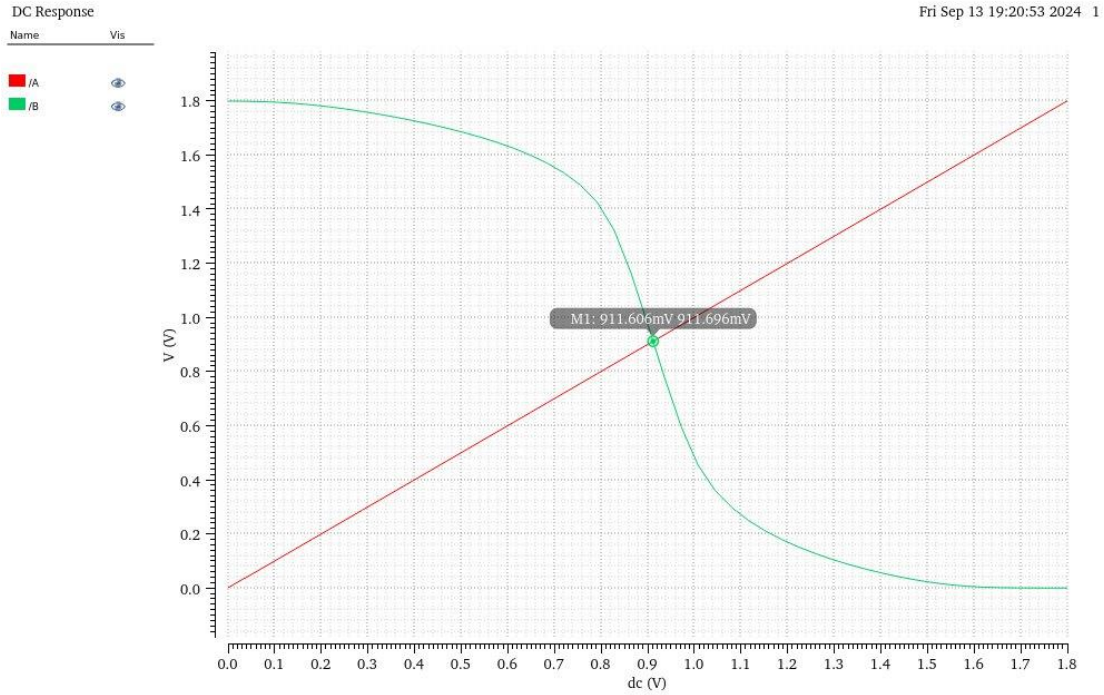


Schematic circuit of CMOS Inverter with Capacitance:



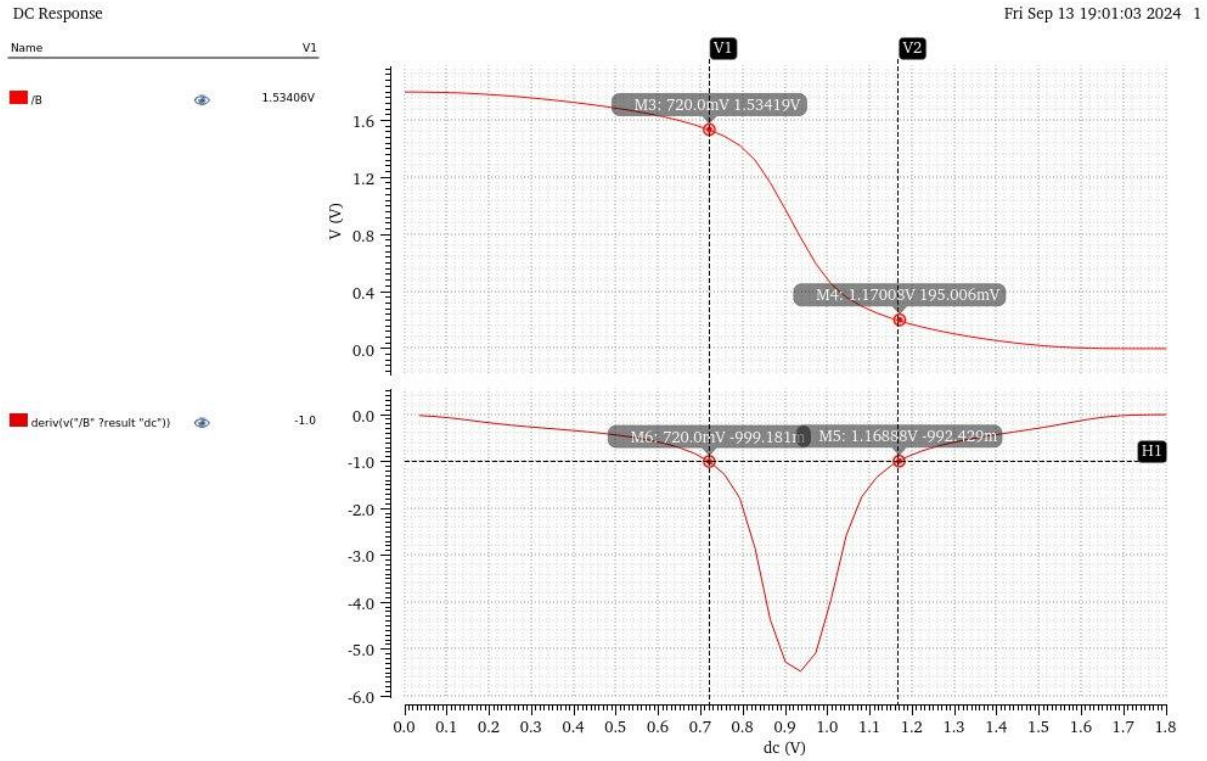
Results and Analysis of all objectives:

1. DC response and finding Threshold point.



Threshold point = 911.606 mV (Vin = Vout)
Note: Wpmos/Wnmos =2.5 : 1

2. Noise Margin Analysis:



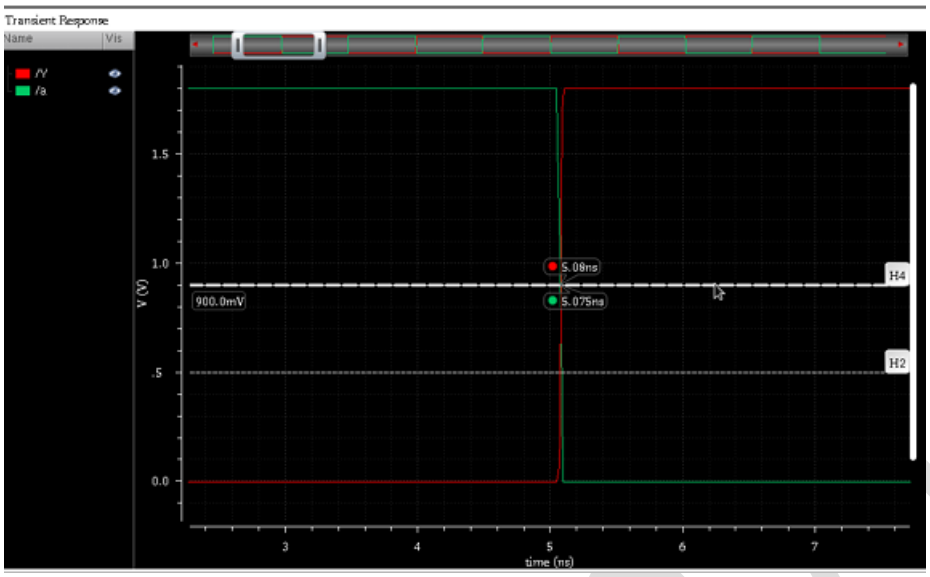
Derivative of output has been plotted to find V IL and V IH at slope =-1;

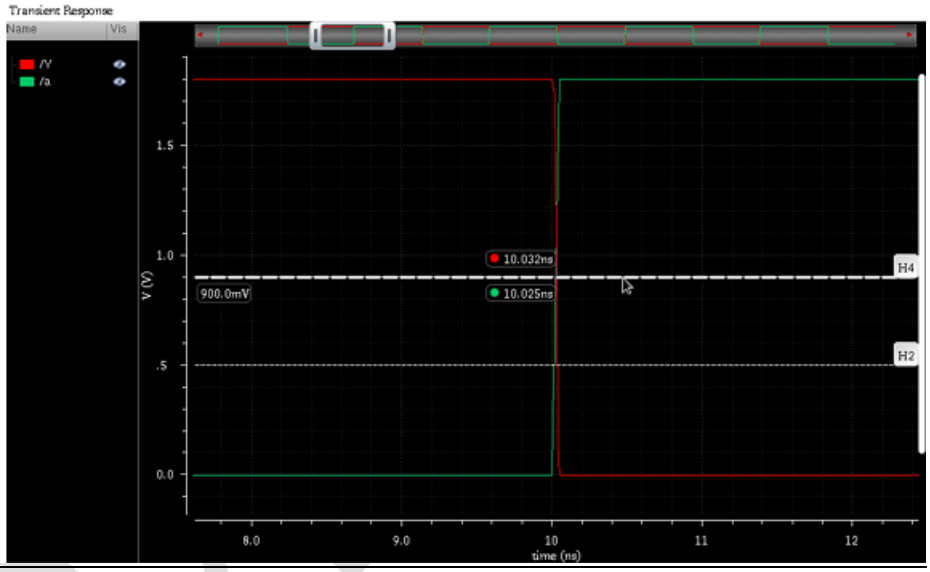
From Graph:

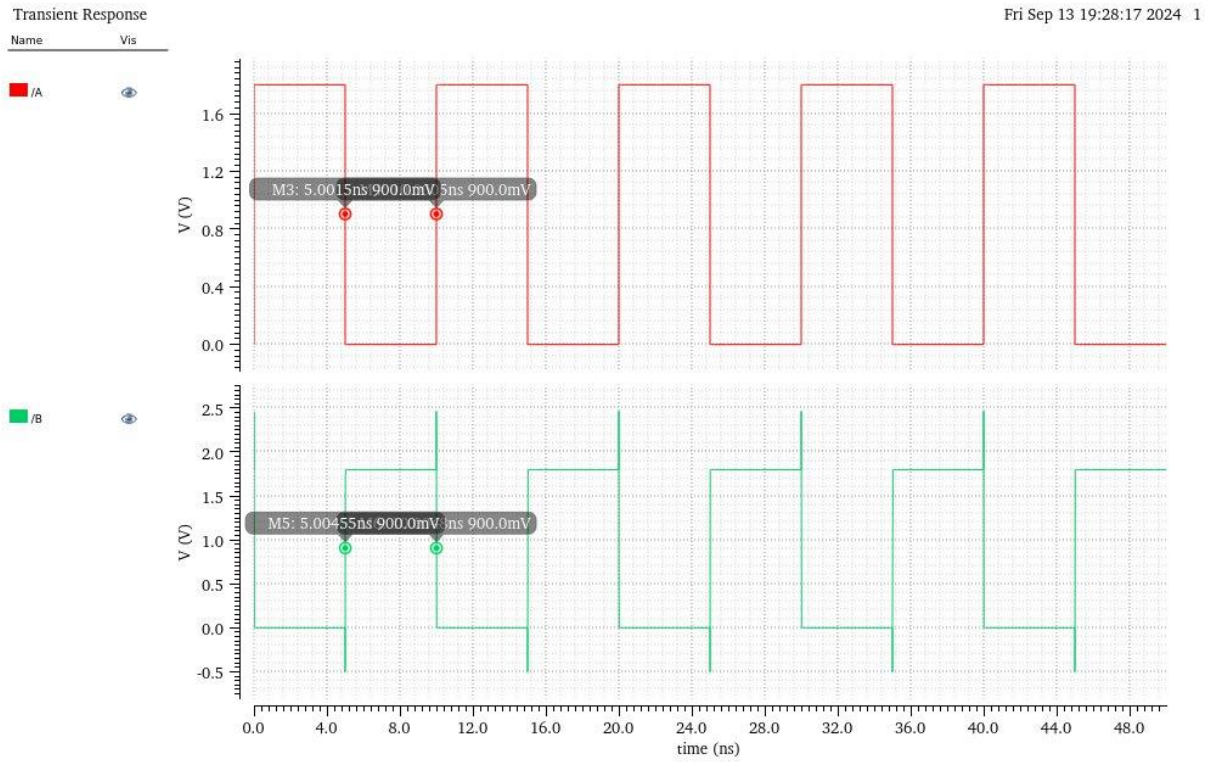
V OH = 1.53406V
V OL = 197.481 mV
V IH = 1.16733 V
V IL = 720.107 mV

NMH= VOH- VIH
= 0.36673 V
NML= VIL- VOL
= 0.524994 V

3. Transient analysis and delay.





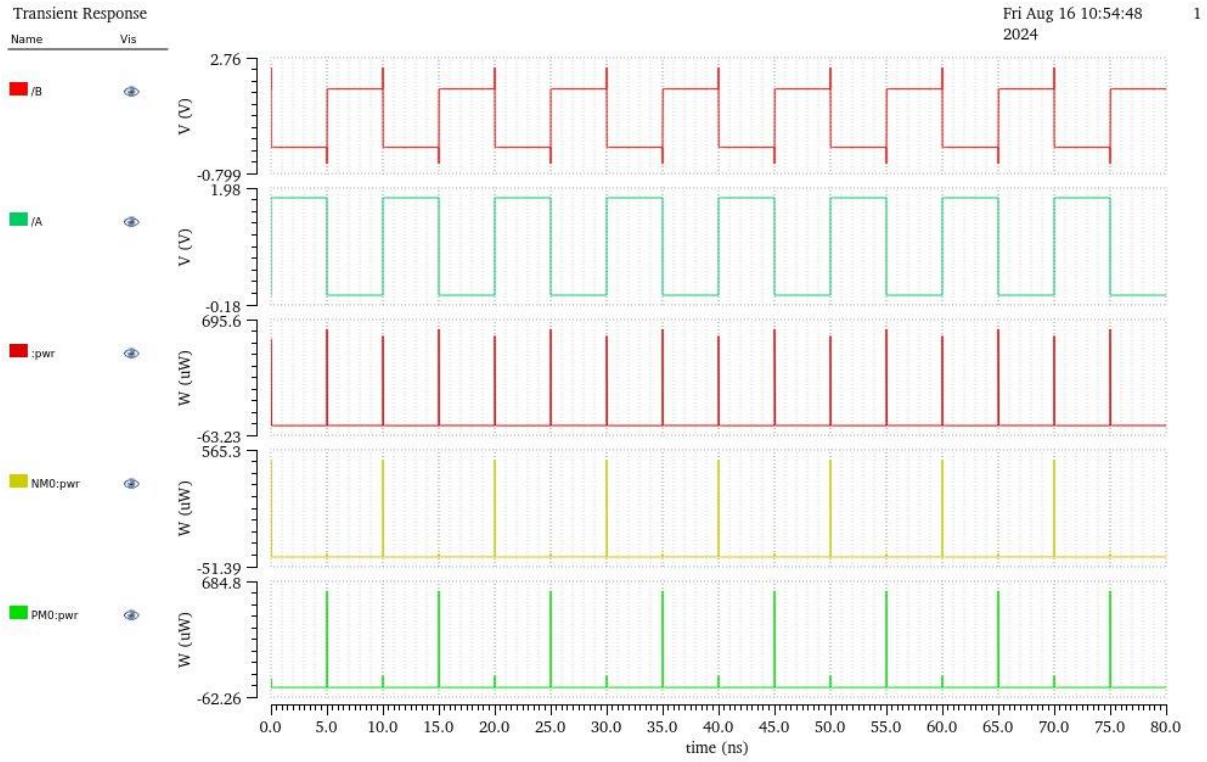


Tpdr = 5.004547 ns – 5.0015 ns
= 3.05 ps
Tpdf = 10.00485 ns – 10.0005ns
= 4.35 ps.

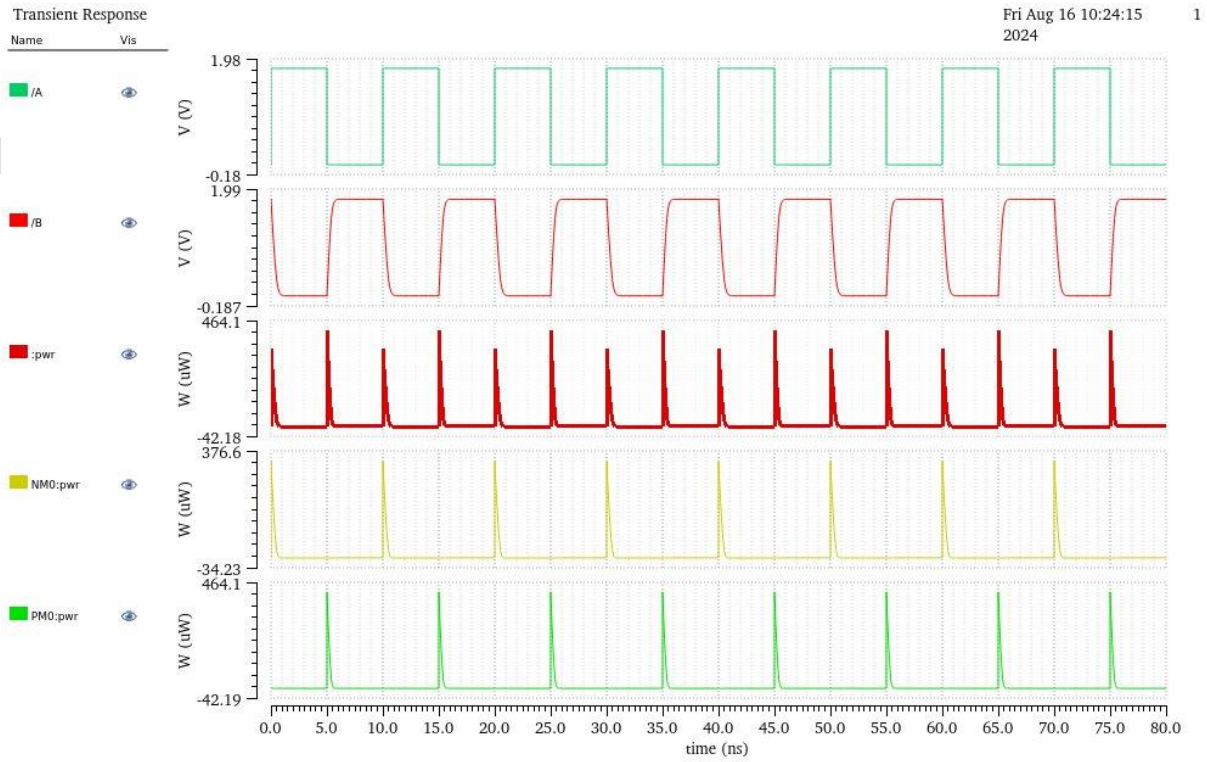
Td = (Tpdr+Tpdf)/2
= 3.7 ps

4. Power Disipiation Analysis:

With C=0 farads.



With some value of Capacitance.



To Find average power:

1. Save all outputs in ADEL Window
2. Click on Power signal to output - All
3. Click save device currents - All
4. Save output format – psfvl
5. Now run the simulation and in Graph open browser section and open psf file.
6. Then plot graphs of Pow , Nmos Pow, Pmos Pow.
7. Select and send Pow signal to calculator and find Average of that.

S No	C (f F)	Average Power (uW)
1.	10	2.034
2.	20	3.678
3	30	5.329
4	40	6.964
5.	50	8.021

By observing the above plot and table, an increase in load capacitance results in an increase in power dissipation.