Experiment -3

Design a chain of inverters for a minimum delay.

Objectives:

4. **To find input capacitance of a inverter.**
5. **Finding delay of stages of NOT gate using linear delay model.**
6. **Finding optimum number of stages for less delay through linear delay model.**

Software Used: Cadence Virtuoso

Experimental Procedure:

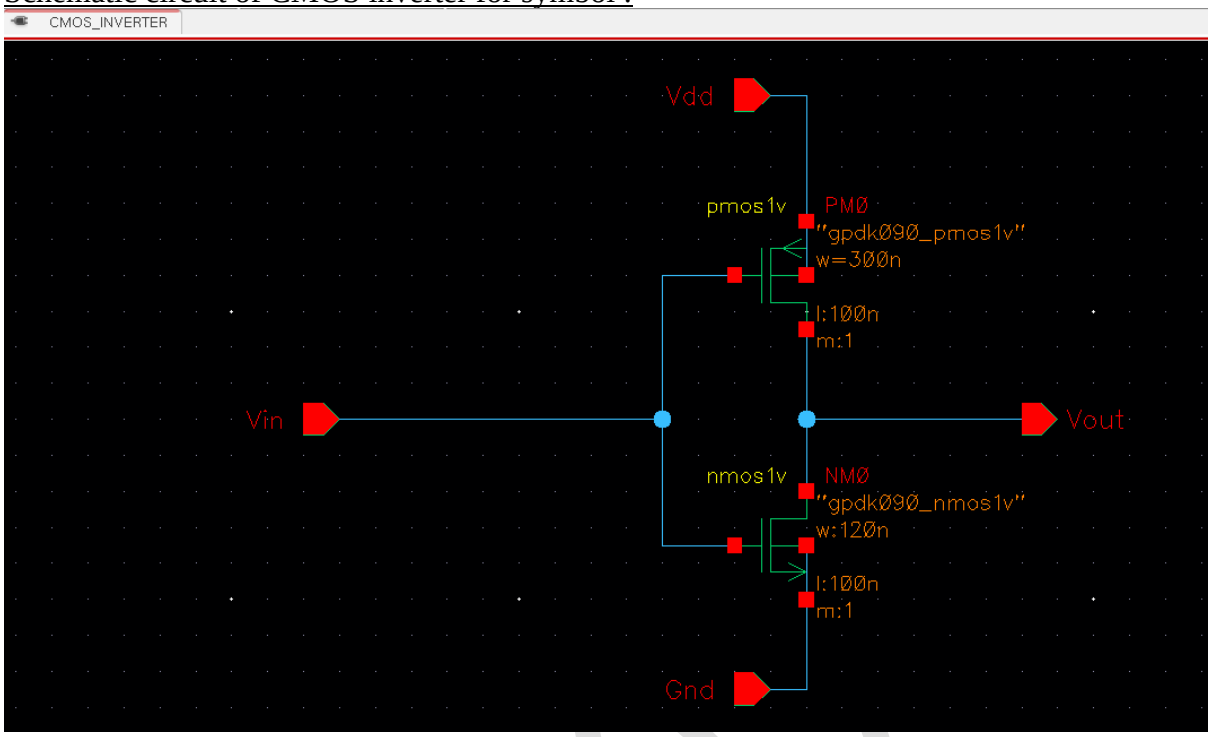
Part a) To find input capacitance of NOT gate.

7. Create a symbol for two input NOT gate.
8. To find the input capacitance of the of the NOT gate , invoke the symbol you have created and connect a piece wise linear source to inputs of NOT gate and perform transient analysis..
9. Plot the input voltage(net) and input current(node).
10. Integrate the output plot i.e current plot from 0ns to time period the wave(10ns).
11. Find input capacitance using the formulae $C_{in} = \frac{\int i\,dt}{v_C(t)}$.
12. Find load capacitance = 64x(Cin).

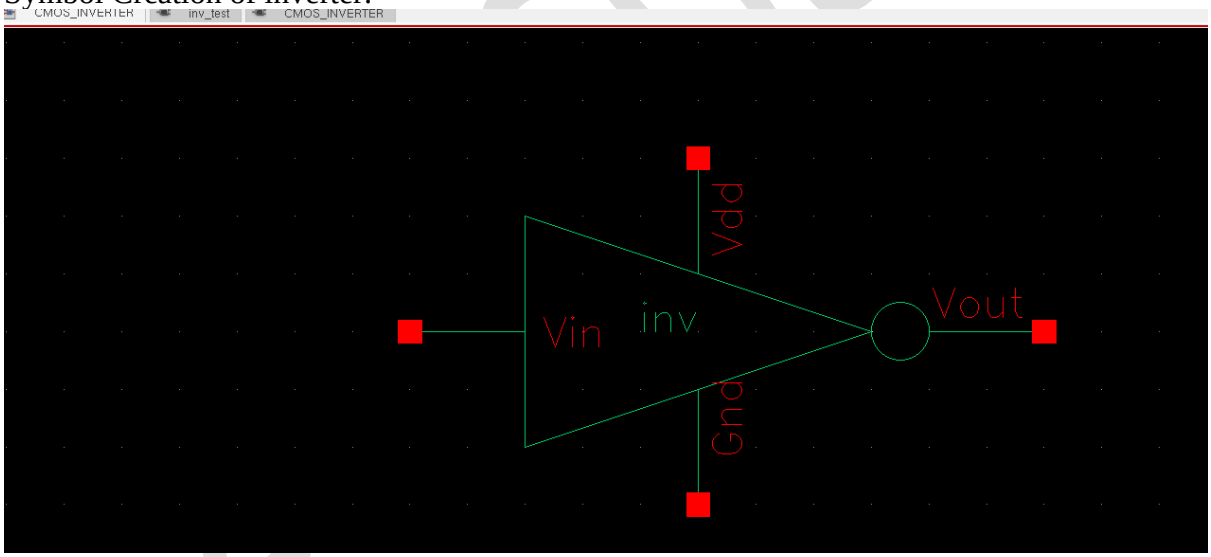
Part b) To find number of stage of chain of not gates that gives less delay.

4. Create a chain of NOT gates i.e 1 stage, 2 stage, 3 stage, 4 stage with load capacitance calculated in above part.
5. Do Sizing of pull up network and pull down network accordingly.
6. Find delay between input and output and check which stage has less delay.

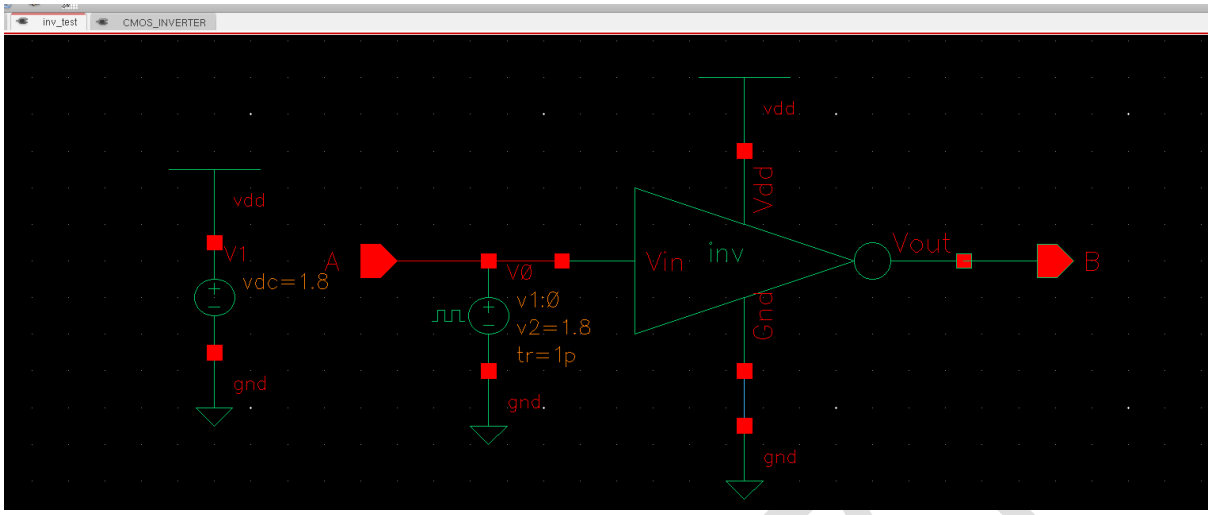
Schematic circuit of CMOS inverter for symbol :



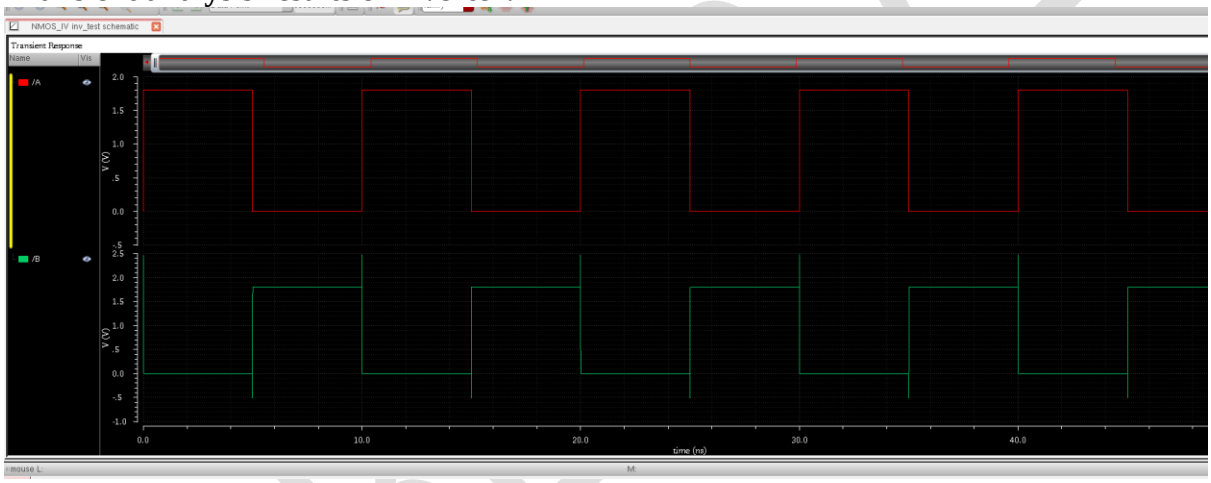
Symbol Creation of inverter:



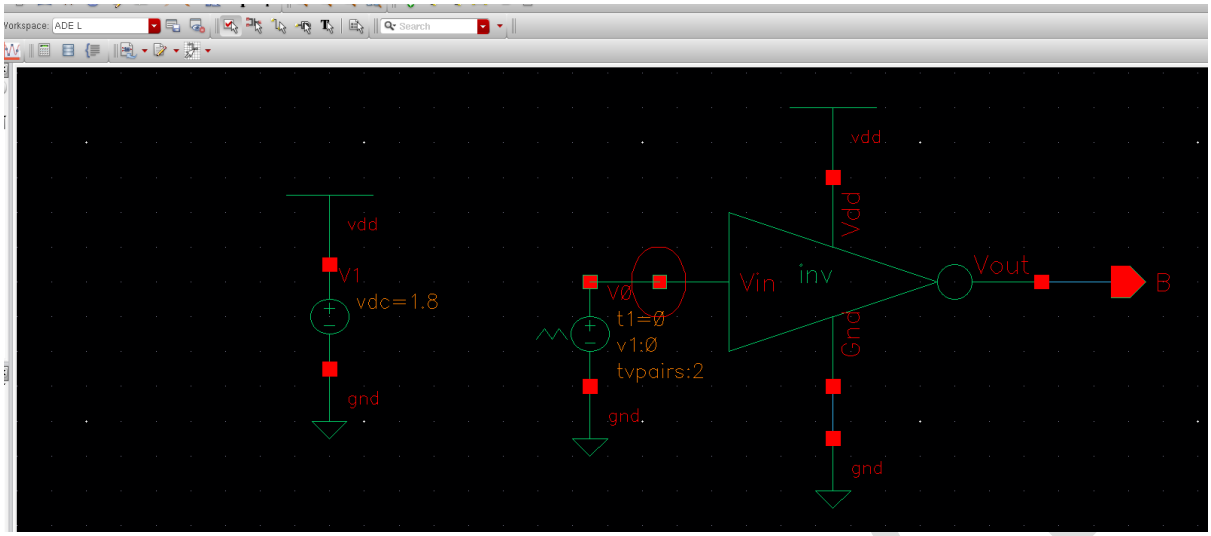
Schematic circuit to test the inverter:

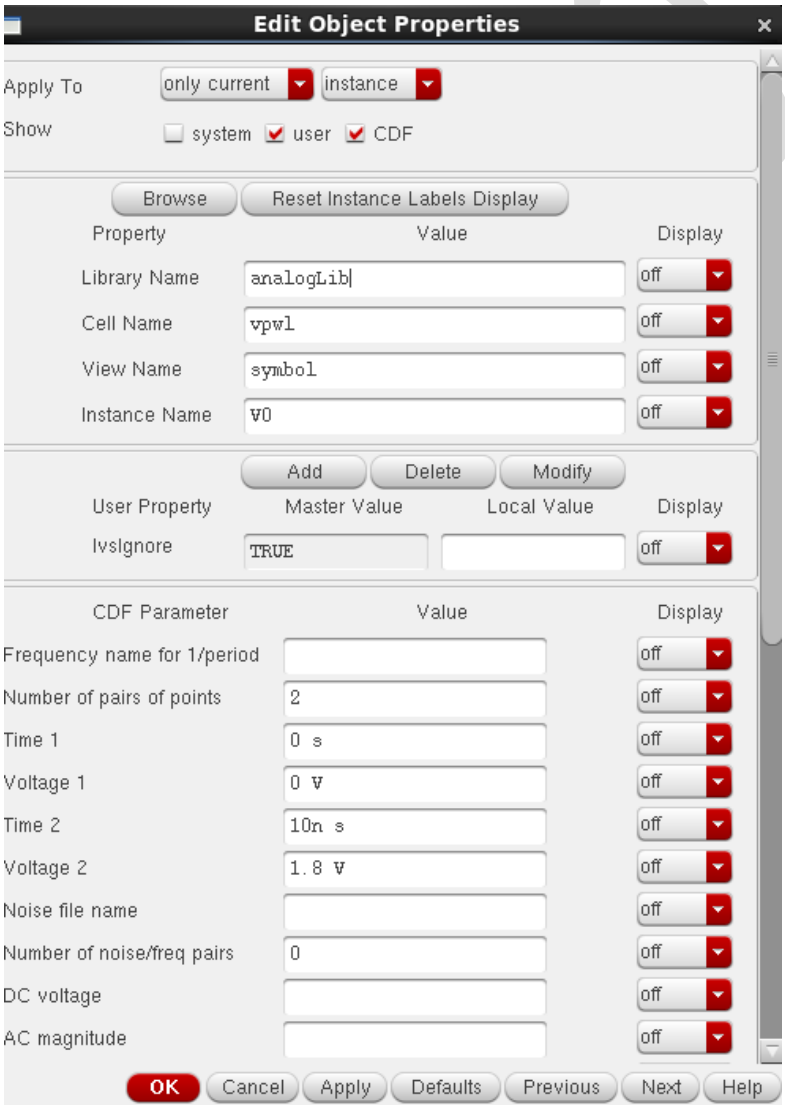


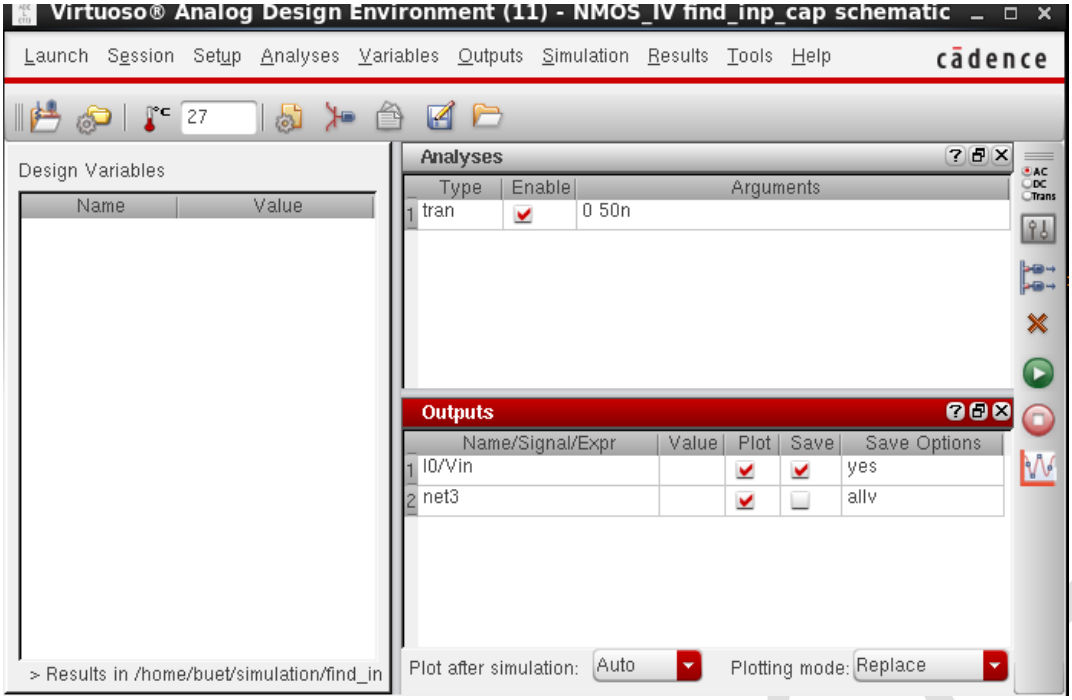
Transient analysis results of inverter:



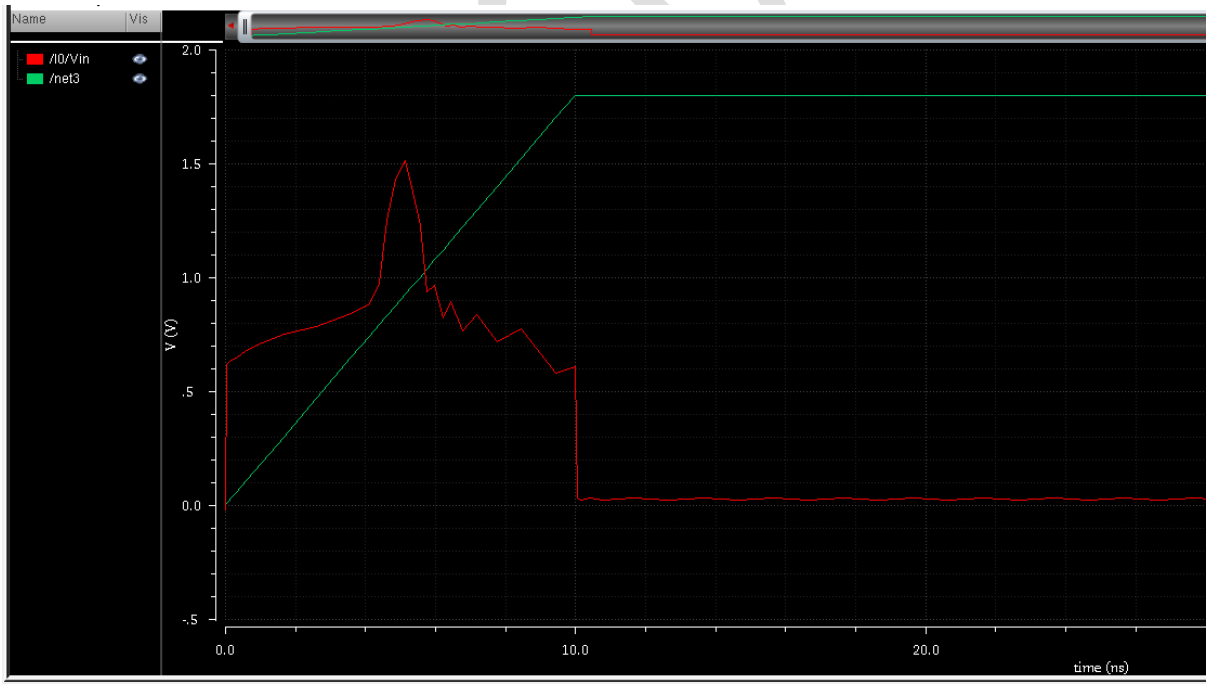
Schematic circuit to find input capacitance of inverter:

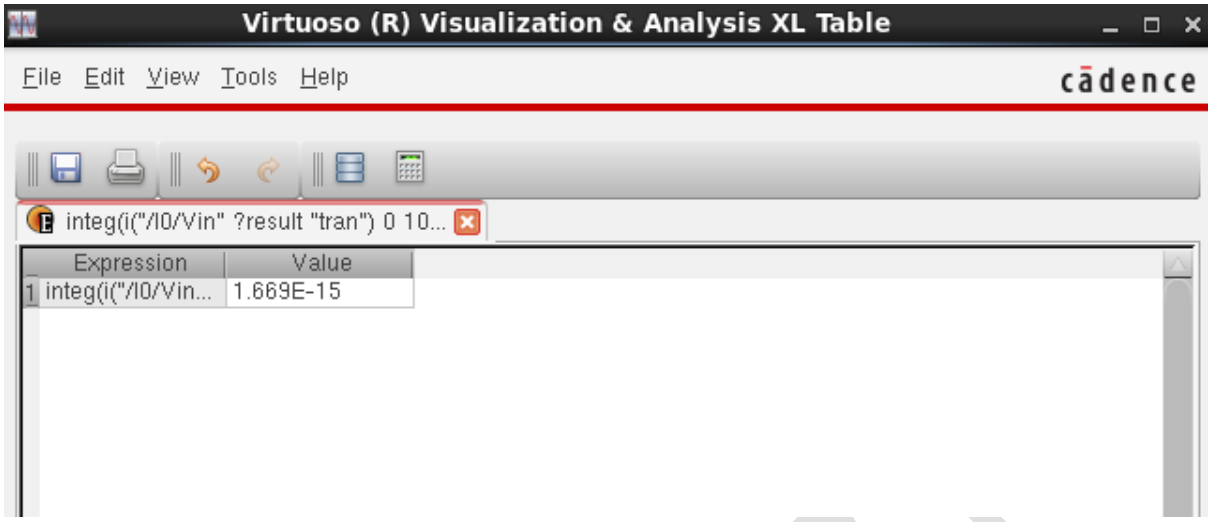




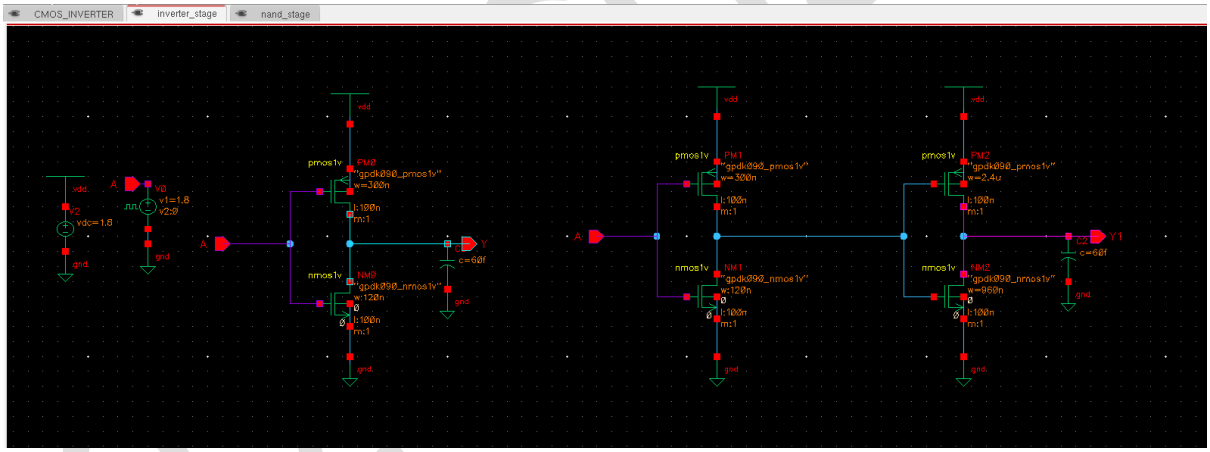


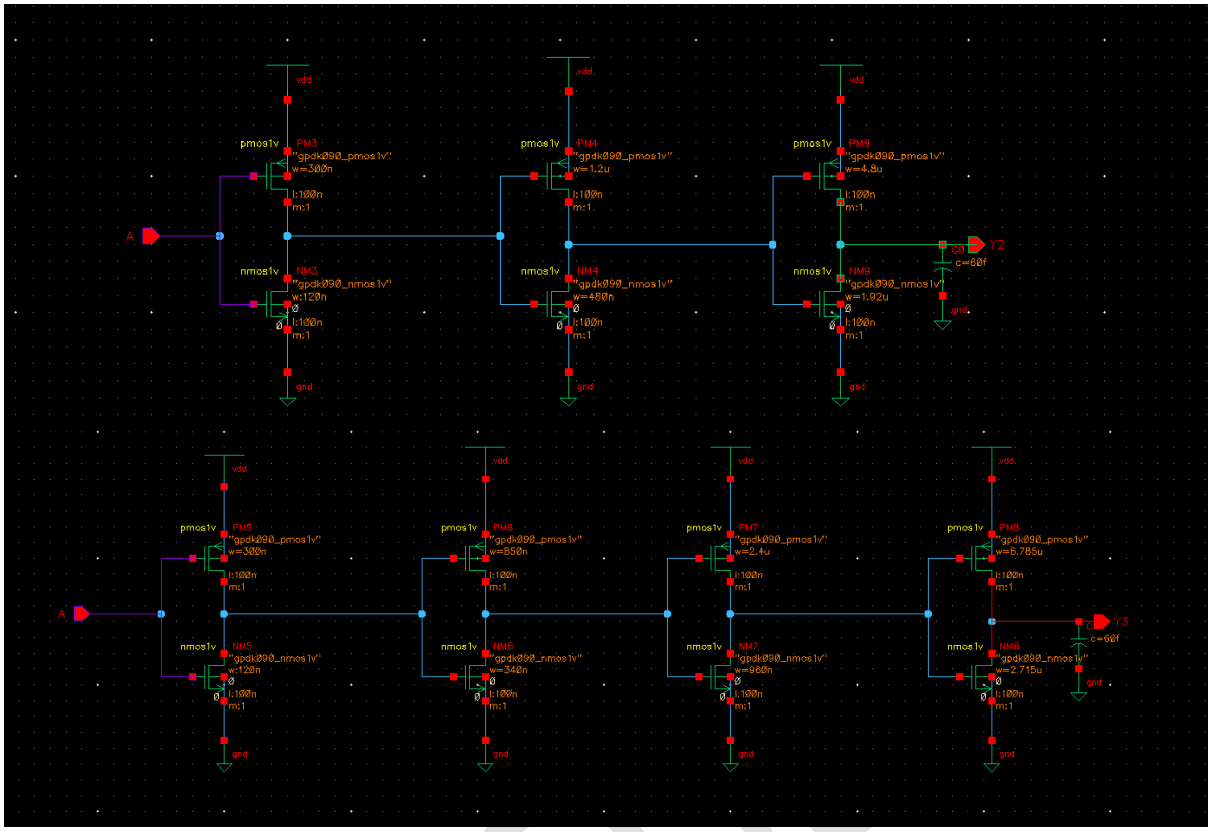
Output plot of input capacitance vs input current:



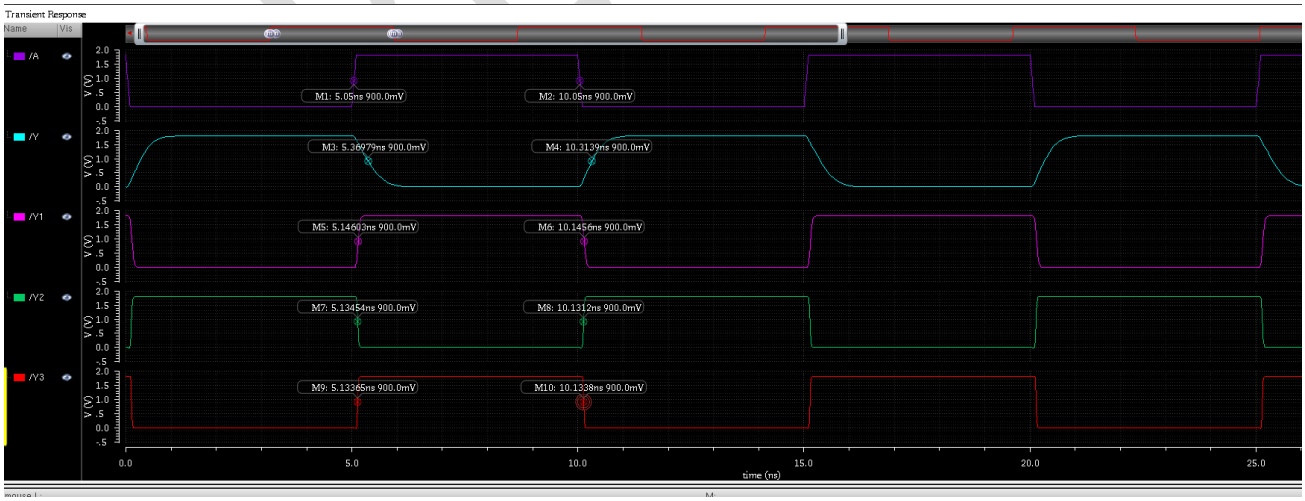


Schematic for stages of Inverters

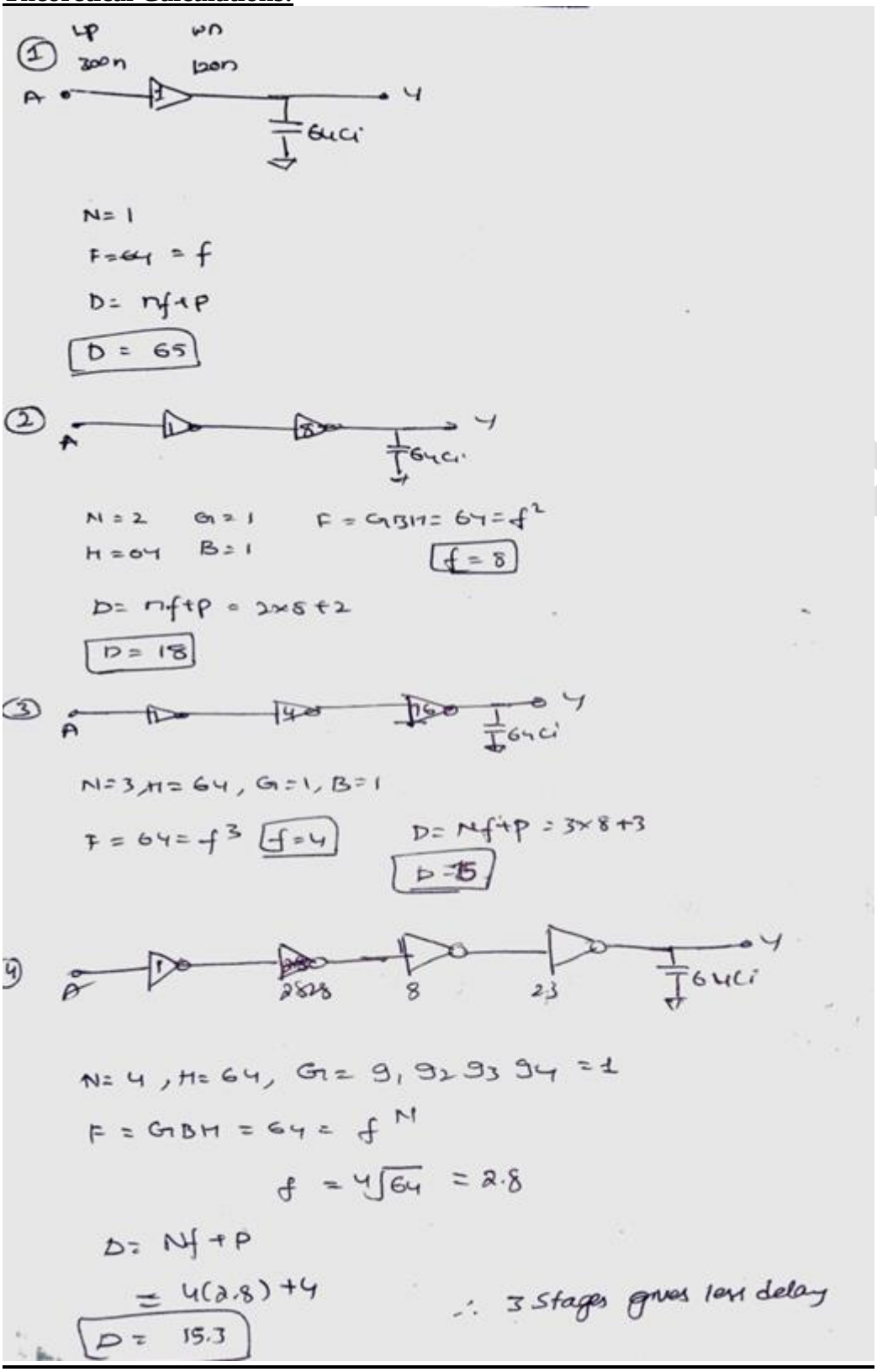


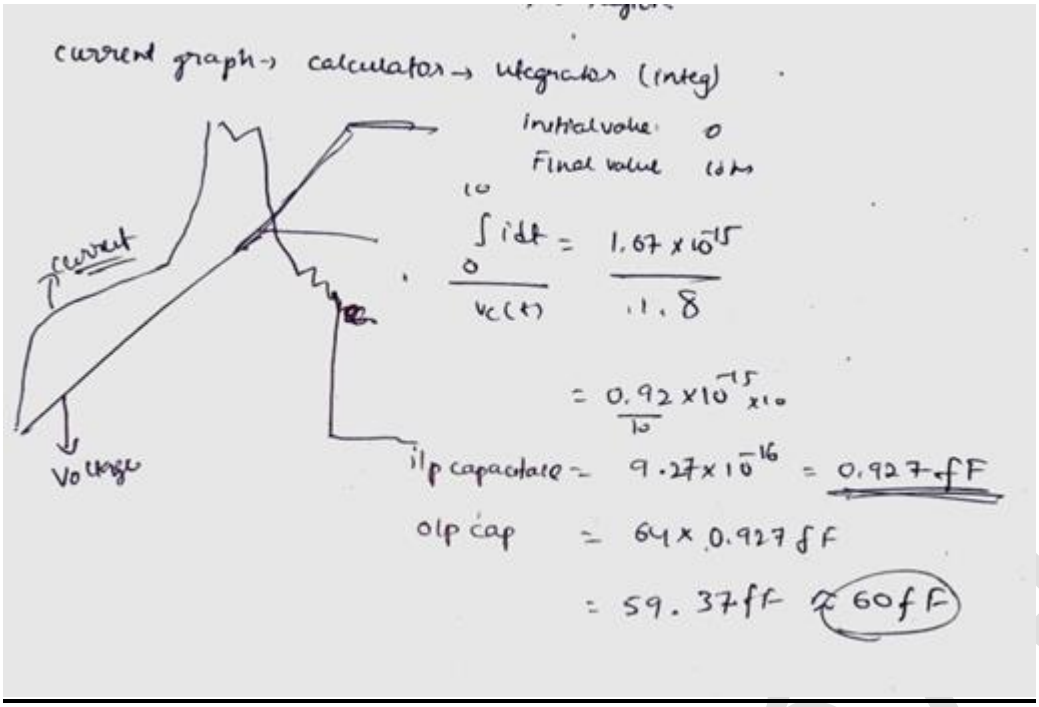


Output plot of transient analysis:



Theoretical Calculations:





Results and Analysis:

1. Input capacitance has been calculated and Cin=0.927fF.
2. Load capacitance has been calculated and Cload=60fF.
3. Symbol of NOT gate has been tested and working properly.

4. Finding delays in Stages:

No of Stages	Output Signal	T(L-H) in ns	T(H-L) in ns	Tpdr (ns)	Tpdf (ns)	Tpd avg= (Tpdr+tpdf)/2
	A	5.05	10.05			
1	Y1	5.36979	10.3139	0.31979	0.2639	0.291845
2	Y2	5.14603	10.1456	0.09603	0.0956	0.095815
3	Y3	5.13454	10.1312	0.08454	0.0812	0.08287
4	Y4	5.13365	10.1338	0.08365	0.0838	0.083725

From the above calculations we can clearly observe that three stages gives the minimum delay which matches theoretically.

******* **THANK YOU*******