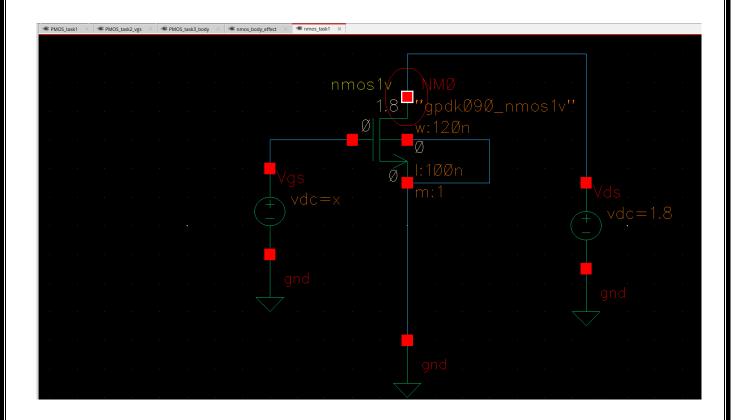
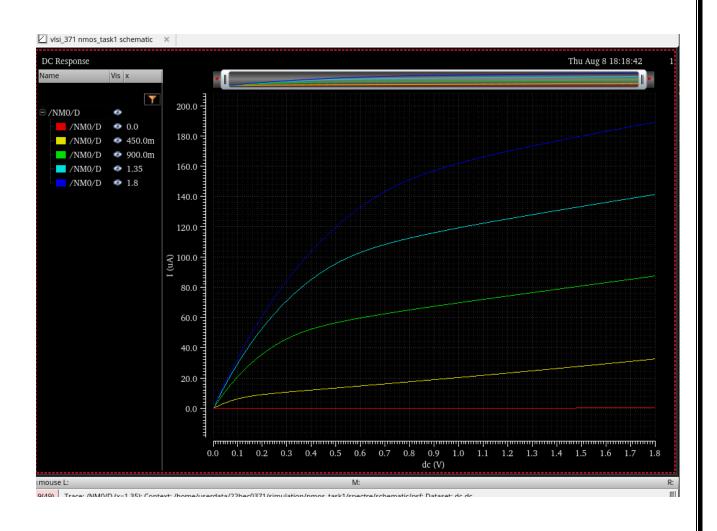
EXPERIMENT -1 N- MOSFET Characteristics

Objectives:

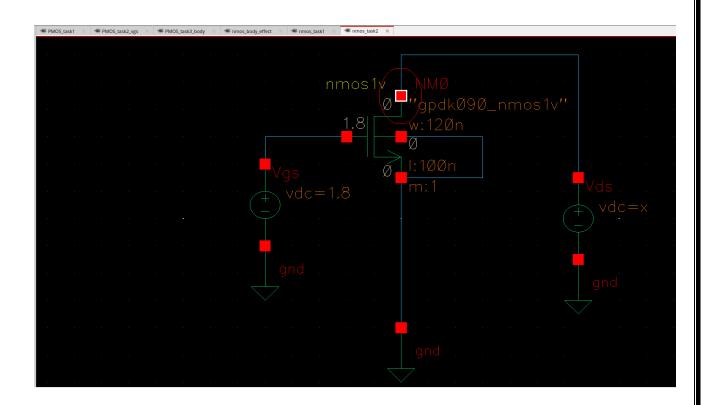
- 1. To plot the Vds-Ids (output) characteristics of NMOS transistor as a function of Vgs by parametric analysis.
 - a. Circuit diagram for obtaining output characteristics of an NMOS:



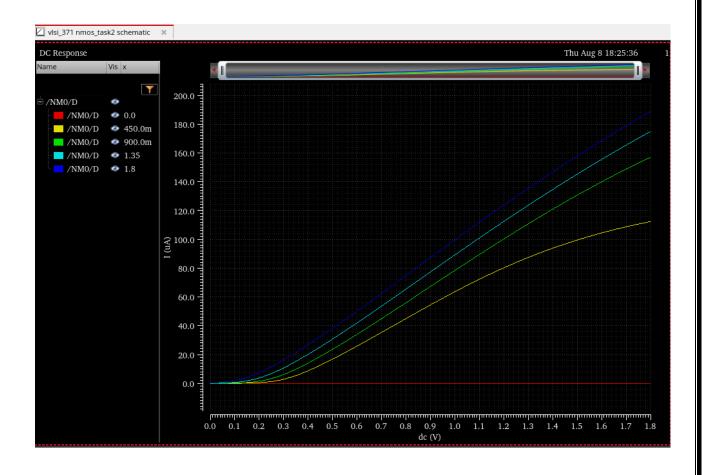
b. Plot of Ids vs Vds for change in Vgs:



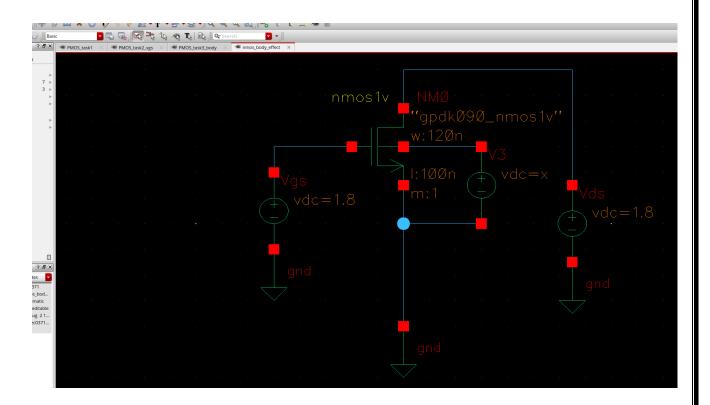
- 2. To plot the $I_D\ Vs\ V_{GS}\ \ (input)$ characteristics as a function of V_{ds} through parametric analysis.
- a. Circuit diagram for obtaining input characteristics of an NMOS:



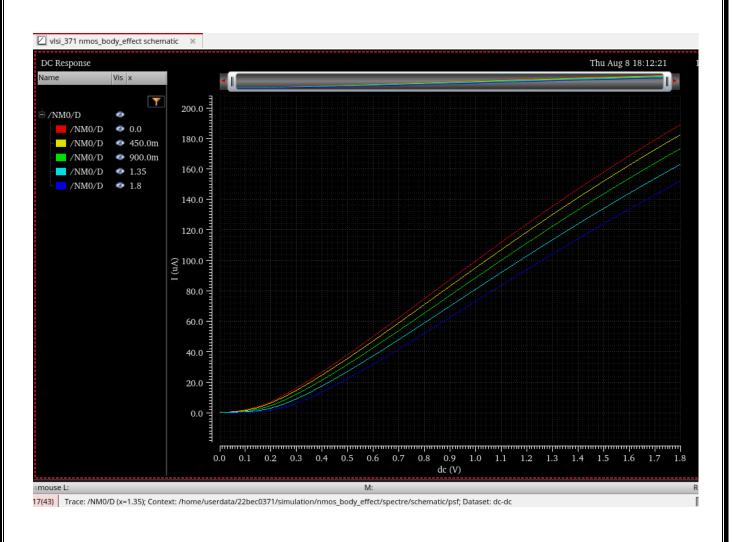
b. Plot of Ids vs Vgs for change in Vds:

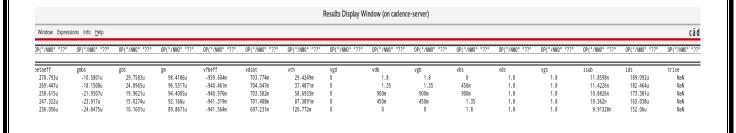


- 3. To plot the $I_D\ Vs\ V_{GS}$ curves as a function of $V_{SB}\$ and show the body effect on threshold voltage.
- a. Circuit diagram for finding the body effect of an NMOS:



b. Plot of Ids vs Vgs for change in Vbs with constant Vds=1.8v:





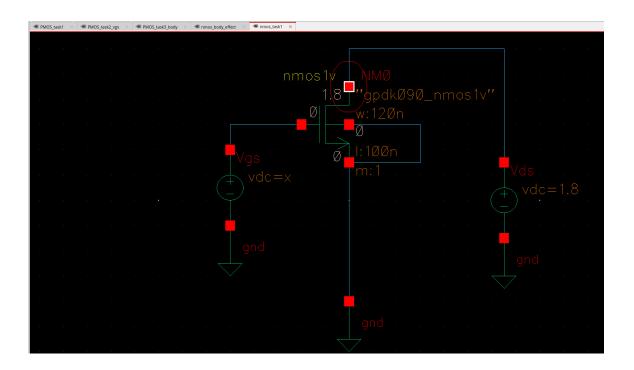
Result Analysis:

Table showing threshold voltage values for different of Vsb.

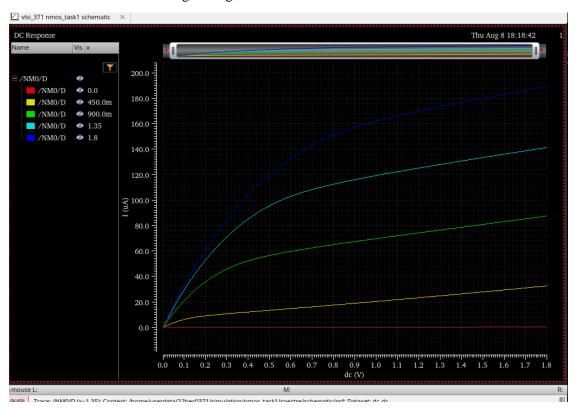
S No	V _{SB (V)}	$V_{TH}(mV)$
1.	0	29.429m
2.	450m	37.4871m
3	900m	58.6933m
4	1.35	87.3891m
5.	1.8	120.722m

By observing the above plot and table, an increase in VSB results in an increase in the threshold voltage.

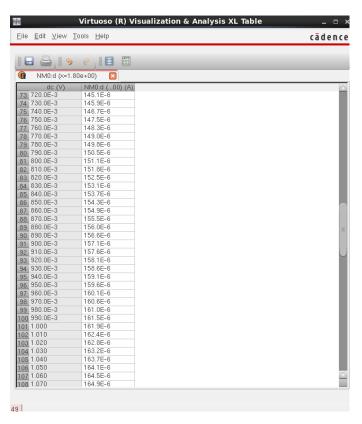
- 4. To find channel length modulation co-efficient (λ) of NMOS transistor by plotting Ids vs Vds.
- a. <u>Circuit diagram for obtaining output characteristics of an NMOS:</u>



b. Plot of Ids vs Vds for change in Vgs



c. To find channel length modulation coefficient(λ) different values of Ids and corresponding values of Vds has been printed as shown.



Ids =
$$44 \cos \frac{(495-44)^2}{L} (1+2 \cos)^2$$

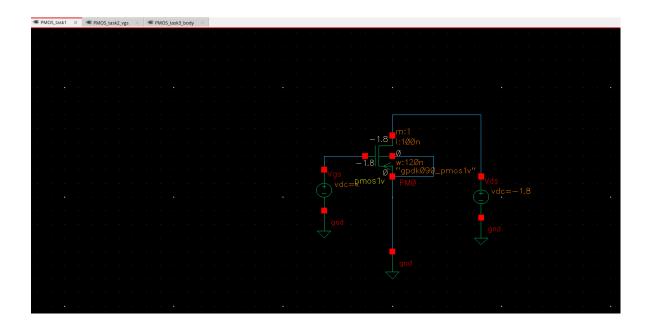
 $\frac{1}{1} \cos \frac{1+2 \cos \frac{1}{2}}{1+2 \cos \frac{1}{2}}$
 $\frac{1}{1} \cos \frac{1+2 \cos \frac{1}{$

CONCLUSION OF NMOS I-V CHARACTERISTICS:

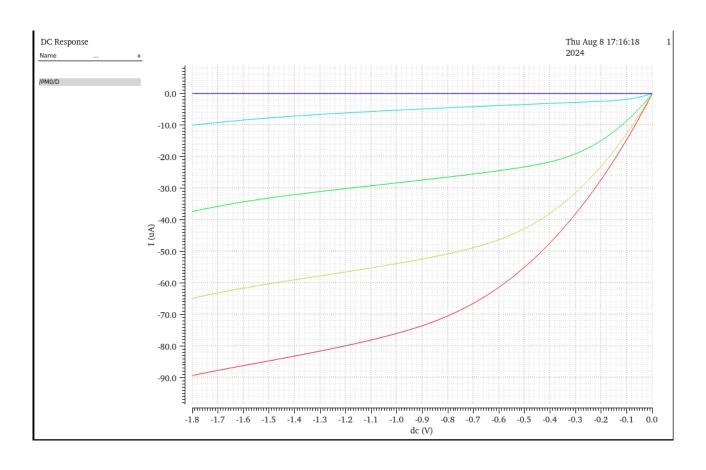
- 1. The output characteristics of NMOS was plotted
- 2. The input characteristics of NMOS was plotted.
- 3. The body effect of NMOS i.e. plot of I_G Vs V_{GS} as function of V_{SB} was also plotted and value of threshold voltage for different V_{SB} values were tabulated. The threshold value of NMOS FET at zero body bias is 29.429 mV
- 4. The channel length modulation co-efficient value (λ) for NMOS is 0.62908 **per volt.**

TASK -1 P- MOSFET Characteristics

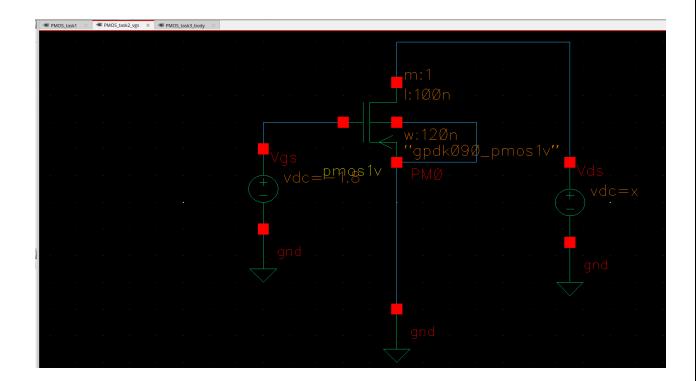
- 1. To plot the Vds-Ids (output) characteristics of PMOS transistor as a function of Vgs by parametric analysis.
- a. Circuit diagram for obtaining output characteristics of an PMOS:



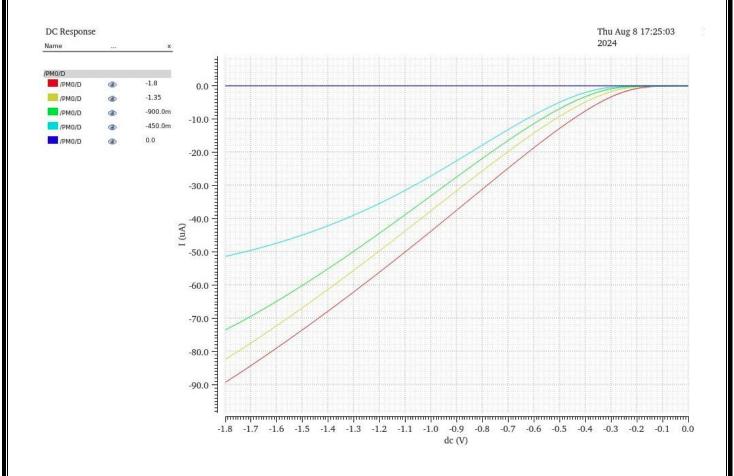
b. Plot of Ids vs Vds for change in Vgs:



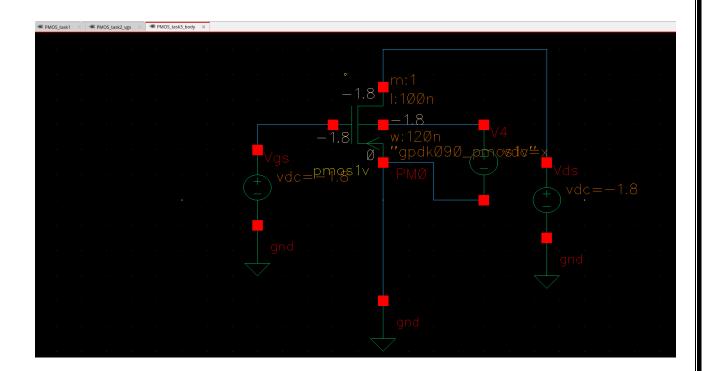
- 2. To plot the $I_D\ Vs\ V_{GS}\ \ (input)$ characteristics as a function of V_{ds} through parametric analysis.
- a. Circuit diagram for obtaining input characteristics of an PMOS:



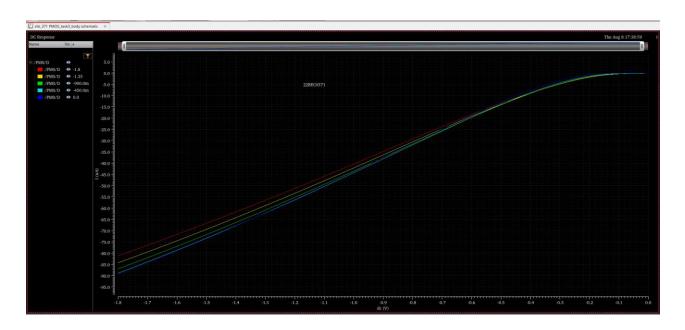
b. Plot of Ids vs Vgs for change in Vds:



- 3. To plot the $I_D\ Vs\ V_{GS}$ curves as a function of $V_{SB}\$ and show the body effect on threshold voltage.
- a. Circuit diagram for finding the body effect of an PMOS:



b. Plot of Ids vs Vgs for change in Vbs with constant Vds=-1.8v:



	Results Display Window (on cadence-server)														
Nindow Expressi	indow Expressions Info <u>H</u> elp														
P("/PMO" "??"	OP("/PMO" "??"	OP("/PMO" "??"	OP("/PMO" "??"	OP("/PMO" "??"	OP("/PWO" "??"	OP("/PMO" "??"	OP("/PMO" "??"	OP("/PNO" "??"	OP("/PMO" "??"	OP("/PMO" "??"	OP("/PWO" "??"				
	gnbs	gds	gn	vfbeff	vdsat	vth	vgd	vdb	vgb	vbs	vds	vgs	isub	ids	trise
125.513u	-6.79879u	16.9033u	46.6187u	-789.836m	-763.287m	-86.7571m	vgd 0	0	0	-1.8	-1.8	-1.8	-57.9496p	-81.1266u	NaN
125.513u 127.63u	-6.79879u -6.50392u	16.9033u 17.0357u	46.6187u 47.5885u	-789.836m -789.594m	-763.287m -785.913m	-86.7571m -98.991m	vgd 0 0	0 -450m	0 -450m	-1.8 -1.35	-1.8 -1.8	-1.8 -1.8	-57.9496p -50.2985p	-81.1266u -84.1912u	NaN NaN
125.513u 127.63u	-6.79879u	16.9033u	46.6187u	-789.836m	-763.287m	-86.7571m	vgd 0 0 0	0	0	-1.8	-1.8	-1.8	-57.9496p	-81.1266u	NaN
taeff 125.513u 127.63u 129.543u 131.053u	-6.79879u -6.50392u	16.9033u 17.0357u	46.6187u 47.5885u	-789.836m -789.594m	-763.287m -785.913m	-86.7571m -98.991m	vgd 0 0 0	0 -450m	0 -450m	-1.8 -1.35	-1.8 -1.8	-1.8 -1.8	-57.9496p -50.2985p	-81.1266u -84.1912u	NaN NaN

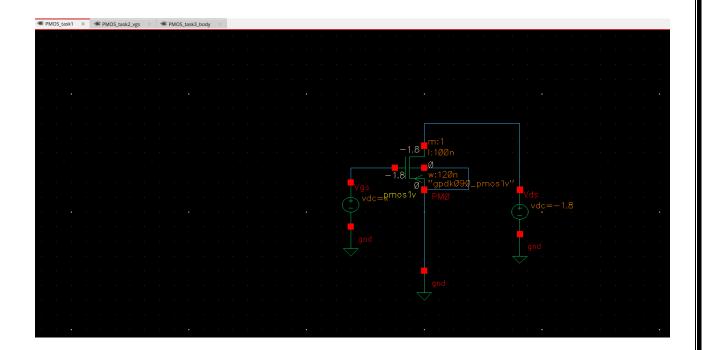
Result Analysis:

Table showing threshold voltage values for different of Vsb.

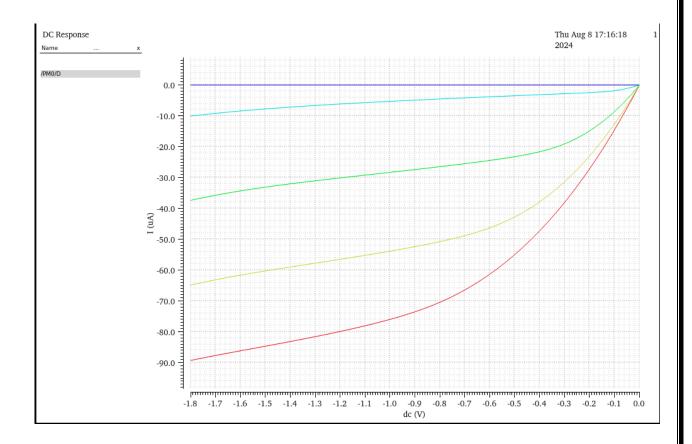
S No	$V_{\mathrm{SB}(\mathrm{V})}$	$V_{TH}(mV)$
1.	0	-86.7571m
2.	-450m	-98.991m
3	-900m	-115.256m
4	-1.35	-137.973m
5.	-1.8	-172.073m

By observing the above plot and table, an increase in VSB results in an increase in the threshold voltage.

- 4. To find channel length modulation co-efficient (λ) of PMOS transistor by plotting Ids vs Vgs.
- a. Circuit diagram for obtaining output characteristics of an PMOS:



b. Plot of Ids vs Vds for change in Vgs:



$$Td_{3} = uncox w \frac{(uq_{3}-utn)^{2}}{2} (1+\lambda vd_{3})$$

$$\frac{dd_{1}}{idd_{2}} = \frac{1+\lambda vd_{3}}{1+\lambda vd_{3}}$$

$$-83.78 \times 10^{6} = 1+\lambda (-1.440)$$

$$-88.72 \times 10^{6} = 1+\lambda (-1.764)$$

$$\lambda = -0.2466 \text{ per volt}$$

CONCLUSION OF PMOS I-V CHARACTERISTICS:

- 1. The output characteristics of PMOS was plotted
- 2. The input characteristics of PMOS was plotted.
- 3. The body effect of PMOS i.e. plot of I_G Vs V_{GS} as function of V_{SB} was also plotted and value of threshold voltage for different V_{SB} values were tabulated. The threshold value of PMOS FET at zero body bias is -86.429 mV
- 4. The channel length modulation co-efficient value (λ) for PMOS is 0.2466 **per volt.**

THANK YOU