

#11 : Performance

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CPU Clocking

The duration of a complete clock cycle is the **clock period** and the number of cycles per second is the **clock rate (or clock frequency)**, which is the inverse of the clock period.

$$\text{ClockRate (Hz)} = \frac{1}{\text{ClockPeriod (s)}}$$

Clock period (duration of a clock cycle)

- e.g., 250ps (picoseconds) = 0.25ns (nanoseconds) = $250 \times 10^{-12}\text{s}$ (seconds)

Clock rate (cycles per second)

- e.g., 4.0GHz = 4000MHz = $4.0 \times 10^9\text{Hz}$ = $1 / (250 \times 10^{-12}\text{s})$

Performance Equation

$$\begin{aligned} \text{CPUTime} &= \text{InstructionCount} \times \text{CPI} \times \text{ClockPeriod} \\ &= \frac{\text{InstructionCount} \times \text{CPI}}{\text{ClockRate}} \end{aligned}$$

Components of performance	Units of measure
CPU execution time for a program	Seconds for the program
Instruction count	Instructions executed for the program
Clock cycles per instruction (CPI)	Average number of clock cycles per instruction
Clock cycle time	Seconds per clock cycle

Cache Performance

CPU time can be divided into the clock cycles that the CPU spends executing the instructions with no misses (**CPIPerfect**) and the clock cycles that the CPU spends waiting for the memory system (**CPIStall**).

$$CPI = CPI_{Perfect} + CPI_{Stall}$$

Memory-stall clock cycles can be defined as the sum of the stall cycles coming from reads plus those coming from writes. For simplicity, let's assume that the read/write miss rates and miss penalties are the same:

$$CPI_{Stall} = \frac{MemoryAccesses}{Instructions} \times MissRate \times MissPenalty$$

Cache Performance

If we consider separate caches/memories for instructions and data then:

$$CPIStall = CPIStallInstructionAccess + CPIStallDataAccess$$

In more detail:

$$CPIStall = 1 \times MissRateInstructionAccess \times MissPenalty \\ + \frac{LoadStores}{Instructions} \times MissRateDataAccess \times MissPenalty$$

Multilevel Caches

With multilevel caches, memory-stall clock cycles can be defined as the sum of the stall cycles coming from the several cache levels (L1, L2, ...). For simplicity, let's assume single instruction/data caches:

$$\begin{aligned} CPI_{Stall} &= MissRate \times MissPenalty \\ &= MissRate_{L1} \times MissPenalty_{L1} \\ &\quad + GlobalMissRate_{L2} \times MissPenalty_{L2} + \dots \end{aligned}$$

The global miss rate for a level L represents the miss rate for the set of levels up to L:

$$\begin{aligned} GlobalMissRate_{L2} &= MissRate_{L1} \times MissRate_{L2} \\ GlobalMissRate_{L3} &= MissRate_{L1} \times MissRate_{L2} \times MissRate_{L3} \end{aligned}$$