There are multiple registers and their functions which are as follows –

Load (LD) − During the next clock pulse transition the information from the bus is transmitted to the register whose load (LD) input is enabled.

Memory Unit − When the write input of the memory is activated, it holds the content of the bus. When the read input is activated, the memory places the 16-bit output onto the bus with the selection variables being S_2S_1 S_0 = 111..

Increment (INR) and Clear (CLR) − When the INR signal is enabled, the contents of the specified register are incremented. The contents are cleared when the CLR signal is enabled.

Address Registers (AR) − The address of the memory for the next read and write operation is determined. It receives or sends an address from or to the bus when selection inputs S_2S_1 S_0=001 is used and the load is enabled. With inputs INR and CLR, the address gets incremented or cleared.

Program Counter (PC) − The address of the next instruction that is to be read from the memory is saved. It receives or sends an address from or to the bus when selection inputs S_2S_1 S_0 = 010is applied and the load input is enabled. With inputs INR and CLR, the address gets incremented or cleared.

Data Register (DR) − The data register includes the data to be written into memory or data that is to be read from the memory. It receives or sends an address from or to the bus when selection inputs are S_2S_1 S_0 = 011 applied and the load input is enabled. With inputs INR and CLR, the address gets incremented or cleared.

Accumulator (AC) − Accumulators are beneficial in executing the register micro-operations including complement, shift, etc. The results acquired are again sent to the accumulator. An accumulator stores the intermediate arithmetic and logic results.

Instruction Registers (IR) − The IR stores the copy of the instruction that the processor has to implement. The instruction that is read from the memory is stored in the IR. It receives or sends instruction code from or to the bus when selection inputs S_2S_1 S_0 = 111 are applied and the load input is enabled.

Temporary Register (TR) − The temporary storage for variables or results is supported by the temporary register. It receives or sends the temporary data from or to the bus when selection inputs S_2S_1 S_0 = 011 are applied and the load input is enabled. With inputs INR and CLR, the address gets incremented or cleared.

Input Registers (INPR) − It includes 8 bits to hold the alphanumeric input information. Input device shifts its serial data into the 8-bit register. The data is moved to AC via the adder/logic circuit with load enabled.

Output Registers (OUTPR) − The data is received from AC and moved to the output device.