Explanation of Half Adder and Full Adde Truth Table

In the combinational circuits, different logic gates are used to design encoder, multiplexer multiplexer. These circuits have some characteristics like the output of this circuit mainly levels which are there at input terminals at any time. This circuit doesn't include any mem state of the input doesn't have any influence on the current state of this circuit. The inputs combinational circuit are 'n' no. of inputs & 'm' no. of outputs. Some of the combinational adder and full adder, subtractor, encoder, decoder, multiplexer, and demultiplexer. This ar overview of half adder and full adder and it's working with truth tables.

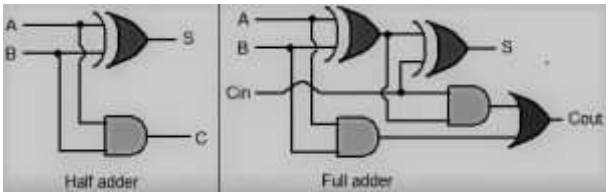
What is an Adder?

An adder is a digital logic circuit in electronics that is extensively used for the addition of computers and other types of processors, adders are even used to calculate addre activities and calculate table indices in the ALU and even utilized in other parts of the p

can be built for many numerical representations like excess-3 or binary coded dec basically classified into two types: Half Adder and Full Adder.

What is Half Adder and Full Adder Circuit?

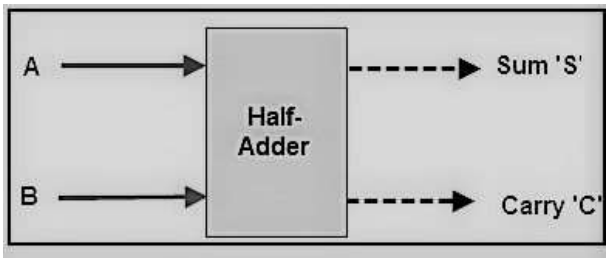
The half adder circuit has two inputs: A and B, which add two input digits and generates a The full adder circuit has three inputs: A and C, which add three input numbers and gen sum. This article gives detailed information about what is the purpose of a half adder tabular forms and even in circuit diagrams too. It is already mentioned that the main and adders is addition. Below are the detailed **half adder and full adder theory.**



Basic Half Adder and Full Adder

Half Adder

So, coming to the scenario of half adder, it adds two binary digits where the input b augend and addend and the result will be two outputs one is the sum and the other is ca sum operation, XOR is applied to both the inputs, and AND gate is applied to both inputs



HA Functional Diagram

Whereas in the full adder circuit, it adds 3 one-bit numbers, where two of the three bits as operands and the other is termed as bit carried in. The produced output is 2-bit output referred to as output carry and sum.

By using a half adder, you can design simple addition with the help of logic gates.

Let’s see an example of adding two single bits.

The 2-bit **half adder truth table** is as below:

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder Truth Table

0+0 = 0

0+1 = 1

1+0 = 1

1+1 = 10

These are the least possible single-bit combinations. But the result for 1+1 is 10, the sum re-written as a 2-bit output. Thus, the equations can be written as

0+0 = 00

0+1 = 01

1+0 = 01

1+1 = 10

The output ‘1’of ‘10’ is carry-out. ‘SUM’ is the normal output and ‘CARRY’ is the carry-out

Now it has been cleared that a 1-bit adder can be easily implemented with the help of the output ‘SUM’ and an AND Gate for the ‘Carry’.

For instance, when we need to add, two 8-bit bytes together, then it can be implement adder logic circuit. The half-adder is useful when you want to add one binary digit quantit

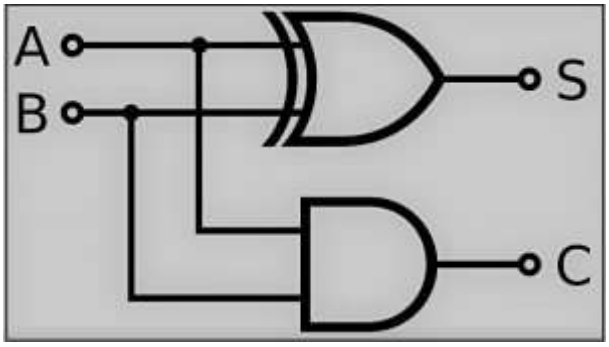
A way to develop two-binary digit adders would be to make a truth table and reduce it. make a three binary digit adder, the half adder addition operation is per twice.

when you decide to make a four-digit adder, the operation is performed one more time. was clear that the implementation is simple, but development is a time taking process.

The simplest expression uses the exclusive OR function:

Sum= A XOR B

Carry = A AND B



HA Logical Diagram

And an equivalent expression in terms of the basic AND, OR, and NOT is:

SUM=A.B+A.B'

VHDL Code For Half Adder

Entity ha is

Port (a: in STD_LOGIC;
b : in STD_LOGIC;
sha : out STD_LOGIC;
cha : out STD_LOGIC);
end ha;

Architecture Behavioral of the above circuit is

begin
sha <= a xor b ;

```
cha <= a and b ;
end Behavioral
```

Half Adder IC Number

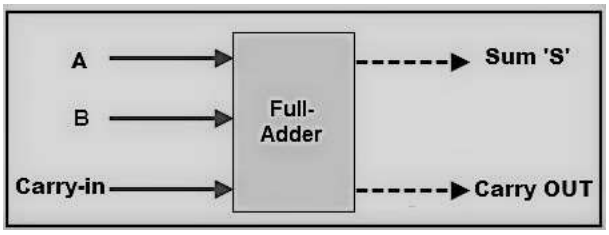
The implementation of half adder can be done through high-speed CMOS digital logic int like 74HCxx series which includes the SN74HC08 (7408) & SN74HC86 (7486).

Half Adder Limitations

The main reason to call these binary adders like Half Adders is, that there is no range to bit using an earlier bit. So, this is a main limitation of HAs once used like binary adder pa time situations which involve adding several bits. So this limitation can be overcome by u adders.

Full Adder

This adder is difficult to implement when compared to half-adder.



Full Adder Functional Diagram

The difference between a half-adder and a full-adder is that the full-adder has thre outputs, whereas half adder has only two inputs and two outputs. The first two inputs ar third input is an input carry as C-IN. When a full-adder logic is designed, you string eigh to create a byte-wide adder and cascade the carry bit from one adder to the next.

INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

FA Truth Table

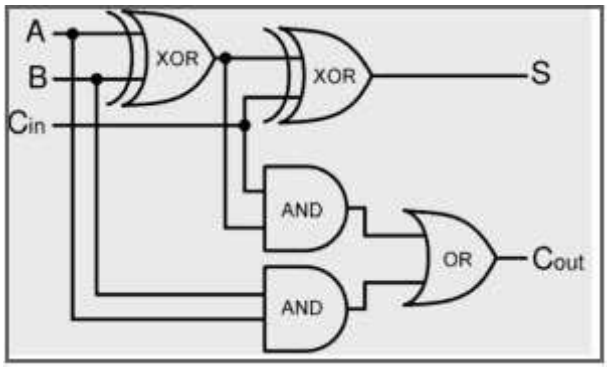
The output carry is designated as C-OUT and the normal output is represented as S whic

With the above **full adder truth-table**, the implementation of a full adder circuit can be The SUM 'S' is produced in two steps:

1. By XORing the provided inputs 'A' and 'B'
2. The result of A XOR B is then XORed with the C-IN

This generates SUM and C-OUT is true only when either two of three inputs are HIGH, th will be HIGH. So, we can implement a full adder circuit with the help of two half adder circ half adder will be used to add A and B to produce a partial Sum and a second-half adder to add C-IN to the Sum produced by the first half adder to get the final S output.

If any of the half adder logic produces a carry, there will be an output carry. So, C-O function of the half-adder Carry outputs. Take a look at the implementation of the full a below.



Full Adder Logical Diagram

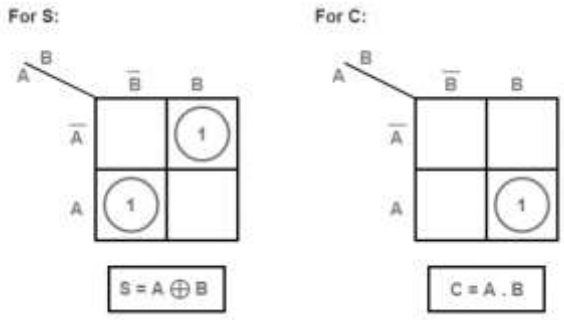
The implementation of larger logic diagrams is possible with the above full adder logic a mostly used to represent the operation. Given below is a simpler schematic representati adder.

With this type of symbol, we can add two bits together, taking a carry from the ne magnitude, and sending a carry to the next higher order of magnitude. In a compu operation, each bit must be represented by a full adder and must be added simultaneo two 8-bit numbers, you will need 8 full adders which can be formed by cascading two of t

Half Adder and Full Adder using K-Map

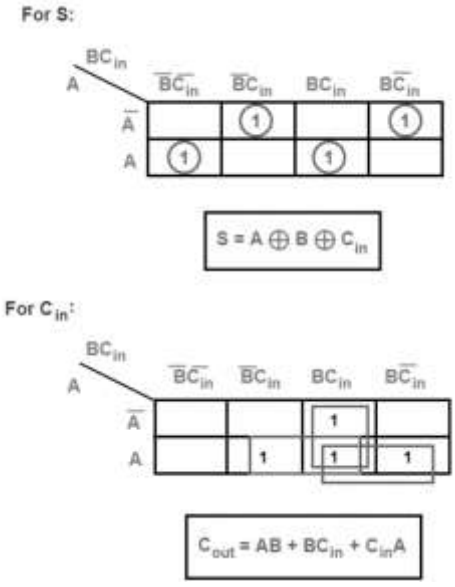
Even the sum and carry outputs for half adder can also be obtained with the method of K map). The **half adder and full adder boolean expression** can be obtained through K-m map for these adders is discussed below.

The half adder K-map is



HA K-Map

The full adder K-Map is



FA K-Map

Logical Expression of SUM and Carry

The logical expression of sum (S) can be determined based on the inputs mentioned in tl

= A'B'Cin + A' B CCin' + A B'Cin'+ AB Cin

= Cin (A'B'+ AB) + Cin' (A'B +A B')

$$= Cin\ EX\text{-}OR\ (A\ EX\text{-}OR\ B)$$

$$= (1,2,4,7)$$

The logical expression of the carry (Cout) can be determined based on the inputs mentio

$$= A'B\ Cin + AB'Cin + AB\ Cin' + ABCin$$

$$= AB + BCin + ACin$$

$$= (3, 5, 6, 7)$$

With the above-mentioned truth tables, the results can be obtained and the procedure is

A combinational circuit combines the different gates in the circuit where those can be an multiplexer and demultiplexer. The characteristics of combinational circuits are as follows

- The output at any instant of time is based only on the levels that are present at input te
- It does not use any memory. The previous state of input does not have any effect on th the circuit.
- It can have any number of inputs and m number of outputs.

VHDL Coding

VHDL coding for full adder include the following.

```
entity full_add is

Port ( a : in  STD_LOGIC;
b : in  STD_LOGIC;
cin : in  STD_LOGIC;
sum : out  STD_LOGIC;
cout : out  STD_LOGIC);
end full_add;

Architecture Behavioral of full_add is
```

```
component ha is
Port ( a : in  STD_LOGIC;
b : in  STD_LOGIC;
sha : out  STD_LOGIC;
cha : out  STD_LOGIC);
end component;
signal s_s,c1,c2: STD_LOGIC ;
begin
HA1:ha port map(a,b,s_s,c1);
HA2:ha port map (s_s,cin,sum,c2);
cout<=c1 or c2 ;
end Behavioral;
```

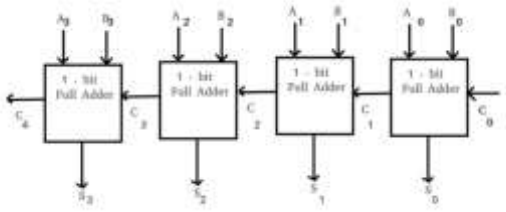
The **difference between half adder and full adder** is that half adder produces results a half adder to produce some other result. Similarly, while the Full-Adder is of two Half Adder is the actual block that we use to create the arithmetic circuits.

Carry Lookahead Adders

In the concept of ripple carry adder circuits, the bits that are necessary for addition are im available. Whereas every adder section needs to hold its time for the arrival of carry from adder block. Because of this, it takes more time to produce SUM and CARRY as each se waits for the arrival of input.

For instance, to deliver output for the nth block, it needs to receive input from (n-1)th bloc is correspondingly termed as propagation delay.

To overcome the delay in ripple carries adder, a carry-lookahead adder was introduced. H complicated hardware, the propagation delay can be minimized. The below diagram sho lookahead adder using full adders.



Carry Lookahead Using Full Adder

The truth table and corresponding output equations are

A	B	C	C+1	Cor
0	0	0	0	No
0	0	1	0	Ge
0	1	0	0	
0	1	1	1	No
1	0	0	0	Pro
1	0	1	1	
1	1	0	1	C
1	1	1	1	Ge

The carry propagates equation is Pi = Ai XOR Bi and the carry generate is Gi = Ai*Bi. Wit equations, the sum and carry equations can be represented as

SUM = Pi XOR Ci

Ci+1 = Gi + Pi*Ci

Gi delivers carry only when both the inputs Ai and Bi are 1 without considering the input to the carry propagation from Ci to Ci+1.

Difference between Half Adder and Full Adder

The **difference between the half adder and full adder table** is shown below.

Half Adder	Full Adder
Half Adder (HA) is a combinational logic circuit and this circuit is used to add two one-bit digits.	Full Adder (FA) is a combinational c circuit is used to add three one bit c
In HA, once the carry is generated from the previous addition cannot be added to the next step.	In FA, once the carry is generated f addition, then it can be added to the
Half adder includes two logic gates like AND gate and EX-OR gate.	Full adder includes two EX-OR gate and two AND gates.
The input bits in the half adder are two like A, B.	The input bits in the full adder are t C-in
Half adder sum and carry equation is S = a⊕b ; C = a*b	Full adder logic expression is S = a ⊕ b⊕Cin; Cout = (a*b) + (C
HA is used in computers, calculators, devices used for digital measuring, etc.	FA is used in digital processors, mu etc.

The **key differences between the half adder and full adder** are discussed below.

- Half adder generates sum & carry by adding two binary inputs whereas the full adder i generate sum & carry by adding three binary inputs. Both the half adder and full adder architecture is not the same.
- The main feature that differentiates HA & FA is that in HA there is no such deal to cons addition carry like its input. But, a FA locates a particular input column like Cin to consi addition's carry bit.
- The two adders will show a difference based on the components used in the circuit for The half adders (HA's) are designed with the combination of two logic gates like AND & the FA is designed with the combination of three AND, two XOR & one OR gates.
- Basically, HA's operate on 2-two inputs of 1-bit, whereas the FA's operate on three inpu adder is used in different electronic devices for evaluating the addition whereas the ful digital processors for the addition of a long bit.
- The similarities in these two adders are, both the HA & FA are combinational digital cir not use any memory element such as sequential circuits. These circuits are essential f operation to provide the addition of the binary number.

Full Adder Implementation using Half Adders

The implementation of a FA can be done through two half adders which are connected lo
diagram of this can be shown below which tells the connection of a FA using two half adc
The sum and carry equations from previous calculations are

$$S = A' B' Cin + A' BC' in + ABCin$$

$$Cout = AB + ACin + BCin$$

The sum equation can be written as.

$$Cin (A'B' + AB) + C' in (A'B + A B')$$

So, Sum = Cin EX-OR (A EX-OR B)

$$Cin (A \text{ EX-OR } B) + C'in (A \text{ EX-OR } B)$$

$$= Cin \text{ EX-OR } (A \text{ EX-OR } B)$$

Cout can be written like the following.

$$COUT = AB + ACin + BCin.$$

$$COUT = AB + ACin + BCin (A + \overline{A})$$

$$= ABCin + AB + ACin + A' B Cin$$

$$= AB (1 + Cin) + ACin + A' B Cin$$

$$= A B + ACin + A' B Cin$$

$$= AB + ACin (B + B') + A' B Cin$$

$$= ABCin + AB + A'B Cin + A' B Cin$$

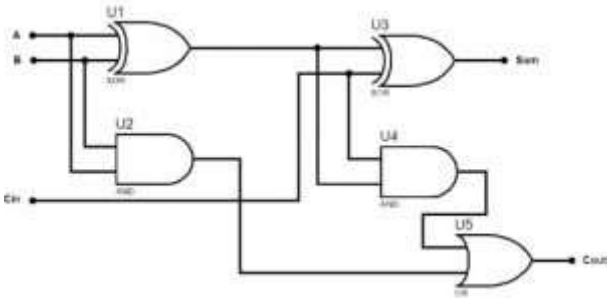
$$= AB (Cin + 1) + A B Cin + A' B Cin$$

$$= AB + AB' Cin + A' B Cin$$

$$= AB + Cin (AB' + A'B)$$

$$\text{Therefore, COUT} = AB + Cin (A \text{ EX-OR } B)$$

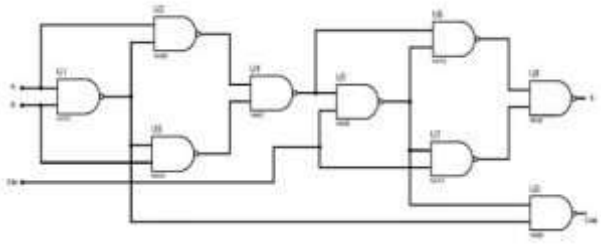
Depending on the above two sums & carry equations, the FA circuit can be implemented two HAs & an OR gate. The circuit diagram of a full adder with two half adders is illustrate



Full Adder using Two Half Adders

Full Adder Design with using NAND Gates

A NAND gate is one kind of universal gate, used to execute any kind of logic design. The the NAND gates diagram is shown below.



FA using NAND Gates

FA is an easy one-bit adder and if we desire to execute the addition of n-bit, then n no. of be employed in the cascade connection format.

Advantages

The **advantages of half adder and full adder** include the following.

- The foremost purpose of a half adder is to add two single-bit numbers
- Full adders hold the ability to add a carry bit which is the resulting from the previous ac
- With full adder, crucial circuits such as adder, multiplexer, and many others can be imp
- The full adder circuits consume minimal power
- The advantages of a full adder over a half adder are, a full adder is used to overcome half adder because; half adder is mainly used to add two 1-bit numbers. Half adders d bit, so to overcome this full adder is employed. In Full adder, the addition of three bits generates two outputs.
- Designing of adders is simple and it is a basic building block so that one-bit addition ca understood.
- This adder can be converted to half subtractor by adding an inverter.
- By using a full adder, high output can be obtained.
- High speed
- Very strong to supply voltage scaling

Disadvantages

The **disadvantages of half adder and full adder** include the following.

- In addition, half adder cannot use before carrying, so it is not applicable for cascading multi-bit.
- To overcome this drawback, FA is necessary to add three 1 bit.
- Once the FA is used in the form of a chain like a RA (Ripple Adder), then the drive cap can be decreased.

Applications

The applications of half adder and full adder include the following.

- The binary bits addition can be done by half adder using ALU within the computer beca adder.
- Half adder combination can be used for designing a full adder circuit.
- Half adders are used in the calculators and to measure the addresses as well as table
- These circuits are used to handle different applications within digital circuits. In the futu role in digital electronics.
- A FA circuit is used as an element in many large circuits such as Ripple Carry Adder. T the number of bits simultaneously.

- FAs are used in Arithmetic Logic Unit (ALU)
- FAs are used in graphics-related applications like GPU (Graphics Processing Unit)
- These are used in the multiplication circuit to execute Carryout Multiplication.
- In a computer, to generate the memory address & to build the program counterpoint to instruction, the Arithmetic Logic Unit is used by using Full Adders.

Thus, whenever the addition of two binary numbers is done then the digits are added at f This process can be performed through a half adder because the simplest n/w that allows numbers. The inputs of this adder are the binary digits whereas the outputs are the sum ((C).

Whenever the number of digits is included, then the HA network is utilized simply to conn digits, as the HA cannot add the carry number from the earlier class. A full adder can be c base of all digital arithmetic devices. This is used for adding three 1-digit numbers. This a three inputs like A, B, and Cin whereas the outputs are Sum and Cout.

Related Concepts

The **concepts related to half adder and full adder** just not stick to a single purpose. Th extensive usage in many applications and a few of the related are mentioned :

- Half adder and full adder IC number
- Development of 8-bit adder
- What are the half adder precautions?
- JAVA Applet of a Ripple Carry Adder

Therefore, this is all about the **half adder and full adder theory** along with the truth diagrams, the design of full adder using half adder circuit is also shown. Many of the **h adder pdf** documents are available to provide advanced information of these concepts important to know **how a 4-bit full adder is implemented?**

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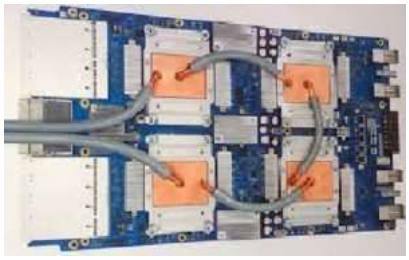

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