The basic computer has

1. eight registers,
2. a memory unit, and
3. a control unit.

- Paths must be provided to **transfer information from one register to another and between memory and registers**. The number of wires will be excessive if connections are made between the outputs of each register and the inputs of the other registers. A more efficient scheme for transferring information in a system with many registers is to use a common bus. We can construct a bus system **using multiplexers or three-state buffer gates**. We just have to connect the **registers and memory** of the basic computer to a common bus system.
- The **outputs of seven registers and memory are connected to the common bus**. The specific output that is selected for the bus lines at any given time is determined from the binary value of the selection variables S2, S1, and S0. The number along each output shows the decimal equivalent of the required binary selection. **For example**, the number along the output of DR is 3. The 16-bit outputs of DR are placed on the bus lines when S2S1S0 = 011 since this is the binary value of decimal 3.
- The **lines from the common bus are connected to the inputs of each register and the data inputs of the memory.** The particular register whose **LD** (**load**) input is enabled receives the data from the bus during the next clock pulse transition. The memory receives the contents of the bus when its write input is activated. The memory places its 16-bit output onto the bus when the read input is activated and S2S1S0 = 111.

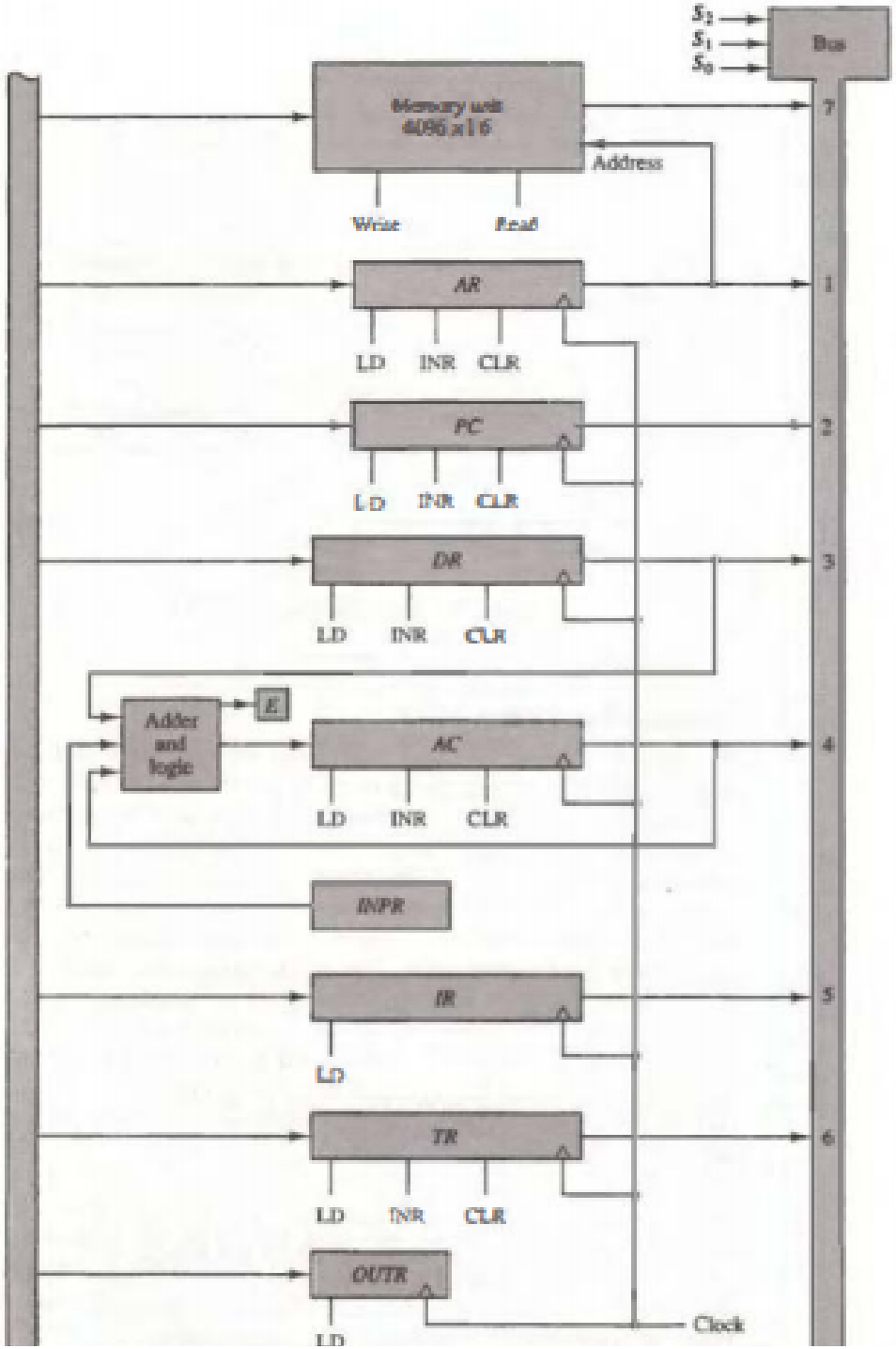
S_2
S_1
S_0
Bus
Memory unit
4096 x 16
Address
Write
Read
AR
LD INR CLR
PC
LD INR CLR
DR
LD INR CLR
Adder and logic
E
AC
LD INR CLR
INPR
IR
LD
TR
LD INR CLR
OUTR
LD
Clock
7
1
2
3
4
5
6

Figure 5-4 Basic computer registers connected to a common bus.

- Four registers, **DR, AC, IR, and TR**, have 16 bits each. Two registers, AR and PC, have 12 bits each since they hold a memory address. When the contents of AR or PC are applied to the 16-bit common bus, the four most significant bits are set to O's. When AR or PC receive information from the bus, only the 12 least significant bits are transferred into the register.
- The input register INPR and the output register **OUTR have 8 bits each and communicate** with the eight least significant bits in the bus. INPR is connected to provide information to the bus but OUTR can only receive information from the bus. This is because **INPR receives a character from an input device which is then transferred to AC** .
- OUTR receives a character from AC and delivers it to an output device. There is no transfer from OUTR to any of the other registers.
- The **16 lines of the common bus receive information from six registers and the memory unit**. The bus lines are connected to the inputs of six registers and the memory. Five registers have three control inputs: **LD** (load), **INR** (increment), and **CLR** (clear). This type of register is equivalent to a binary counter with parallel load and synchronous. The increment operation is achieved by enabling the count input of the counter. Two registers have only a LD input.
- The input data and output data of the memory are connected to the common bus, but the **memory address is connected to AR** . Therefore, AR must always be used to specify a memory address. By using a single register for the address, we eliminate the need for an address bus that would have been needed otherwise. The content of any register can be specified for the memory data input during a write operation. Similarly, any register can receive the data from memory after a read operation except AC .
- The 16 inputs of AC come from an adder and logic circuit. **This circuit has three sets of inputs**. One set of 16-bit inputs come from the outputs of AC . They are used to implement register rnlcrooperations such as complement AC and shift AC . Another set of 16-bit inputs come from the data register DR . **The inputs from DR and AC are used for arithmetic and logic microoperations**, such as add DR to AC or AND DR to AC . The result of an addition is transferred to AC and the end carry-out of the addition is transferred to flip-flop E (Extended AC bit). A third set of 8-bit inputs come from the input register INPR.
- Note that the content of any register can be applied onto the bus and an **operation can be performed in the adder and logic circuit during the same clock cycle**. The clock transition at the end of the cycle transfers the content of the bus

into the designated destination register and the output of the adder and logic circuit into AC . For example, the two microoperation.

DR<---AC and AC <--DR

can be executed at the same time. This can be done by placing the content of AC on the bus (with S2S1S0 = 100), enabling the LD (load) input of DR, transferring the content of DR through the adder and logic circuit into AC, and enabling the LD (load) input of AC, all during the same clock cycle. The two transfers occur upon the arrival of the clock pulse transition at the **end of the clock cycle**.