VLSI Implementation of a Neuromorphic System for Pattern Recognition Using Spike-Based Learning

Sakib Hasan Mitul
A.M. Nazmus Sadat
Depertment of EEE East West University
Date: 10th November 2024

Simulations And results:

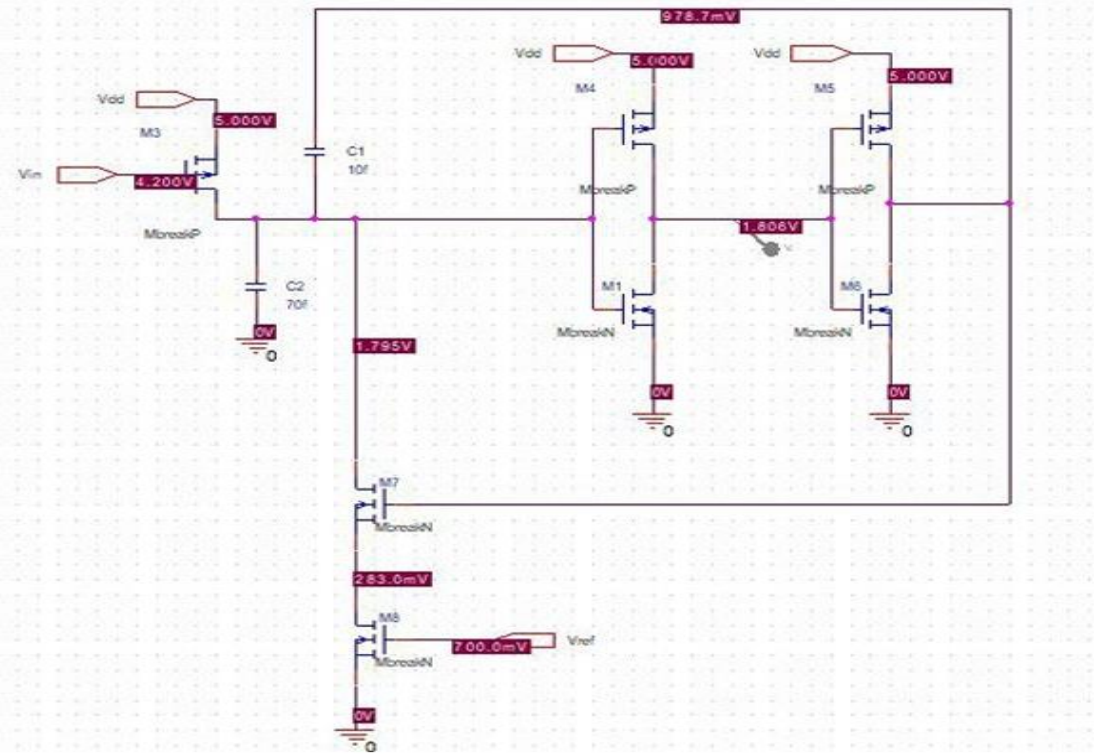


Figure 1: Integrate and fire neuron as ganglion cell

Components:

1. Voltage Sources:

- Vdd: Power supply
- Vin: Acts as the input signal for the differential amplifier
- Vref: Reference voltage for comparison

2. Capacitors:

- C1: Used for stability or frequency compensation
- C2: Used for stability or filtering

3. Observed Node Voltages:

- Node before M3: Voltage at the top left of the circuit
- Node before M1 and M6: Common source voltage for the differential pair
- Output Nodes: Voltages observed at the output branches near M1 and M6
- Other notable voltages: Voltage between M7 and

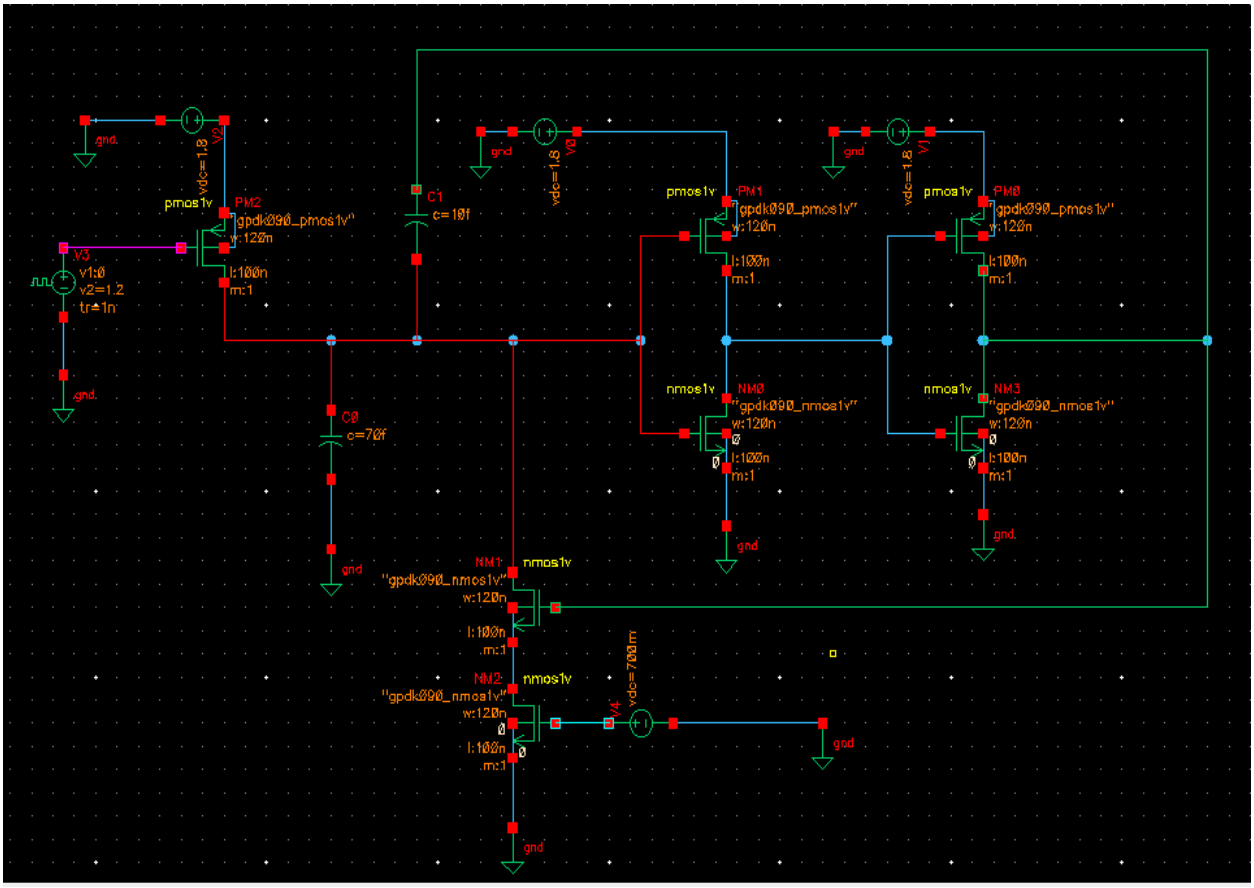


Figure 2: Neuron schematic circuit

All the **MOSFETs** have been used in the circuit share the same parameters as **the lengths** are **100nm** and **widths 120nm.**

This circuit is an **integrate-and-fire neuron model** that mimics the way biological neurons accumulate signals and produce a spike when a certain threshold is reached. It consists of multiple stages that handle different aspects of the integration and firing process, allowing it to replicate the behavior of a neuron.

Key Components and Stages

1. **Input Stage (NM0, NM1):**
    - The differential pair (NMOS transistors NM0 and NM1) compares input signals, converting their voltage difference into a differential current that is fed to the next stage.

2. **PMOS Load (PM0, PM1):**
    - This stage uses PMOS transistors to form a current mirror load for the differential pair. It converts the differential current from the input stage into a corresponding voltage signal.
3. **Current Mirror (PM2, PM3):**
    - Provides a stable current to the differential pair, ensuring balanced operation and enhancing the circuit's gain.

4. **Biasing (NM3):**
    - Controls the current through the differential pair, setting the circuit's operating point and ensuring that the circuit responds accurately to input variations.
5. **Capacitors (C1 and C2):**
    - C1 serves as the main integrator, accumulating charge over time based on the input signal, like a neuron's membrane potential.
    - C2 is used for frequency compensation, enhancing stability, and handling reset after a spike.
6. **Voltage Sources (Vdd and Vss):**
    - Provide power (Vdd) and ground (Vss) to the circuit, establishing the necessary operating conditions.

Circuit Operation

- **Integration:** When an input voltage (Vin) is applied, it charges C1 through the differential pair, representing the gradual accumulation of inputs. This continues until the voltage across C1 reaches a specific threshold.
- **Threshold Firing:** Once the voltage across C1 reaches a threshold, the transistors trigger a discharge, generating a spike or "action potential," mimicking the firing behavior of a biological neuron.
- **Reset:** After the spike, C1 discharges, allowing the circuit to reset and prepare to integrate the next signal.

Biological Analogies

This circuit effectively replicates the integrate-and-fire behavior of a neuron. Capacitor C1 acts like a neuron's membrane, accumulating charge until it reaches a threshold, which then triggers an action potential. After firing, the circuit resets, ready to accumulate new input signals.

This architecture, with differential input, current mirrors, and biasing, ensures stability and precision, making it a reliable model of a neuron's signal integration and firing mechanism.

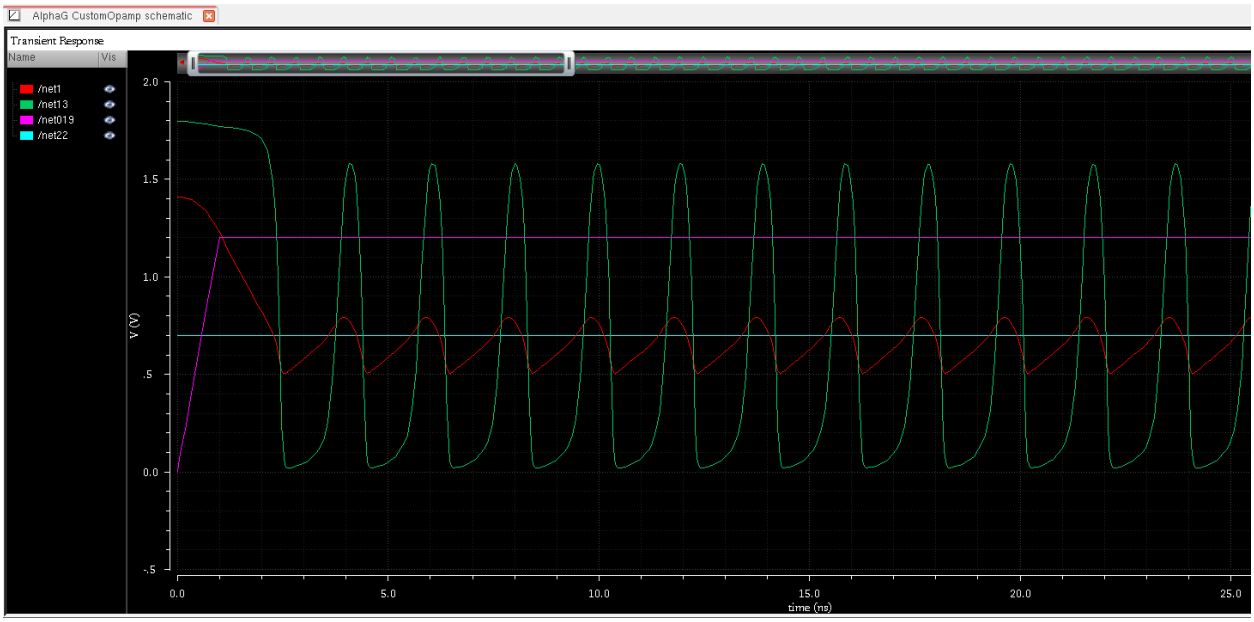


Figure 3: Transient Response of Vmem, Vout, Vin, and Vthr

- **Vmem (Red Curve):** Vmembrane voltage across capacitance which crosses the threshold voltage and resulting the spike.
- **Vout (Green Curve):** The output voltage exhibits a periodic waveform with peaks and troughs, showing the amplified response to Vin.
- **Vref (Purple Curve):** The constant reference voltage, Vref, provides a baseline for Vin comparison, allowing differential signal processing.
- **Vin (Cyan Curve):** The input voltage, Vin, initially rises and then oscillates, driving the circuit response.

- **Differential Amplification:** The circuit amplifies the difference between Vin and Vref, producing a waveform at the output that mirrors input oscillations.
- **Stability:** Vref and Vdd ensure the circuit operates reliably, keeping the output accurately aligned with the input signal changes.

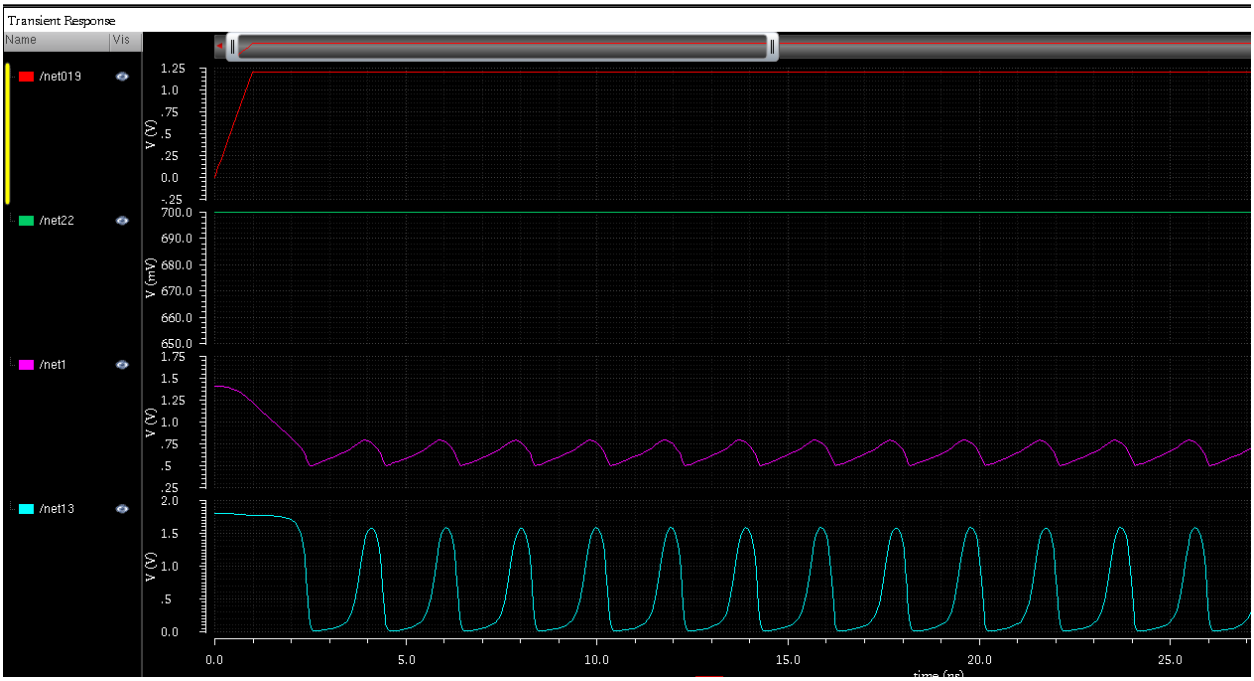


Figure 4: Transient Response of Differential Amplifier with Input, Reference, and Output Signals

- ✓ **Input Signal (Red Curve /net019):** Quickly rises to ~1.8V, indicating circuit initialization and steady-state achievement.
- ✓ **Reference Voltage (Green Curve /net22):** Stable at ~700mV, acting as a Vref baseline to set thresholds and control output response.
- ✓ **Intermediate Signal (Magenta Curve /net1):** Shows a periodic waveform oscillating between 0.7V and 1.3V, modulating with changes in the input.
- ✓ **Main Output (Cyan Curve /net13):** Oscillates between 0V and 2V, representing amplified response linked to the input signal and modulated by Vref.
- ✓ **Overall Behavior:** Input signal initiates oscillations in output signals, with the reference voltage helping maintain consistent periodic output patterns, indicative of an oscillatory or differential amplifier system.

Power Calculation for Vdd and the Generated Current (Id):

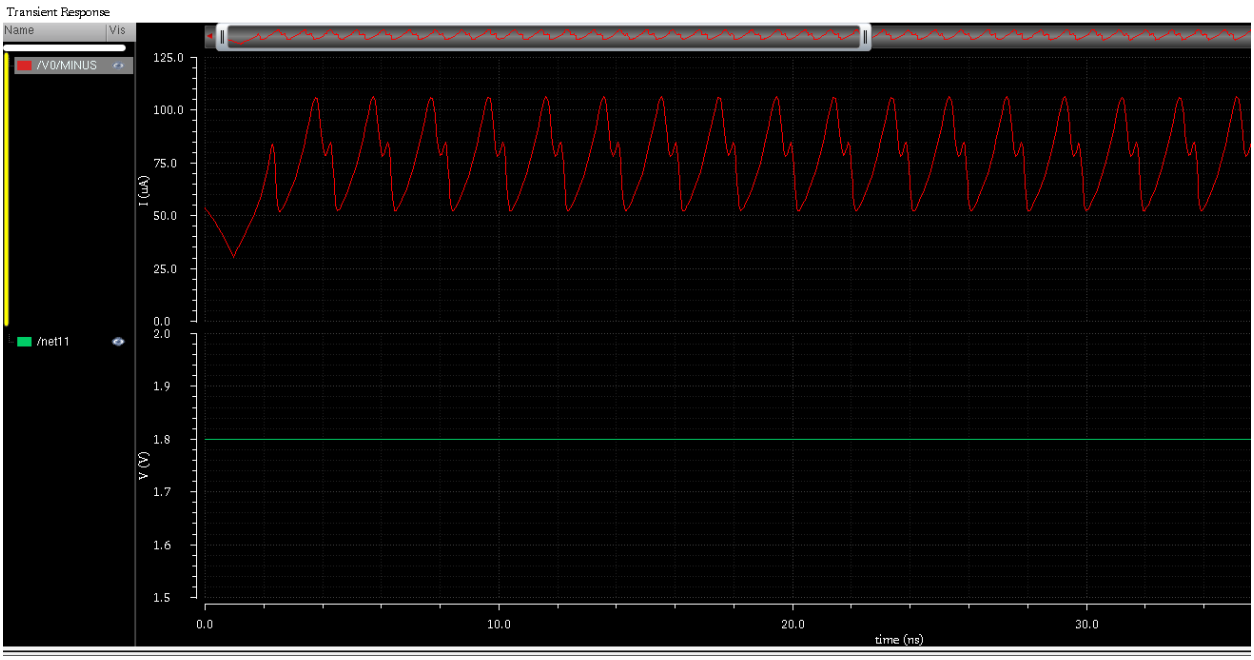
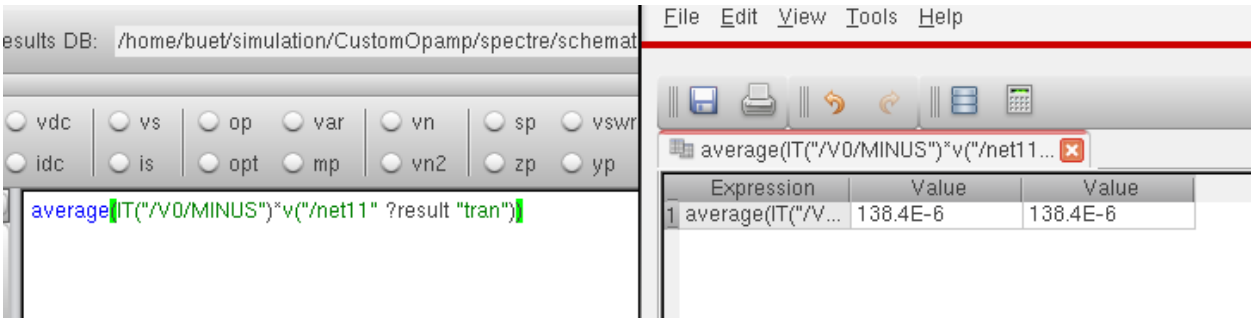


Figure 5: Transient Response of Current and Voltage in a Switching Circuit

- ✓ **Current Oscillations:** The red current curve (III) oscillates between 25 µA and 125 µA, likely indicating periodic charging/discharging or switching events.
- ✓ **Voltage Stability:** The green voltage curve (VVV) remains stable at approximately 1.8V, suggesting a steady-state DC supply unaffected by current fluctuations.
- ✓ **Periodic Current Behavior**: The circuit's current spikes periodically, possibly due to an active switching component or regulator behavior.
- ✓ **Constant Voltage Support:** A stable voltage source supports a load drawing a varying current without impacting the supply stability.



Average power(i) = 138.4 uW

-

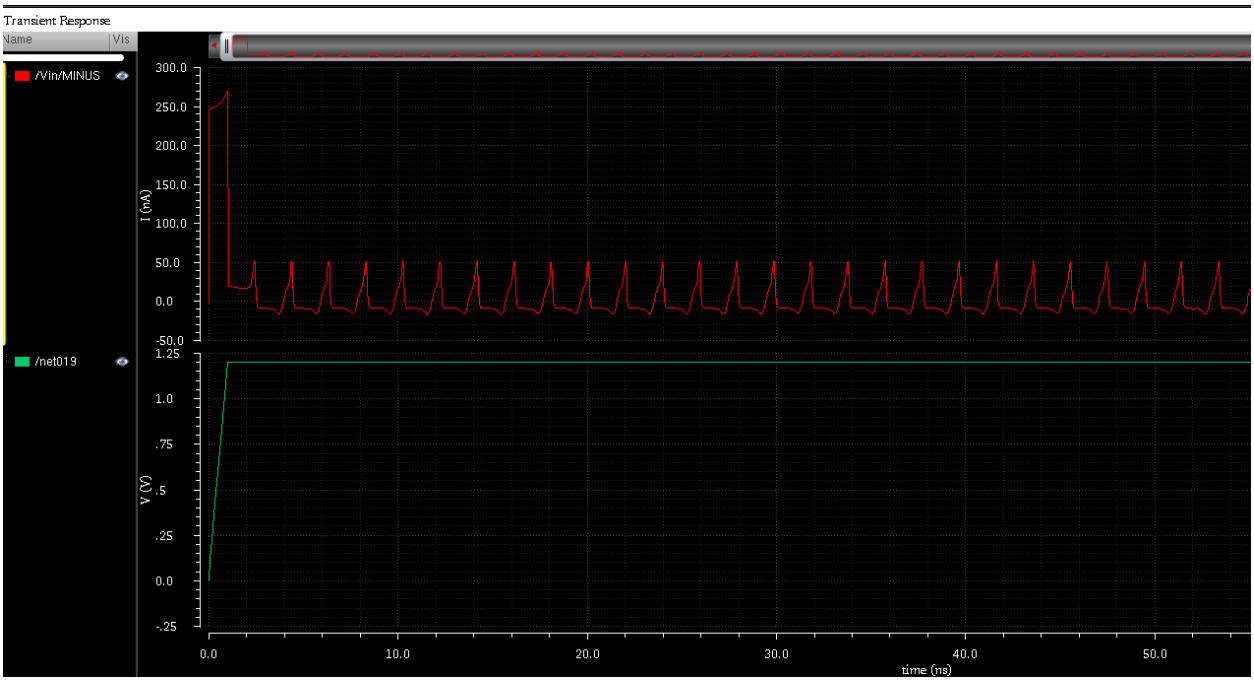
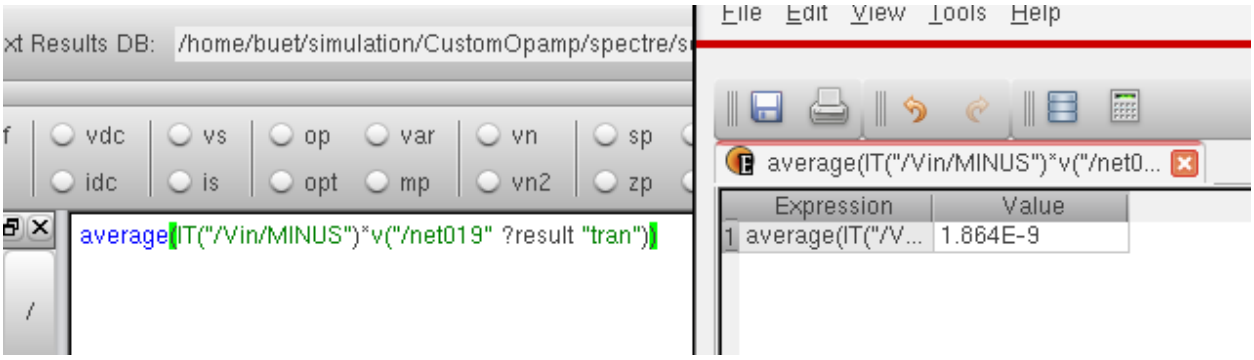


Figure 6: For Vin and generated current

- ✓ **Current Inrush (III, Red Curve):** Initially peaks around 250 mA before dropping.
- ✓ **Current Oscillation:** Settles into periodic spikes between 0 mA and 100 mA, suggesting a pulsed or switched load behavior.
- ✓ **Voltage Rise (VVV, Green Curve):** Quickly reaches 1.25 V and stabilizes, indicating a steady DC operating voltage.
- ✓ **Overall Response:** The circuit shows an initial high inrush current with subsequent steady-state oscillations in current, while the voltage stabilizes at a constant level.
- ✓ **Behavior Type:** Reflects characteristics typical of circuits with capacitive charging, switching loads, or PWM control.
- ✓



Average power(ii) = 1.864 nW

The average power consumption is calculated as follows:

- **Average Power (i):** 138.4 µW
- **Average Power (ii):** 1.864 nW

Total Power Consumption of the System: Average Power (i) + Average Power (ii)
The total power consumption of the system is approximately **138.4 µW**

Equivalent circuit:

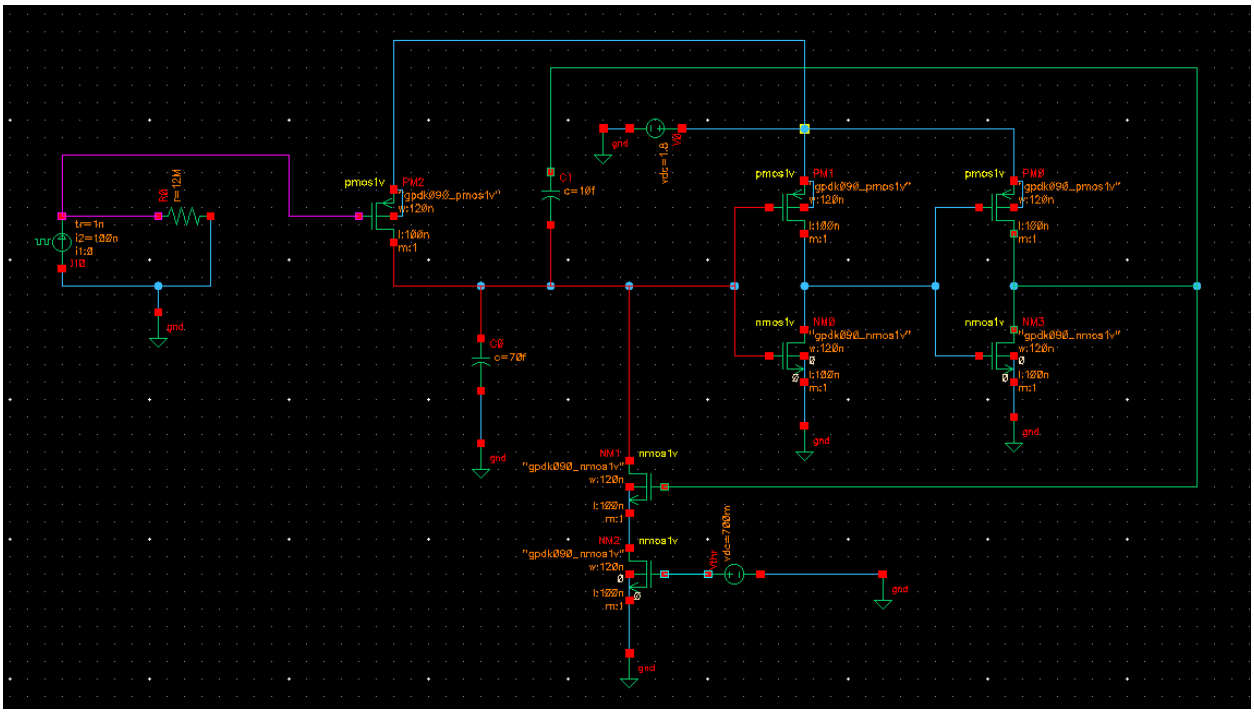


Figure 7: Equivalent circuit

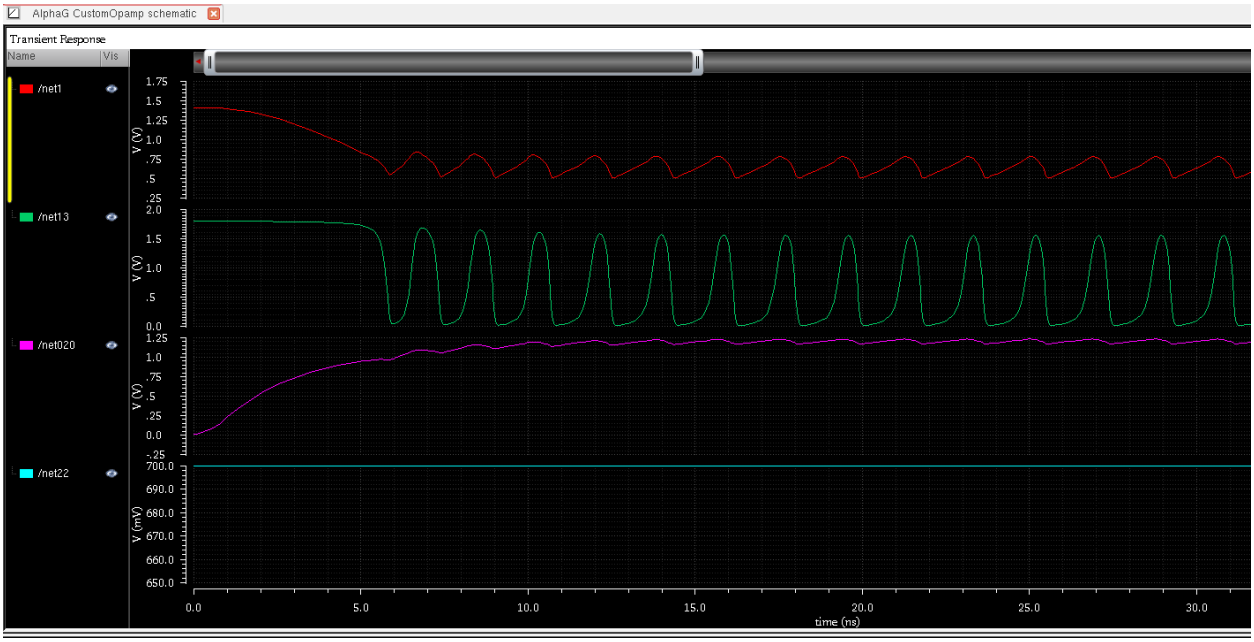


Figure 8: Neuron-Like Transient Response in Equivalent Circuit

1. **/net1 (Red Trace)**: Starts high at ~1.75 V, shows periodic spikes, simulating action potentials from capacitive charge-discharge cycles.
2. **/net13 (Green Trace)**: Maintains ~1.5 V with periodic dips, indicating reset or refractory phases, possibly from feedback control.
3. **/net020 (Purple Trace)**: Gradually rises and stabilizes around 0.75 V, representing threshold buildup prior to firing events.
4. **/net22 (Cyan Trace)**: Holds a steady 670 mV, likely serving as a constant reference voltage for the circuit.

Each trace contributes to mimicking the key dynamics of neural firing, thresholding, and reset behavior in the circuit.

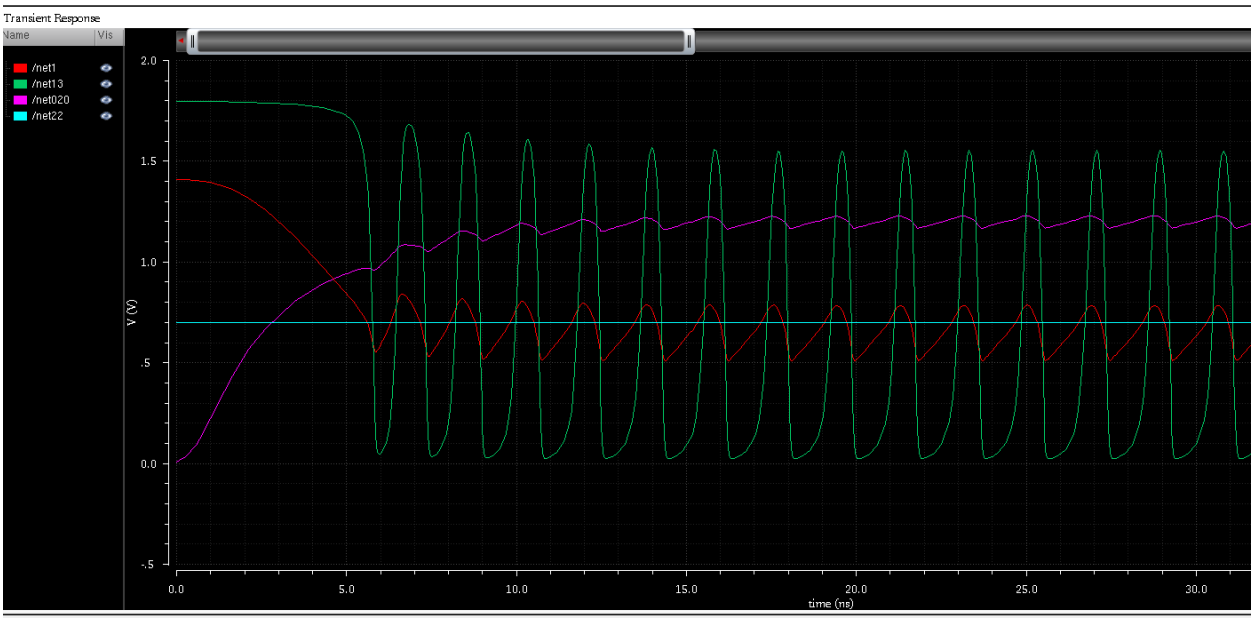


Figure 9

We got some error for this circuit:

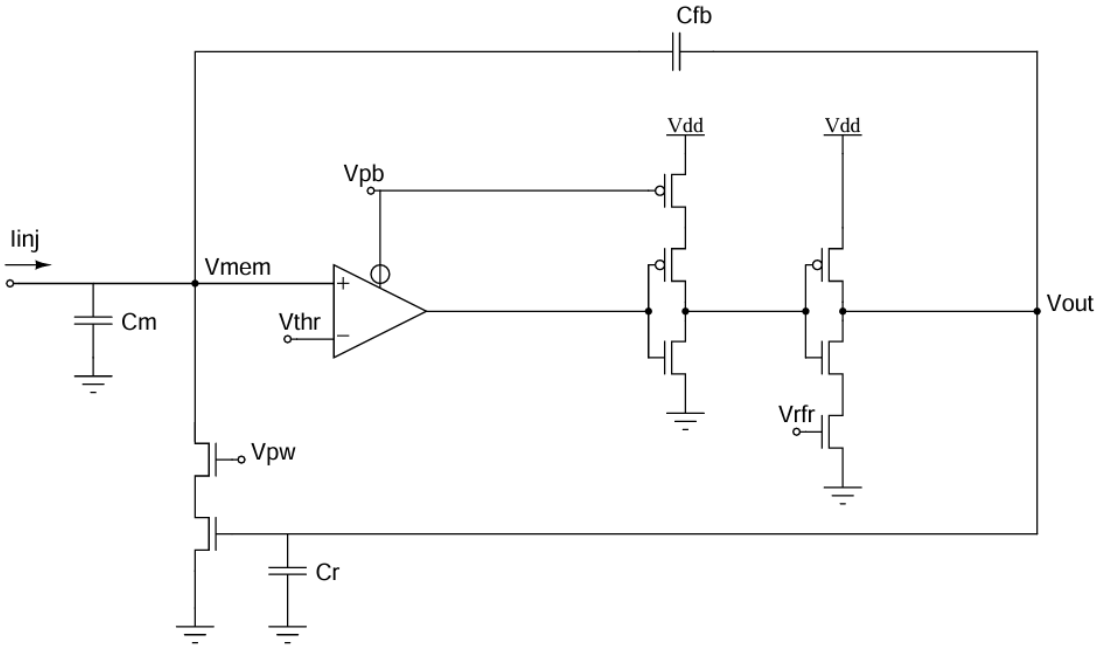


Figure 10

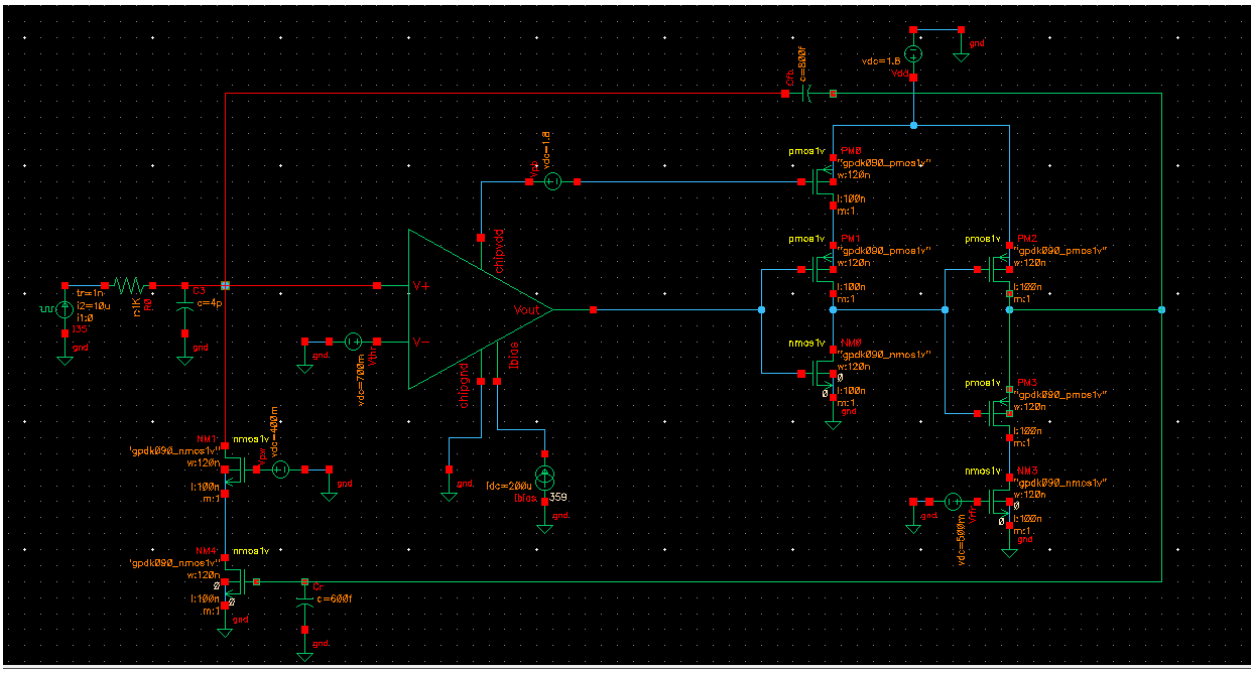


Figure 11

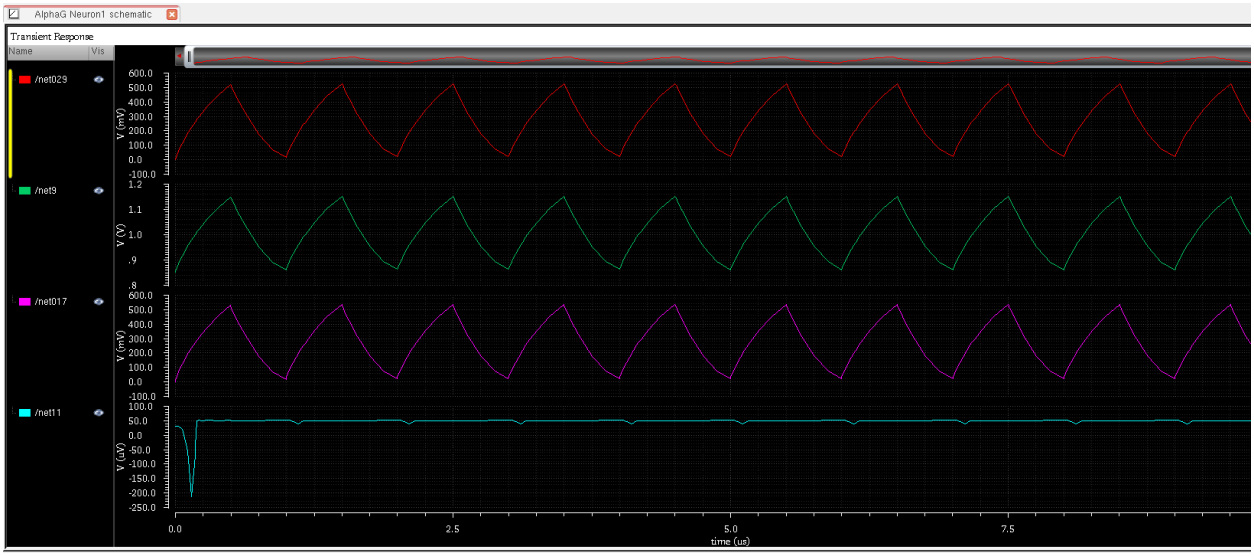


Figure 12