

EAST WEST UNIVERSITY  
ELECTRICAL & ELECTRONIC ENGINEERING  
POST LAB-03

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Student ID: 2020-1-80-092

Course code: EEE 416

Course Title: VLSI Circuit & Systems

Experiment no: 03

Experiment name: Introduction to Cadence, NAND Gate  
design and design rule checking

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### OBJECTIVE :

In this experiment we have learnt to use cadence to build a NAND gate , verify it and also build a layout of NAND gate .

### Methodology :

In NAND gate , we used two inputs , connected two pmos in parallel and two nmos in series. Then we generated sinusoids and build a layout and verified it .

CS Scanned with CamScanner

### RESULTS

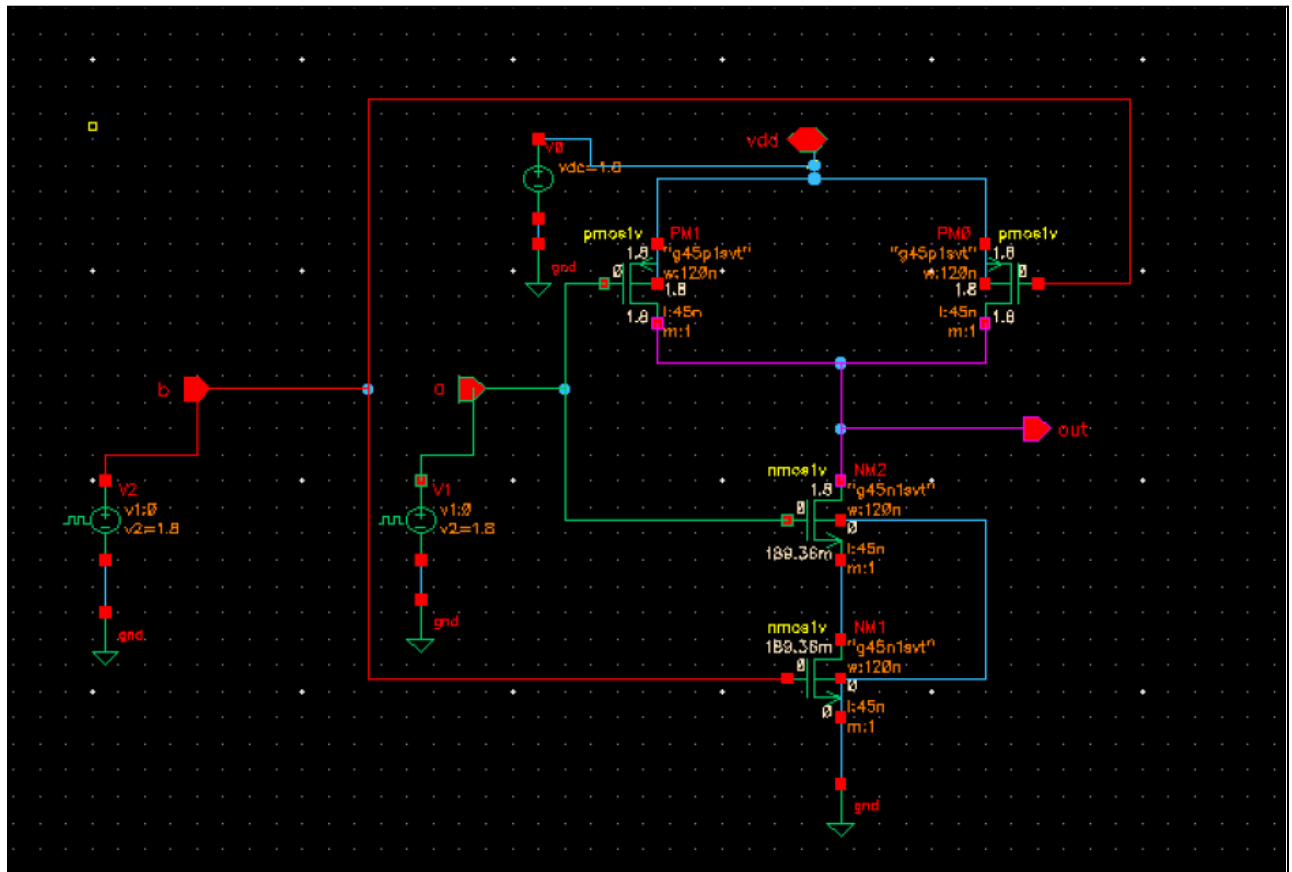


Fig 1 : NAND gate circuit diagram

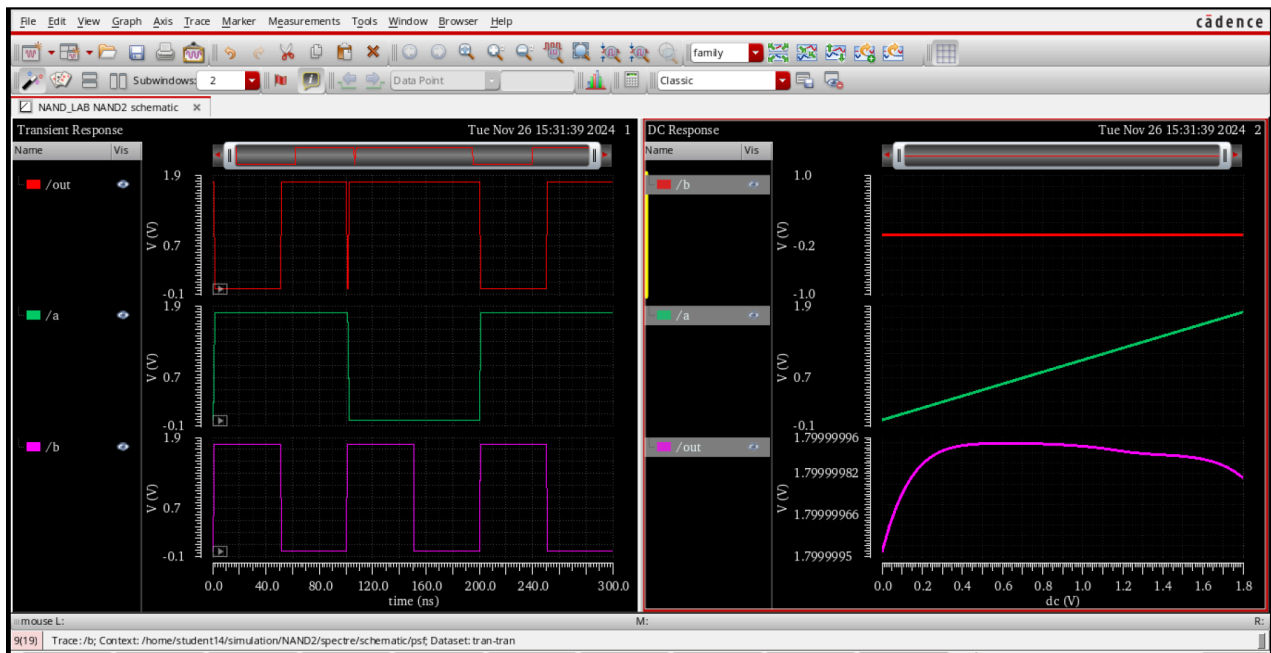


Fig 2 : NAND gate input and output result

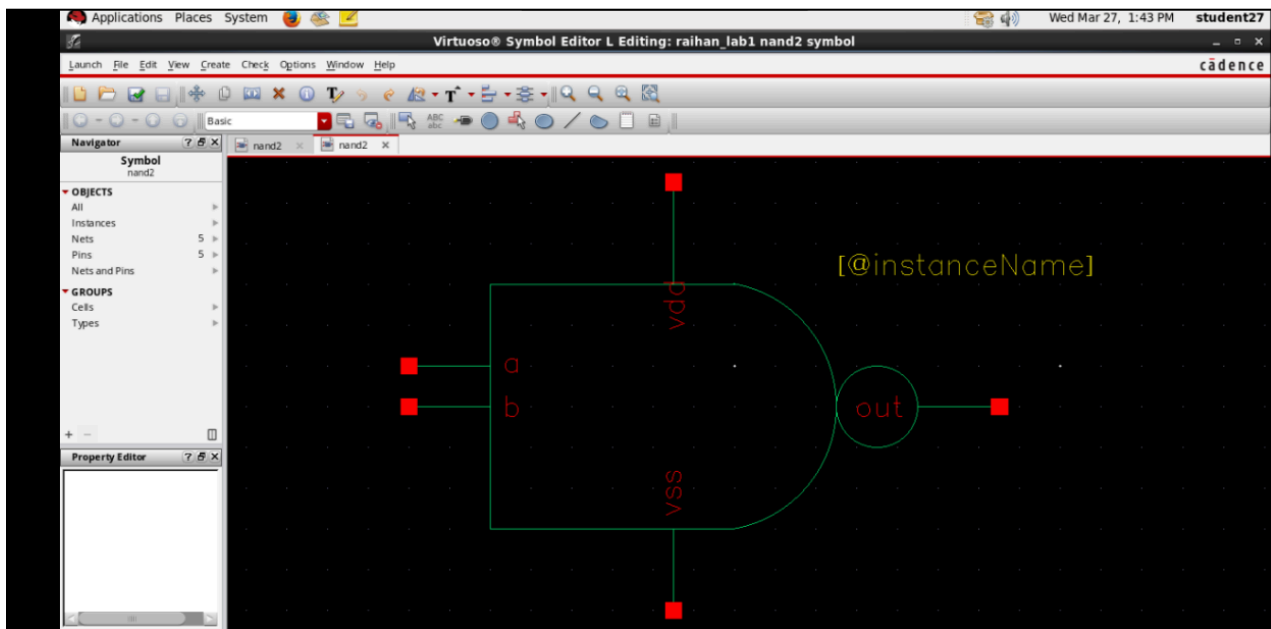


Fig 3 : NAND gate symbol

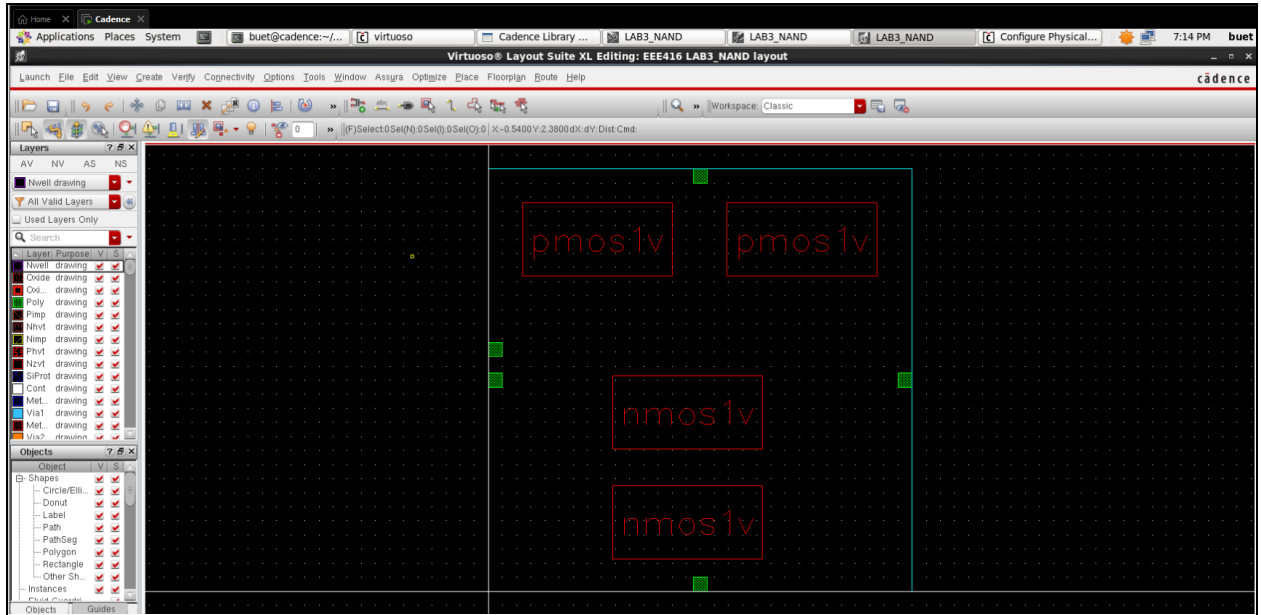


Fig 4 : Mosfet boxes in the starting of layout design

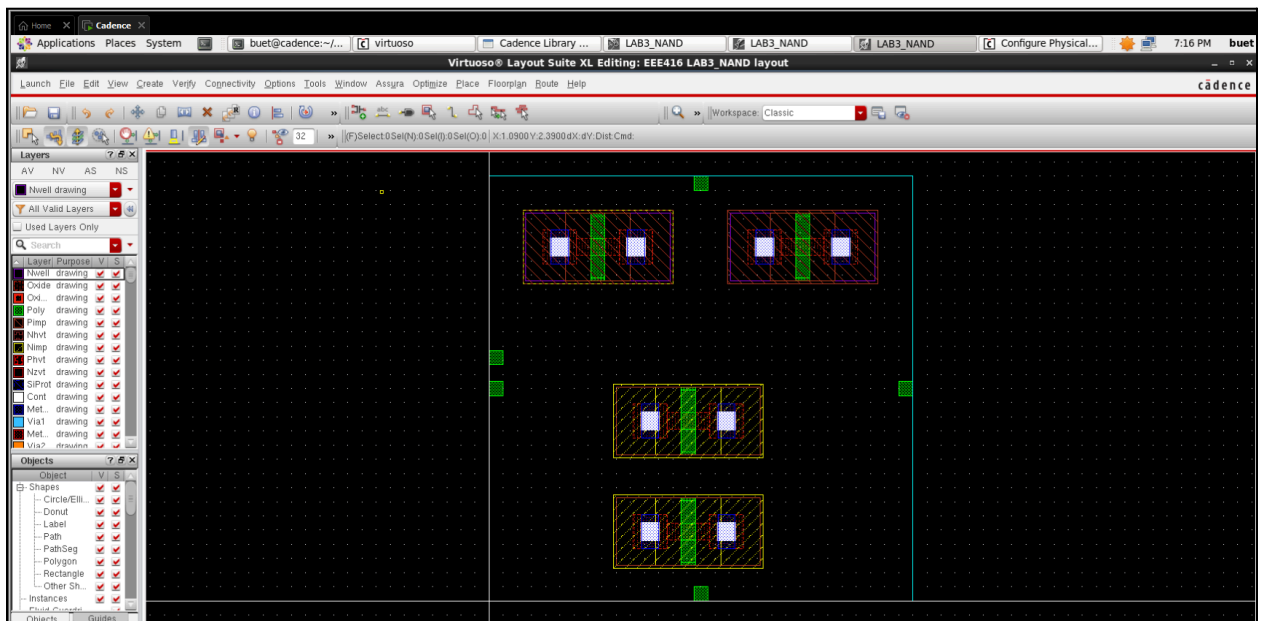


Fig 5 : After pressing shift+f

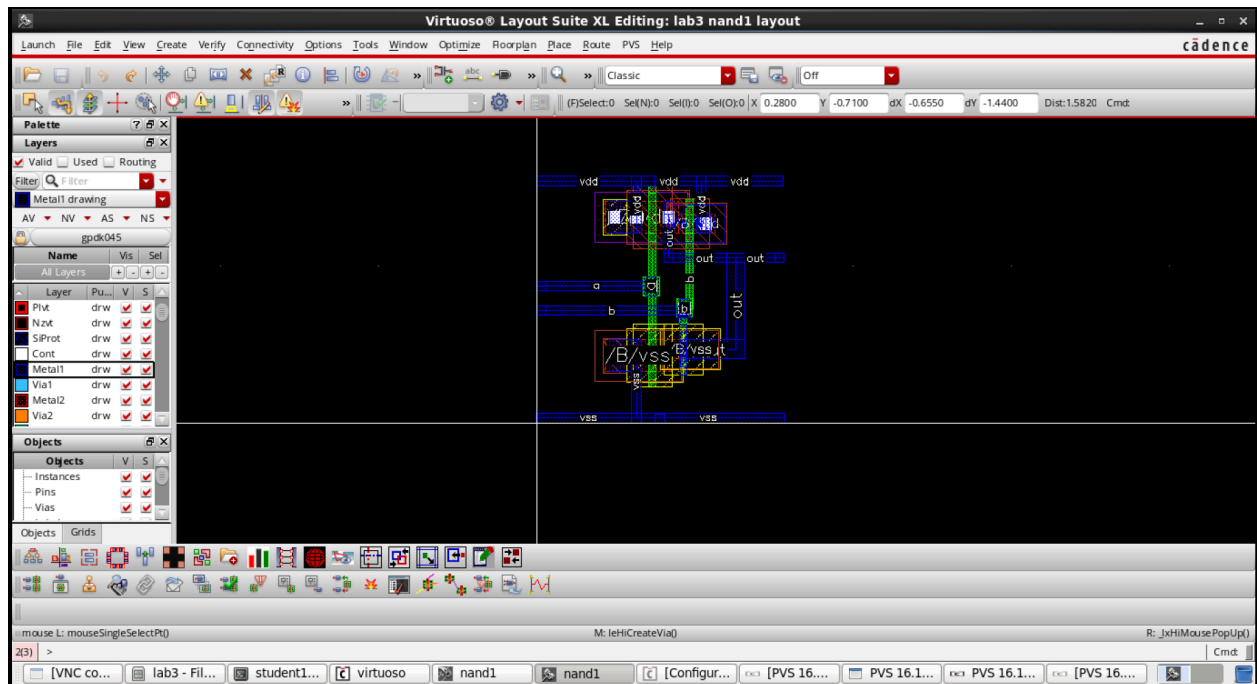


Fig 6 : NAND gate layout design

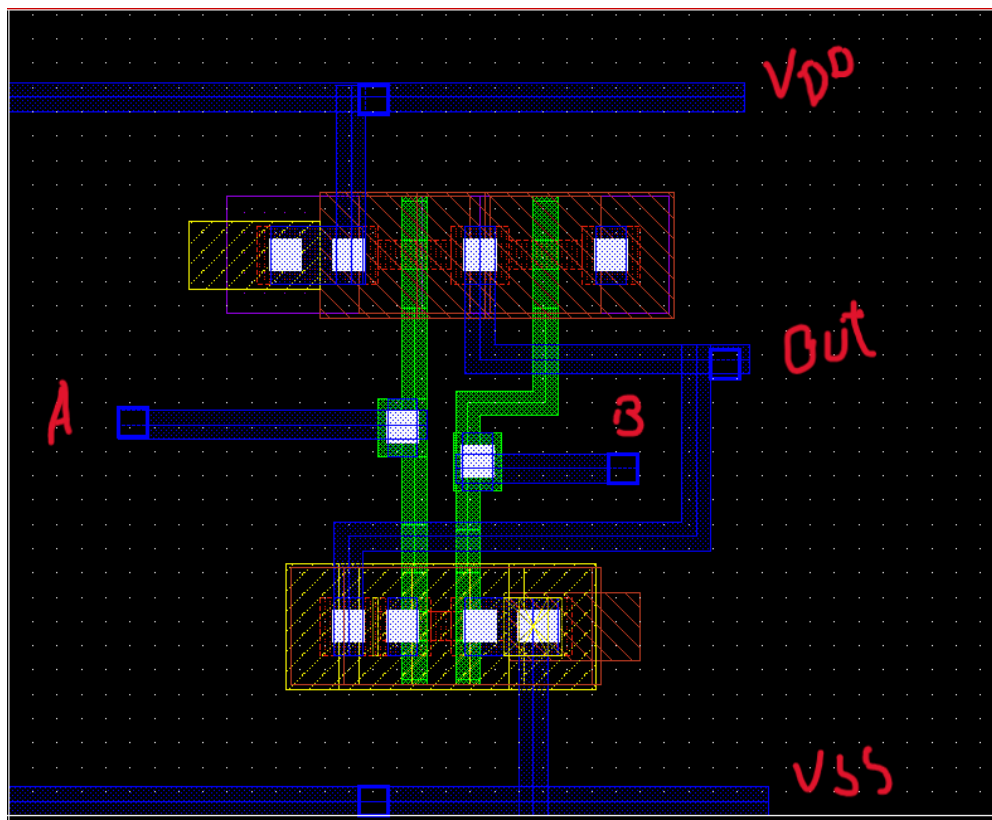


Fig 7 : Layout design

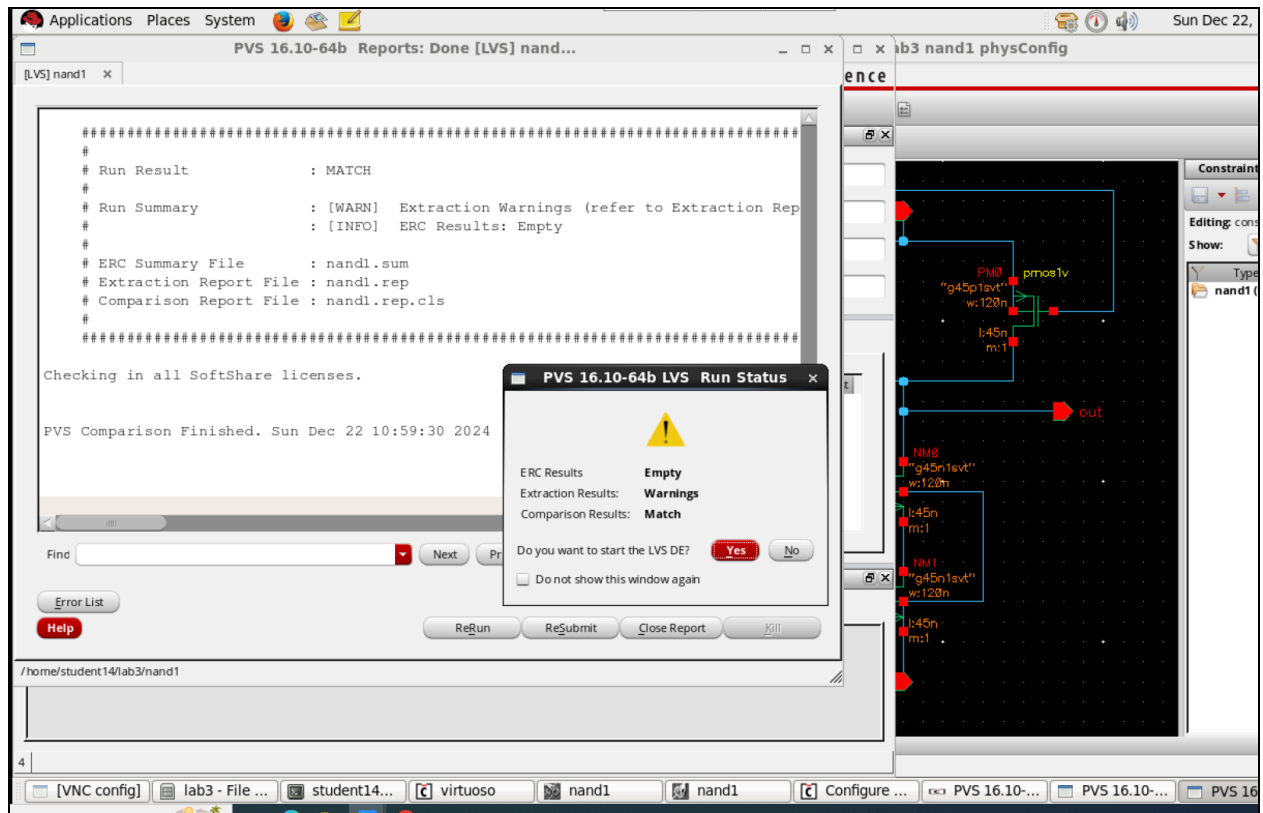


Fig 8 : LVS match result

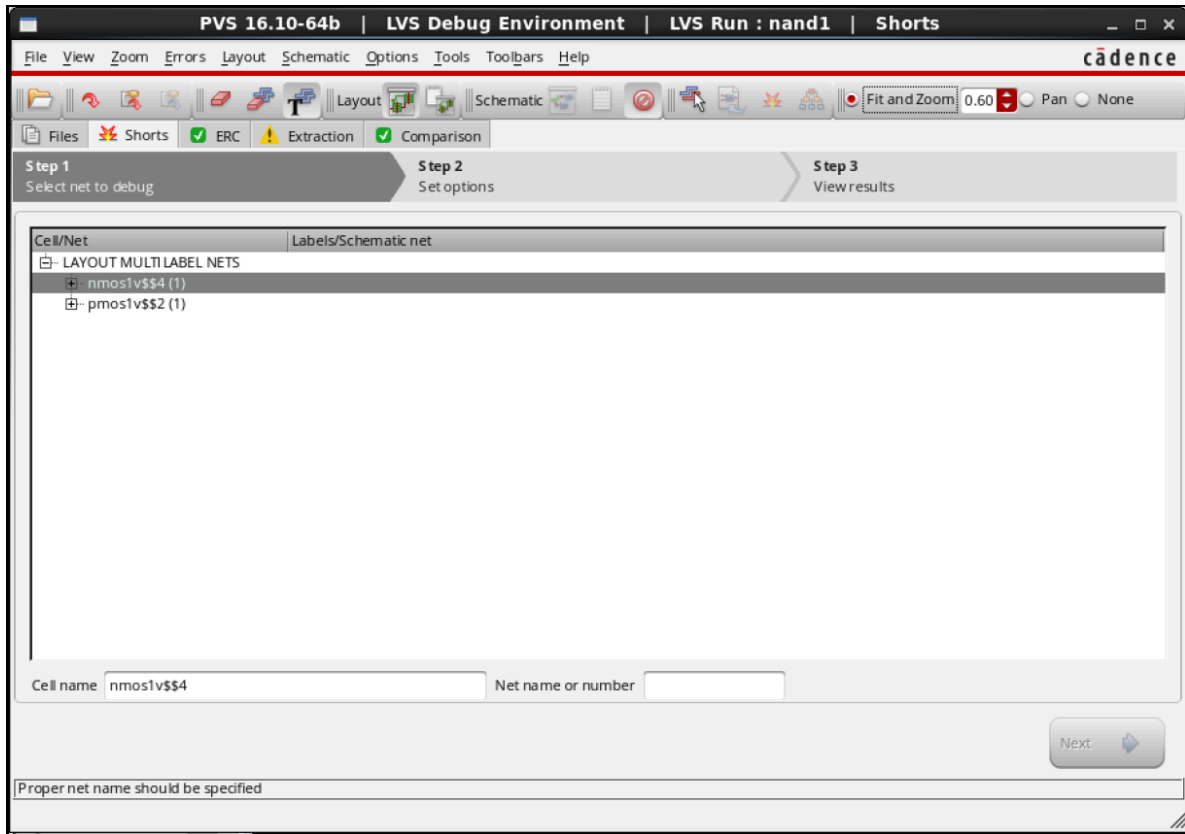


Fig 9 : LVS match result

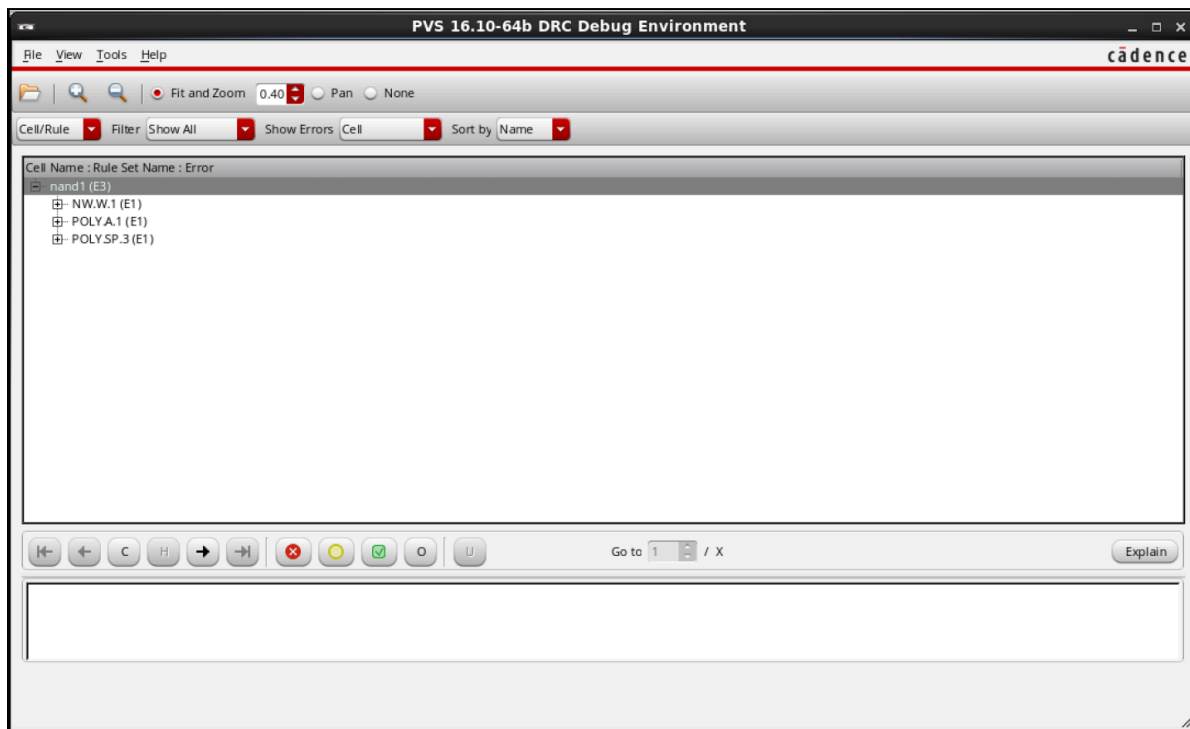


Fig 10 : DRC match result

Truth Table :

Input		Output
a	b	
0	0	1
0	1	1
1	0	1
1	1	0

From the sinusoid we can see when the input  $a=1$  and  $b=1$  the output is 0.

When  $a=1$ ,  $b=0$  the output becomes 1. No we can see the ~~si~~ truth table and verify the sinusoid of Nand gate.



### Explanation:

During this experiment we tried to follow design rule of MOSFET. We considered the size of n-well, polysilicon spacing, metal spacing, latch up effect. In MOS design, design rules are to be strictly maintained to fabricate and integrate the circuit. Also it is mandatory to deduct the latch up effect. Due to ionization effect we generated body contact and polarization contact.

### Conclusion:

This experiment gives opportunity to be familiarized with the 'cadence'. We understood from the circuit level implementation to the layout design.

The theory ~~the~~ of design rules that were taught in the class. We experienced the importance of that while ~~to~~ designing the layout.