EAST WEST UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

COURSE TITLE : VLSI CIRCUIT & SYSTEMS

COURSE CODE : EEE 416

COURSE INSTRUCTOR : DR. MOHAMMAD MOJAMMEL AL HAKIM

PROJECT TITLE : NOR 3 INPUT SCHEMATIC SYMBOL & LAYOUT GENERATION

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OBJECTIVE

The objective of this project is to design a 3-input NOR gate using Cadence Virtuoso, including it's schematic, symbol and layout. The design process involves analyzing the circuit's performance using pulse signals and ensuring proper functionality through LVS and DRC. This project makes us familiar with 45 nm CMOS technology and fabrication process.

Methodology

The design process starts with constructing the schematic for the 3 input NOR gate in Cadence Virtuoso using NMOS and PMOS transistors. The schematic is simulated with square wave inputs to ensure proper functionality. A symbol for the circuit is then created to enable it's use in hierarchial designs. The layout is designed based on the schematic, following 45 nm CMOS technology design rules. Afterwards, the design undergoes LVS to varify that the layout matches the schematic and DRC to ensure it meets fabrication rules. Then the layers of 45 nm mosfets are shown to understand how the fabrication happens.

Schematic diagram of the 3 input NOR gate and its performance analysis

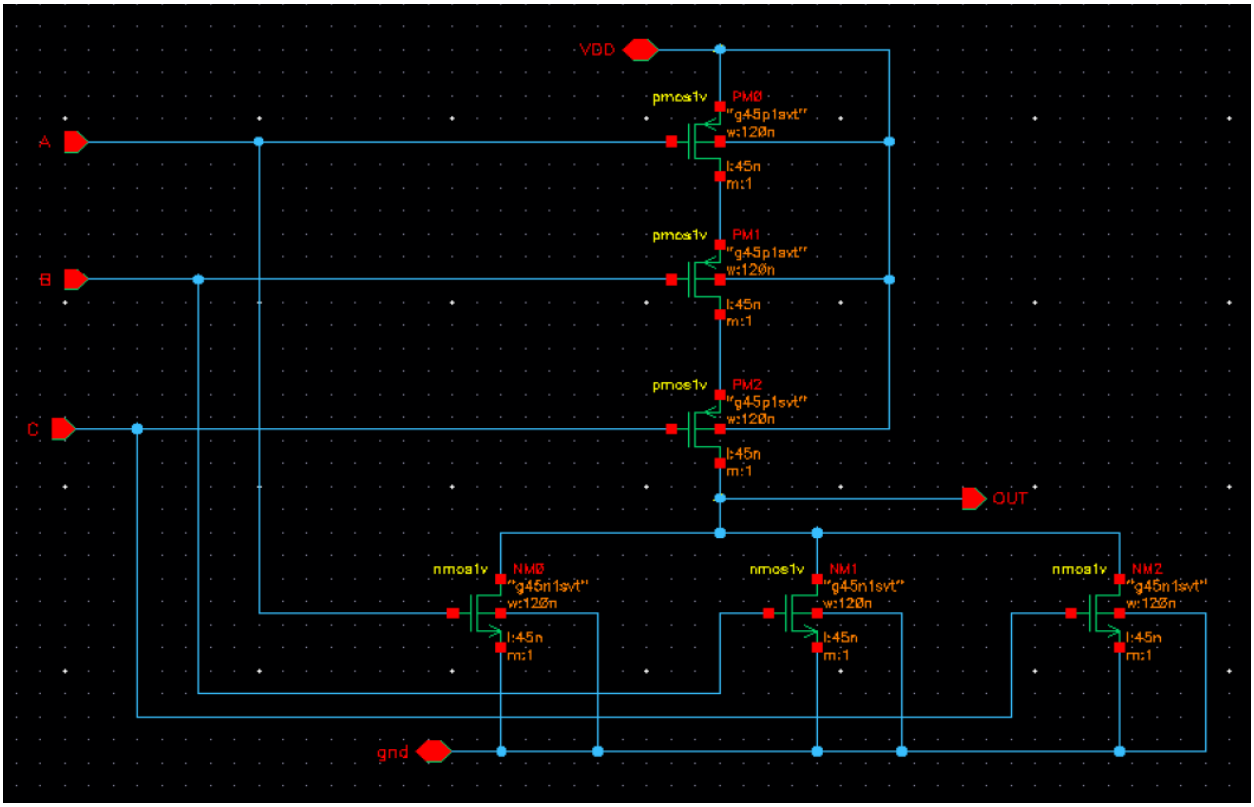

Fig 1: Schematic diagram of the 3 input NOR gate

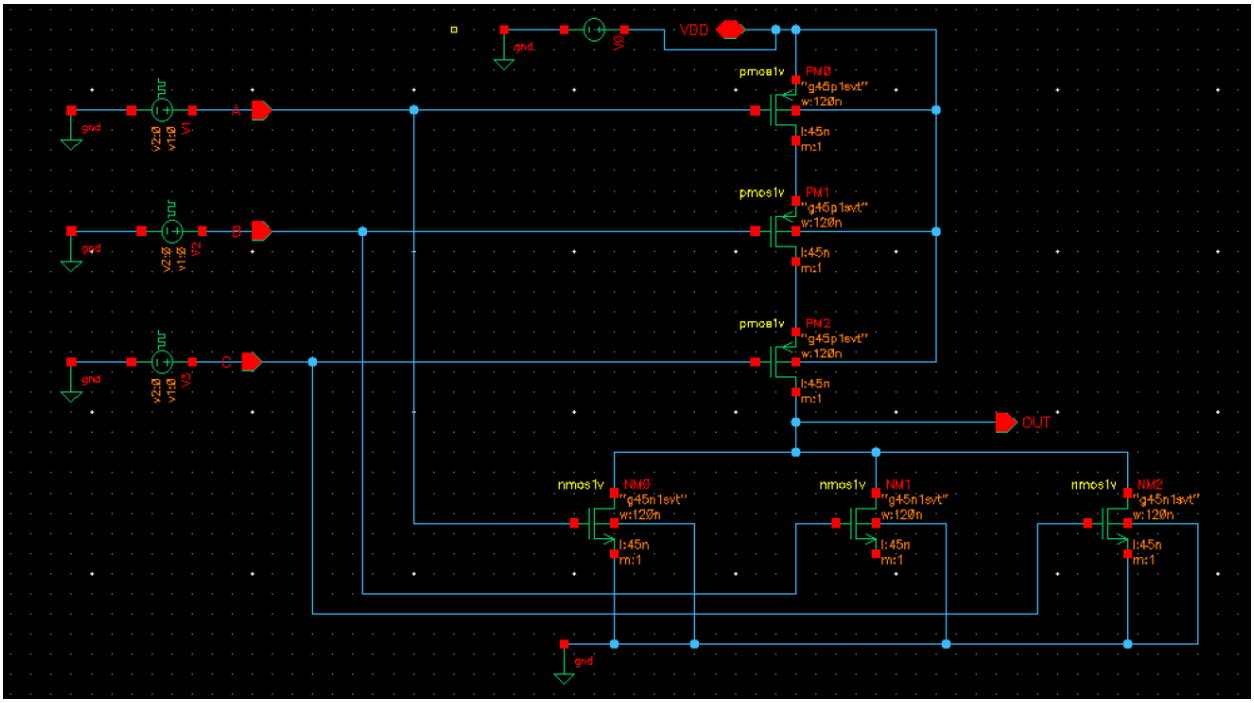

Fig 2 : Schematic diagram of the 3 input NOR gate attached with Vdc and Vpulse sources

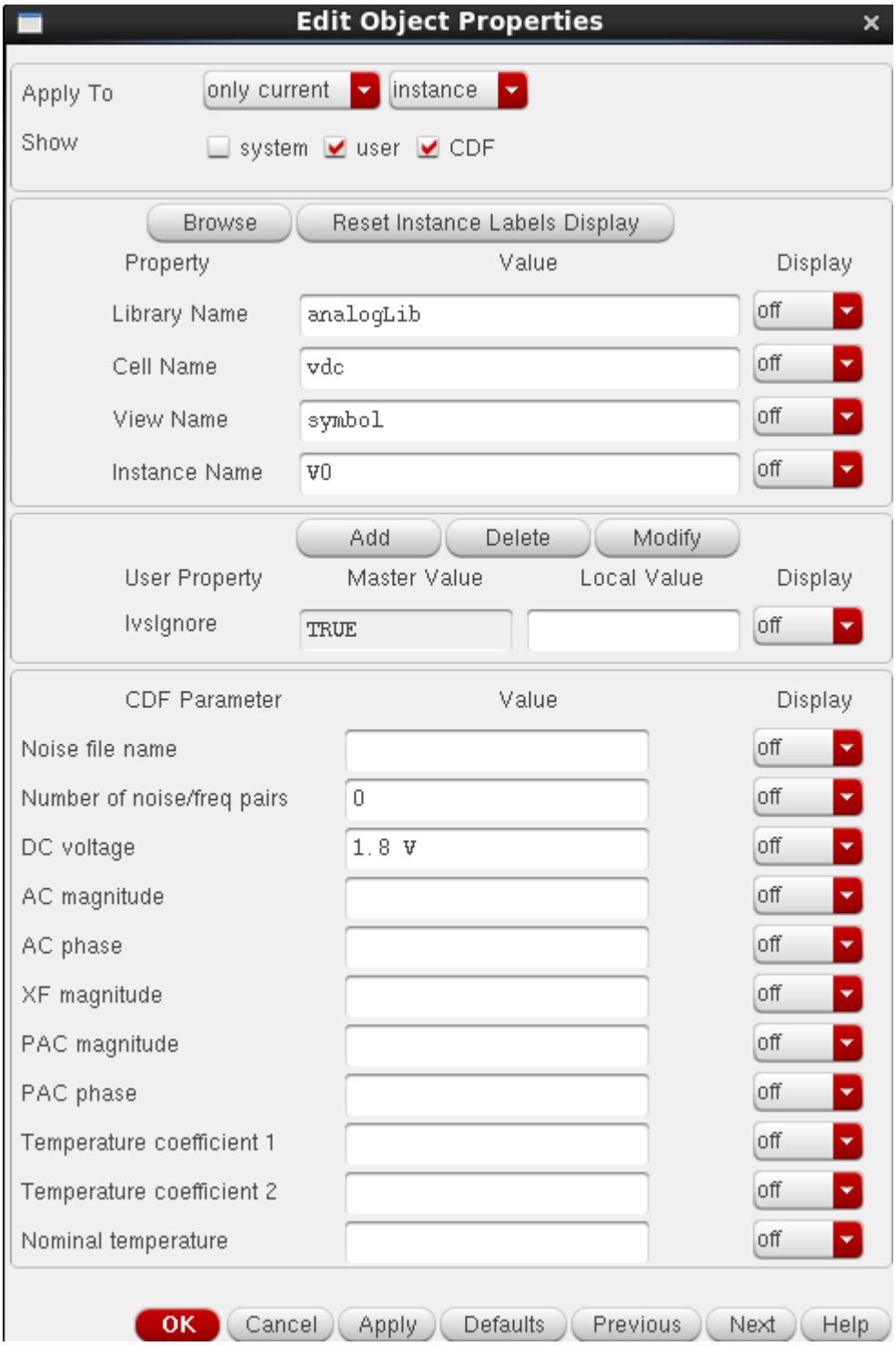

Fig 3: Vdc/VDD specifications

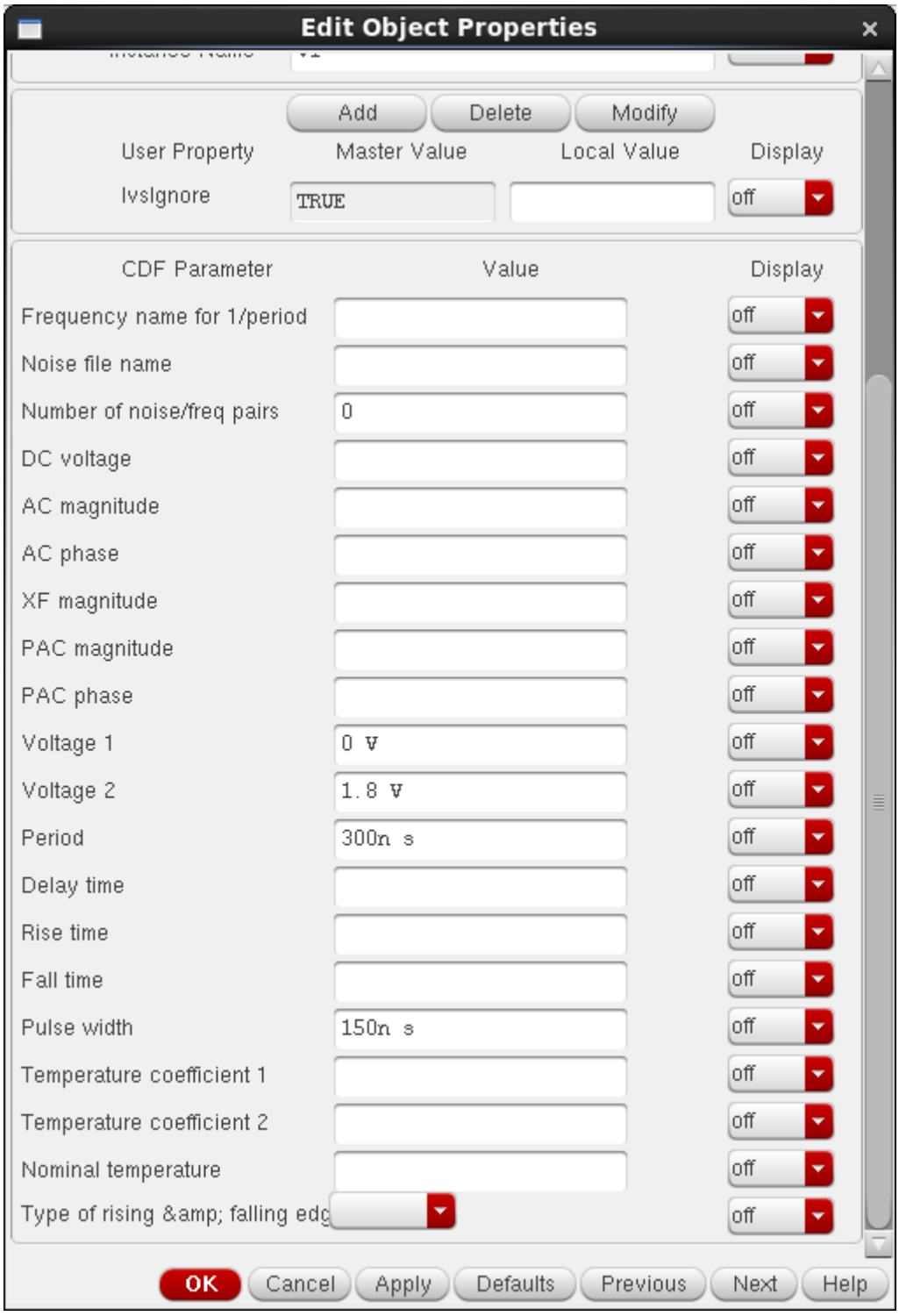

Fig 4: Vpulse connected in pin A specifications

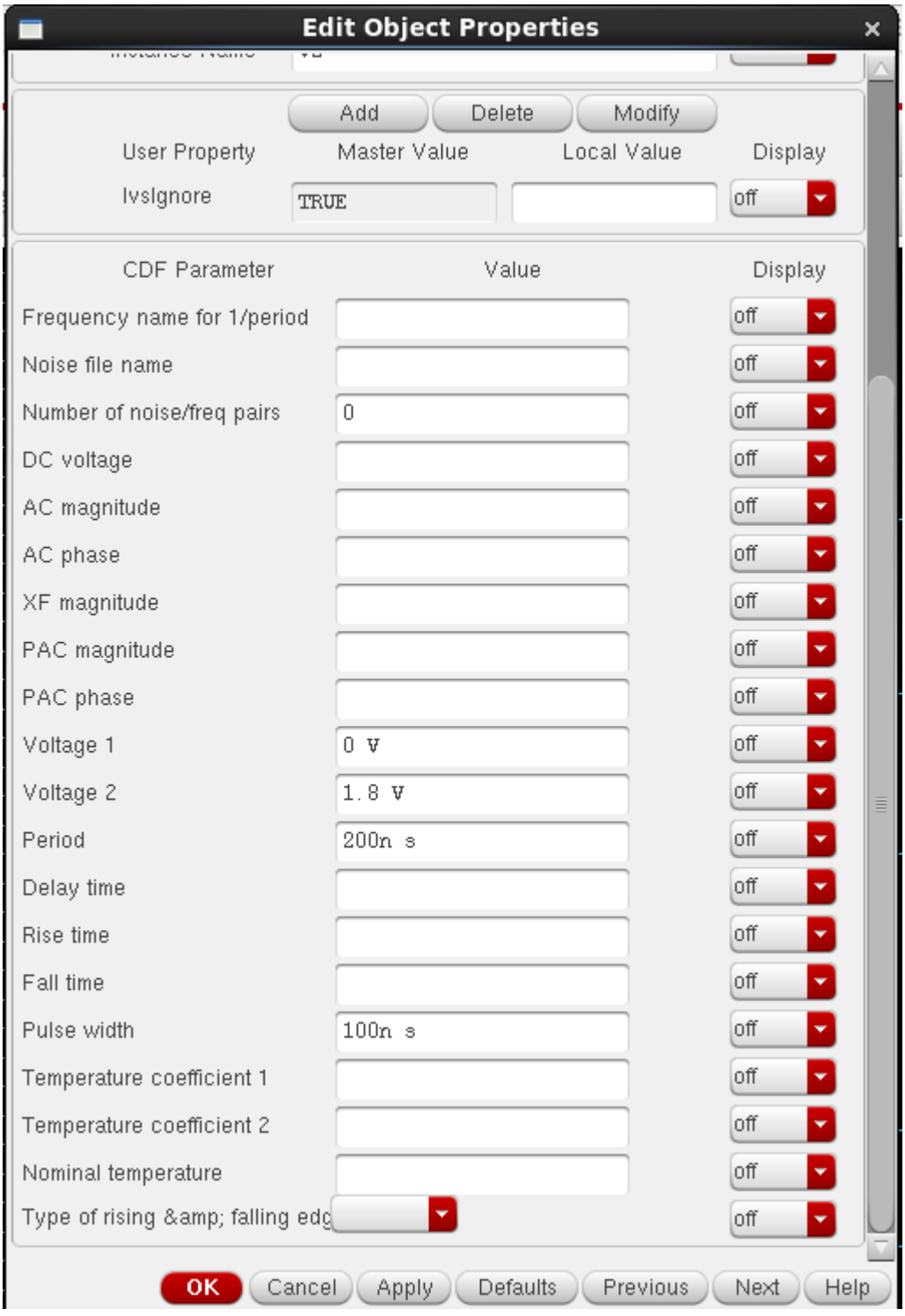

Fig 5: Vpulse connected in pin B specifications

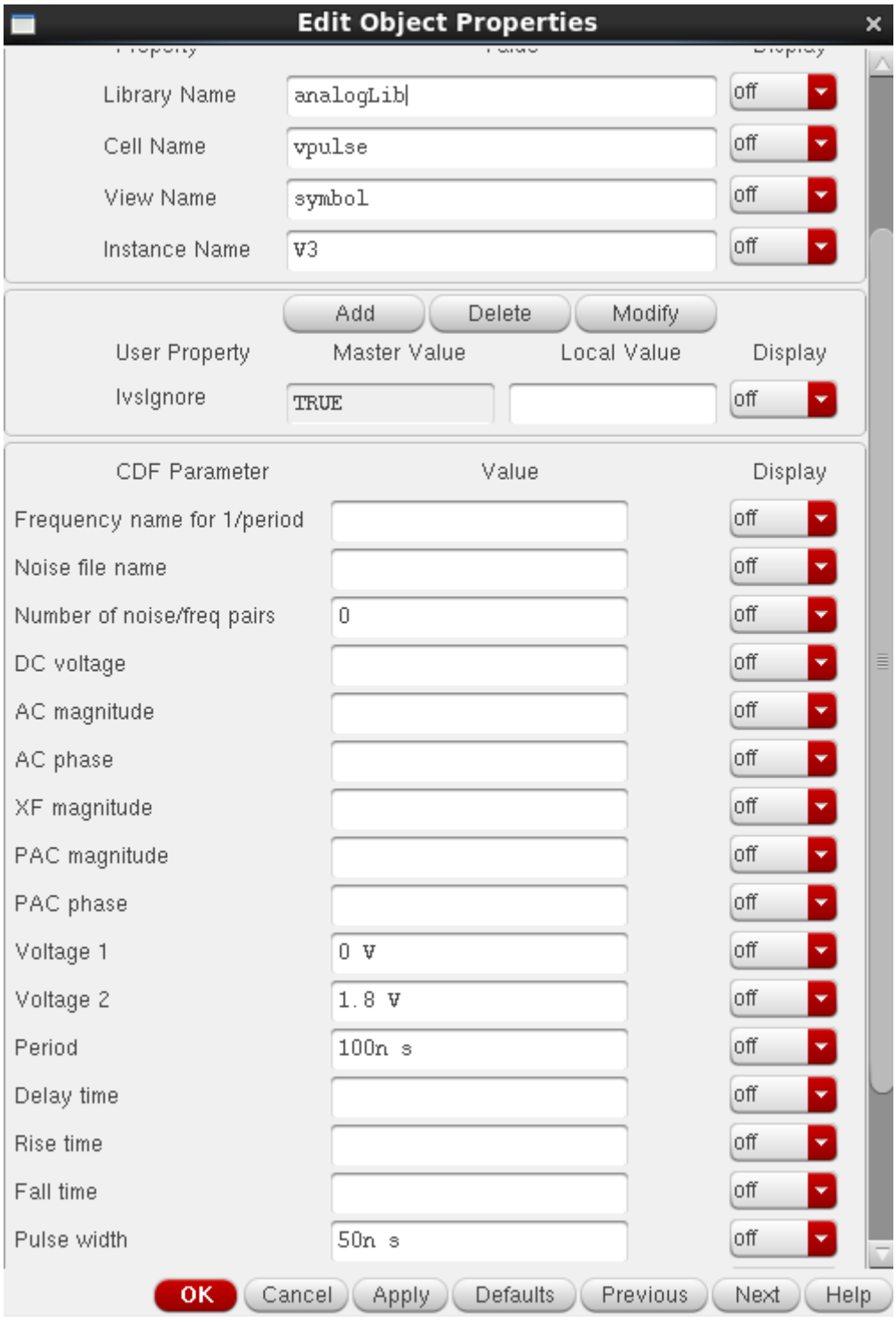

Fig 5: Vpulse connected in pin C specifications

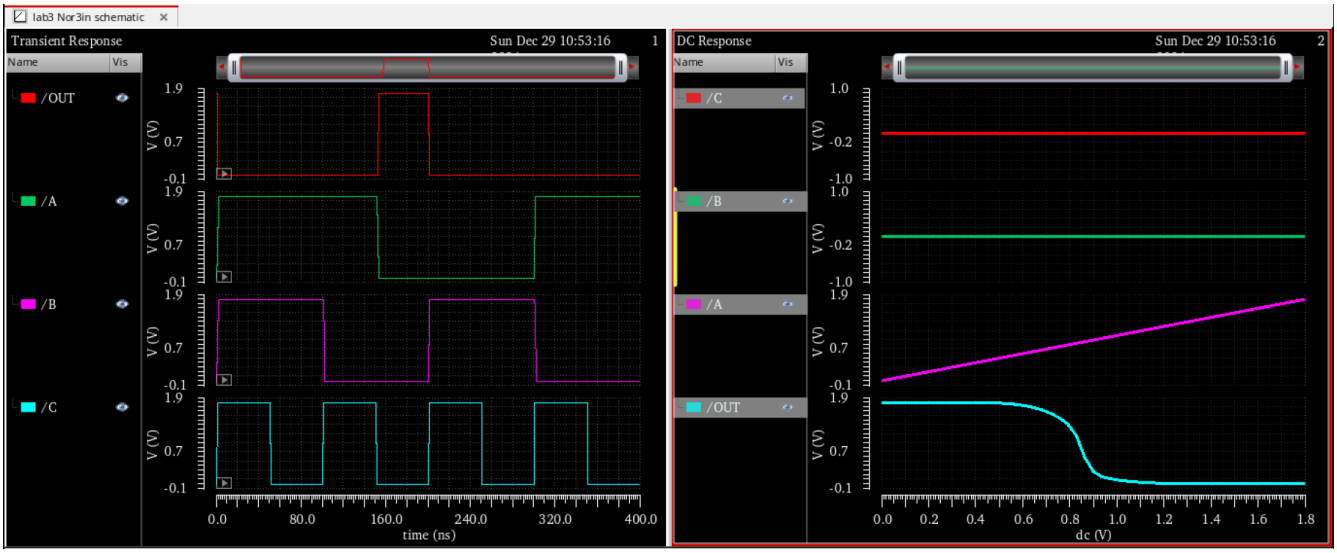

Fig 7: Performance analysis using square wave signals

Output signal is only high when all the input signals (A,B,C) are low and for all other combinations of the input signals, the output signal stays low.

Symbol Draw

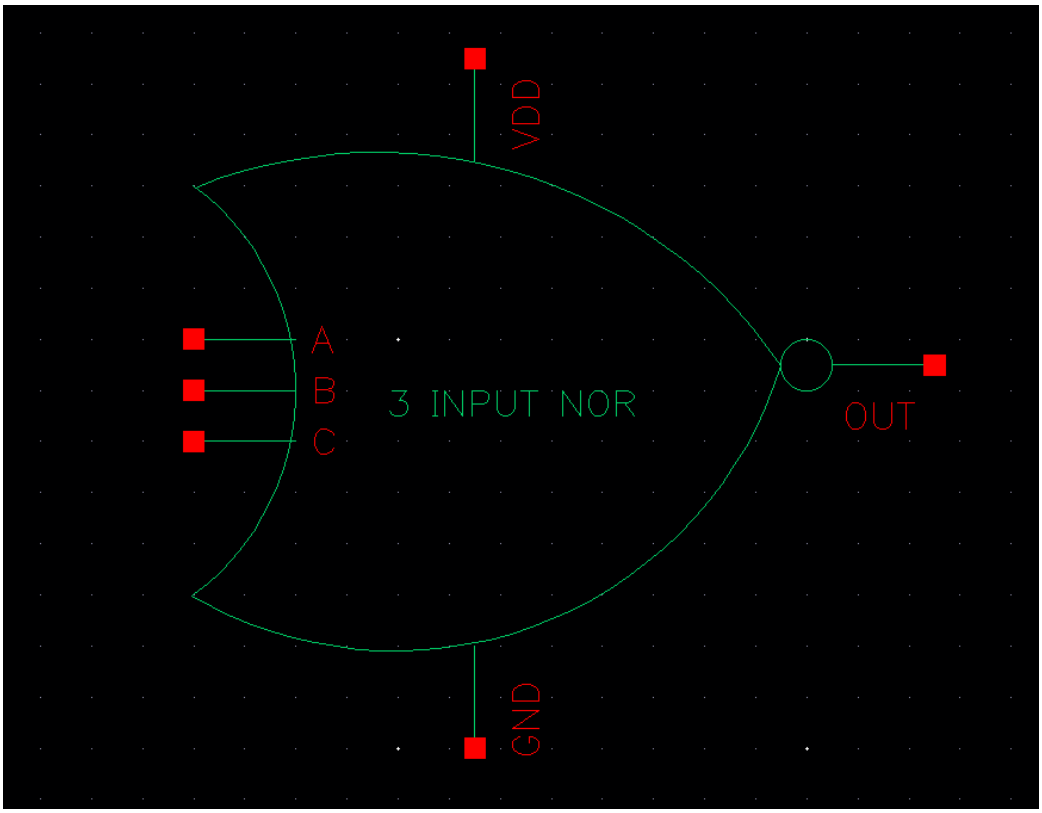

Fig 8: Symbol of the 3 input NOR gate

SCHEMATIC DESCRIPTION :

The provided schematic represents a 3 input NOR gate designed using CMOS technology. It comprises a parallel PMOS network and a series NMOS network. The PMOS (3) transistors pull the output high (V_{DD}) when all inputs (A,B,C) are low, while the NMOS transistors pull the output low when any input is high. The circuit functions according to the NOR gate logic, where the output is the compliment of the OR operation of the inputs, expressed as $OUT = (\overline{A+B+C})$.

PERFORMANCE ANALYSIS :

The transient response of the circuit confirms its correct functionality. The output remains high only when all inputs are low and transitions to low as soon as any of the inputs is high. Smooth transitions confirm reliable operation with predictable delays. due to the charging and discharging of the load capacitance, characteristic of CMOS gates.

Overall, the 3 input NOR gate performs as expected, demonstrating correct logic operation. The DC response further validates the circuits behaviour by showing a rapid transition of the output voltage as the input voltage crosses the threshold level.

Layout Draw

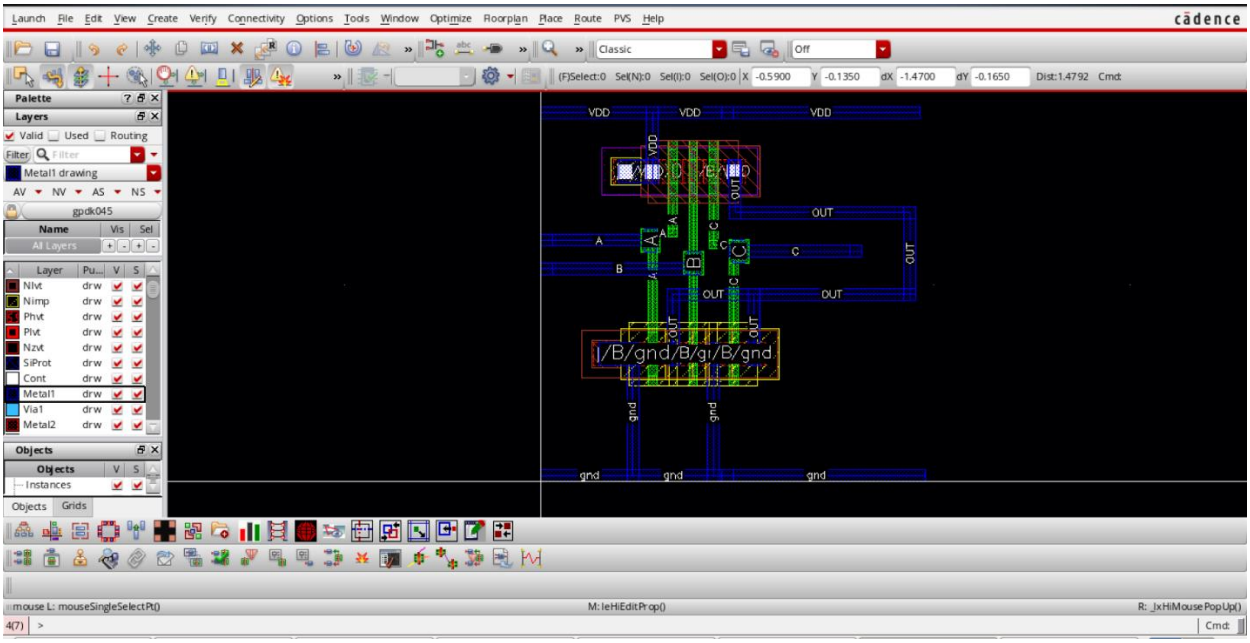

Fig 9: Layout design of 3 input NOR gate

Run LVS

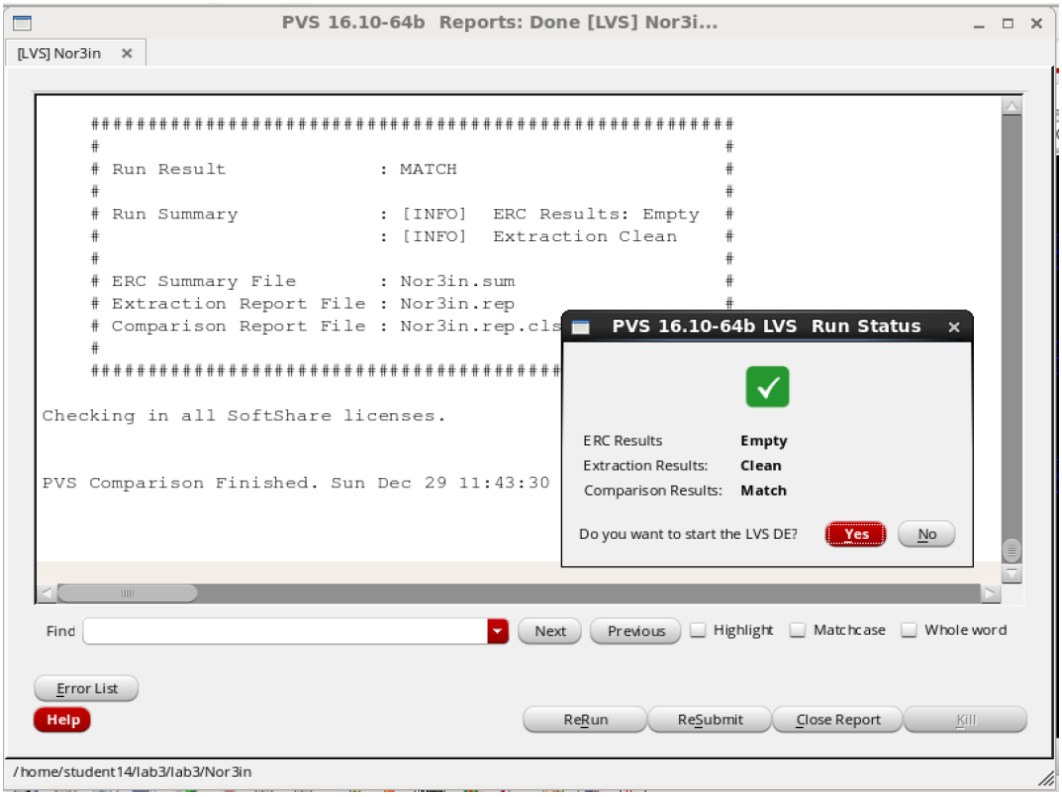

Fig 10: LVS is clean

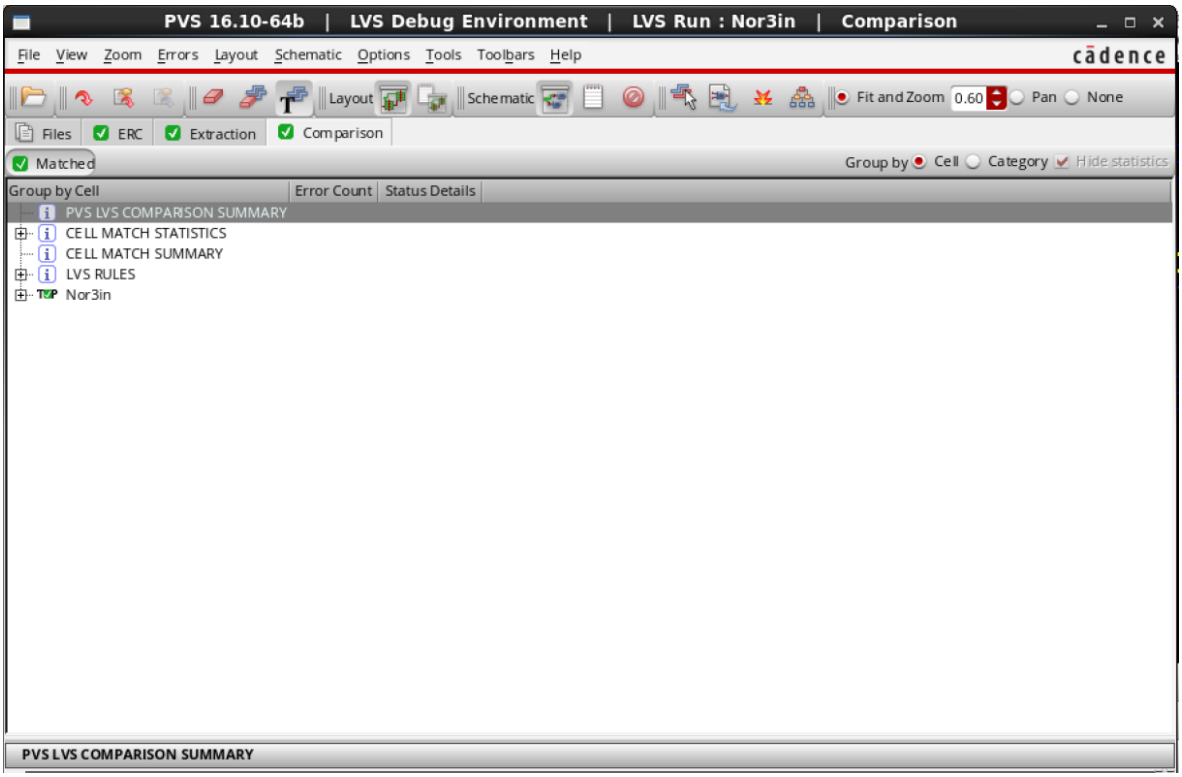

Fig 11: LVS run results

Run DRC

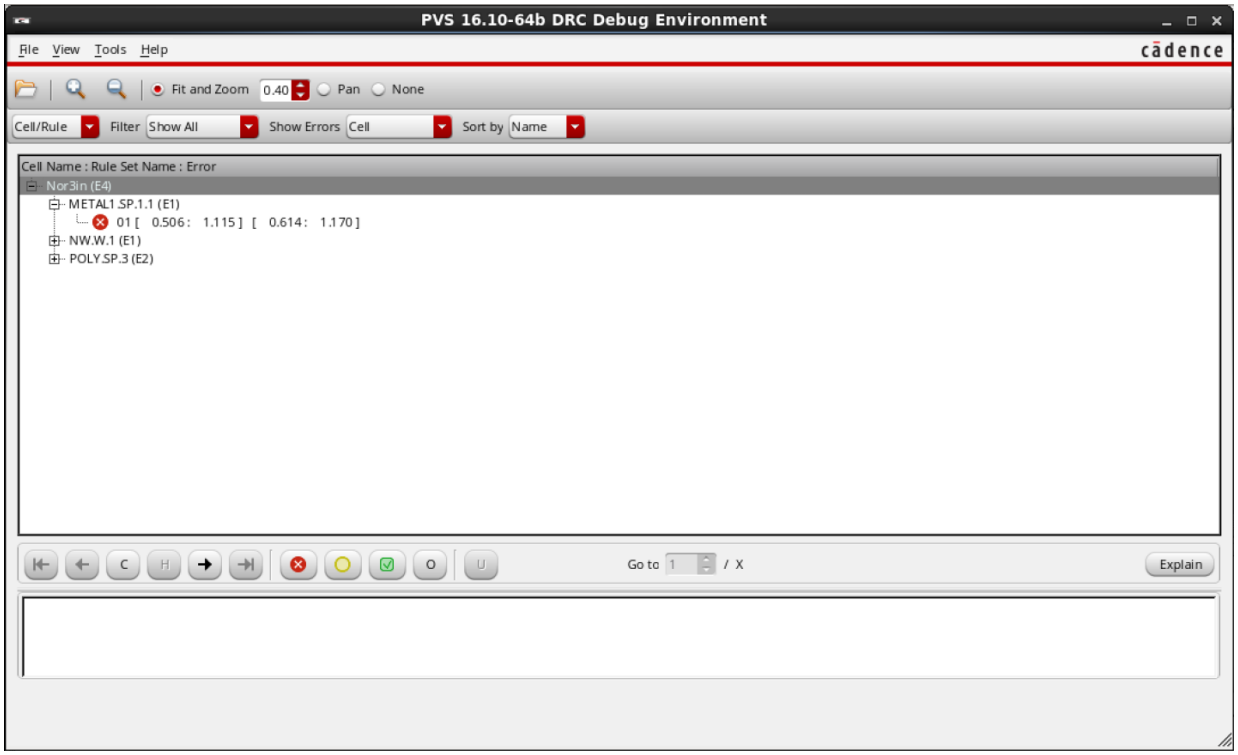

Fig 12: DRC error lists

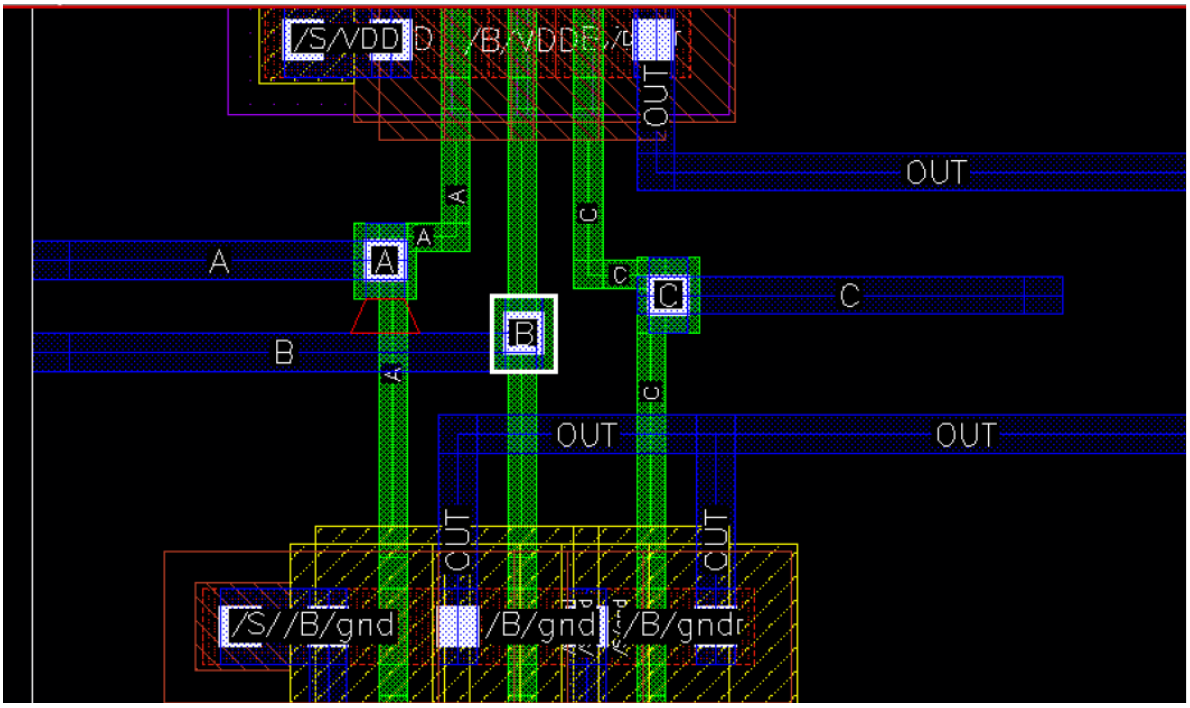

Fig 13: Metal1.SP error in layout

Fixed METAL1.SP.1.1 error in layout by shifting metal layers farther from each other.

Fixed NW.W.1 error by increasing the PMOS width from 120nm to 240nm.

Fixed POLY.SP.3 error by shifting the VIA a little far from the poly layer.

Layout after fixing all 3 errors

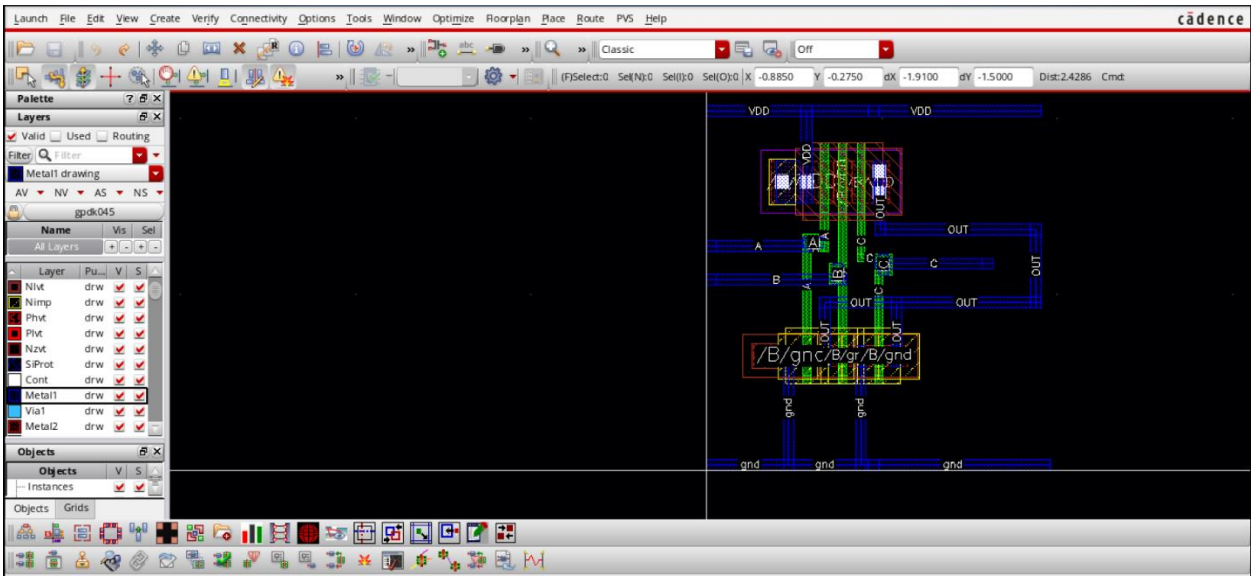

Fig 14: Final layout of the 3 input NOR gate

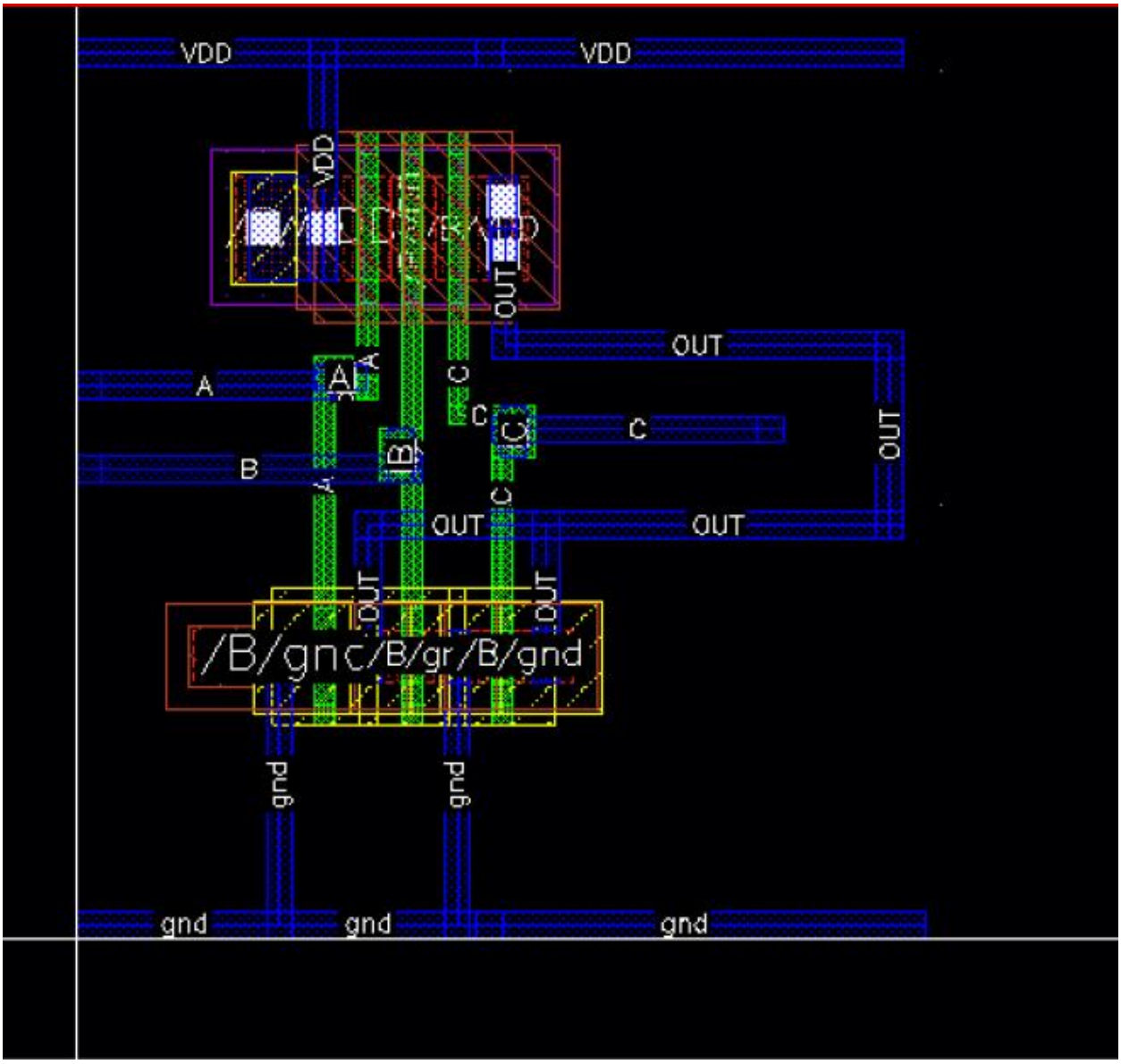

Fig 15: Final layout of the 3 input NOR gate

Run DRC again for checking errors

Fig 16: No error found in DRC

Sequential description of possible process steps to fabricate the 45 nm CMOS device.

1. Substrate Preparation
   * Start with a P-type silicon wafer
   * Perform oxidation to create a thin silicon dioxide layer for isolation.

2. Well Formation
   * Use photolithography and ion implantation to define the N-well and P-well regions.
   * Anneal the wafer to activate dopants and repair lattice damage.

3. Polysilicon Gate Formation and Field Oxide Formation
   * Use the LOCOS or STI (Shallow Trench Isolation) technique to isolate the transistors. This prevents current leakage between adjacent devices.
   * Deposite a thin oxide layer as a gate dielectric
   * Deposite and pattern polysilicon using photolithography.

4. Source and Drain Implantation
   * Define the active regions for the source and drain.
   * Perform light doping for the LDD regions.
   * Use spacer formation and a second, heavier implantation to complete the source and drain doping.

5. Contact Formation.

* Open Vias (contacts) in the oxide layer to expose the source and drain terminal
* Represented by the red contact/via layers, these ensure electrical connectivity between metal layers and underlying components.

6. Metal layer Deposition and Patterning.

* Deposit the first metal layer and pattern it as per the layout.
* This forms the interconnections for inputs (A, B, C), output (OUT), V_{DD} and gnd.
* Add additional metal layers as needed, ~~separated~~ separated by interlayer dielectrics (ILDs) with vias connecting them.

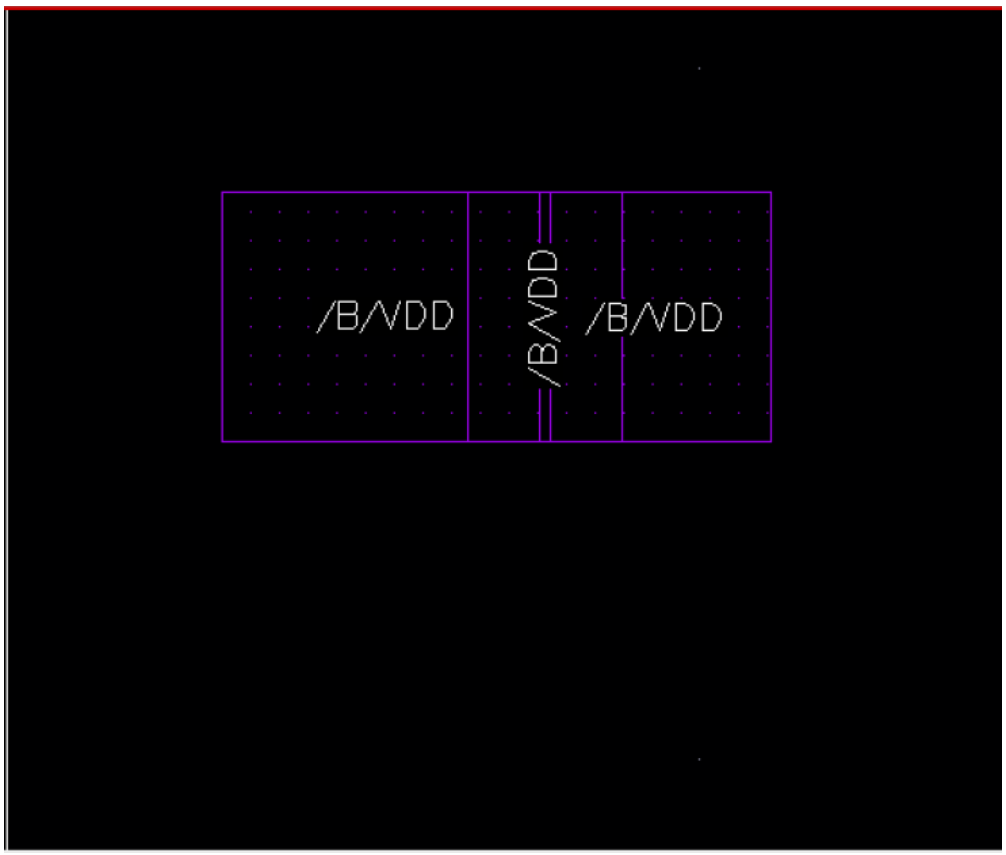

Fig 17 : Nwell formation in P type substrate

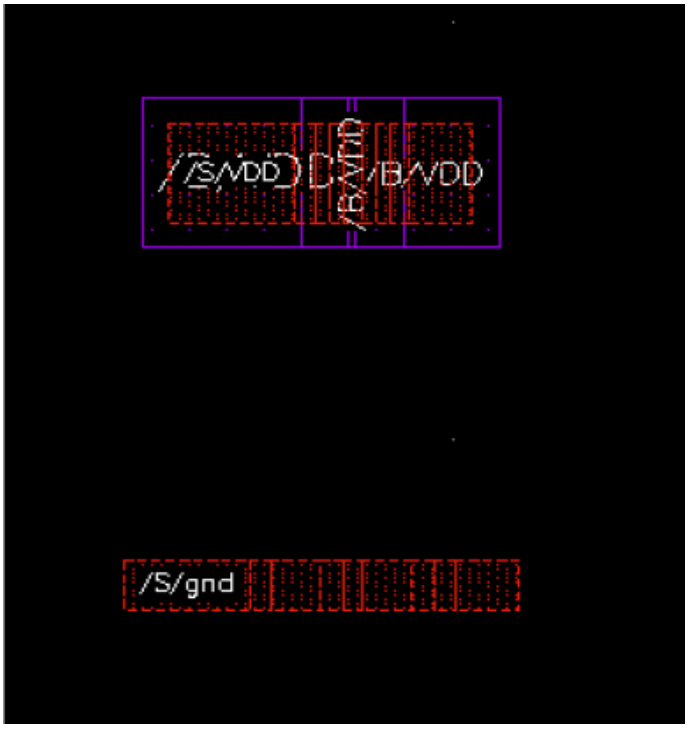

Fig 18: Oxide formation in the substrate

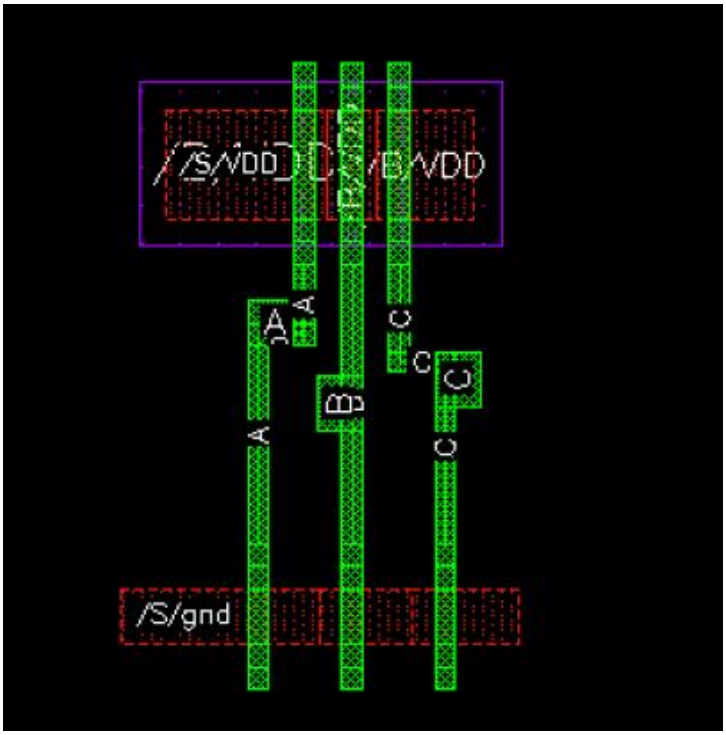

Fig 19: Gate formation above the gate oxide

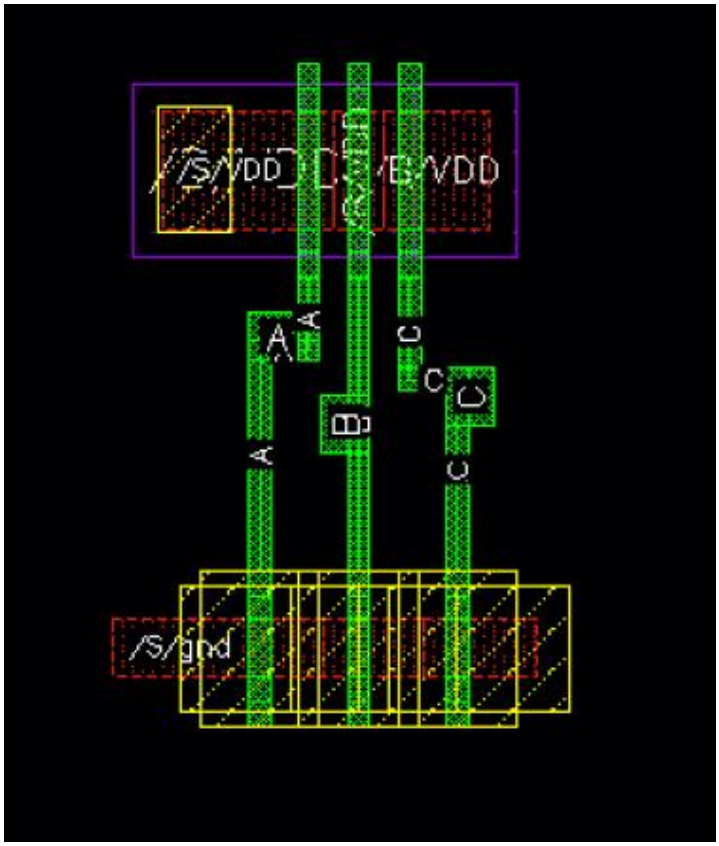

Fig 20: After providing N+ implant (forming LDD and HDD in NMOS)

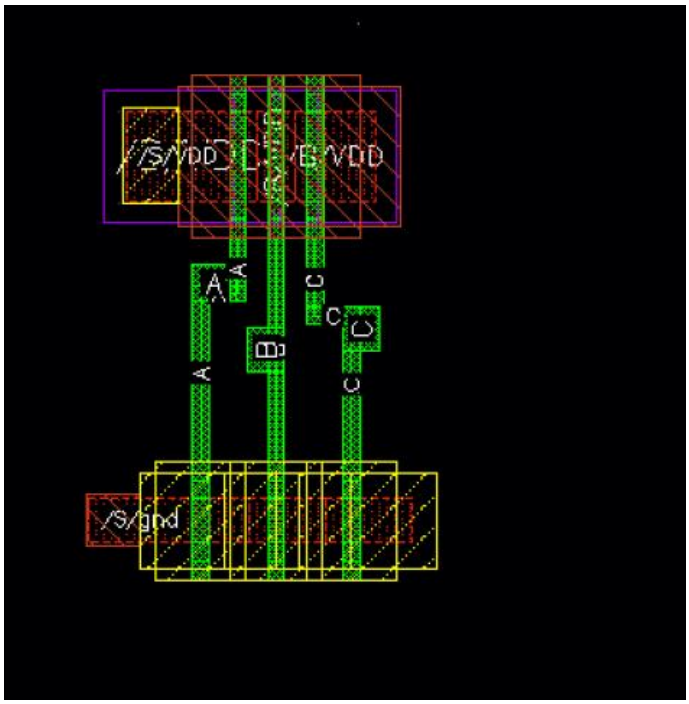

Fig 21: After providing P+ implant

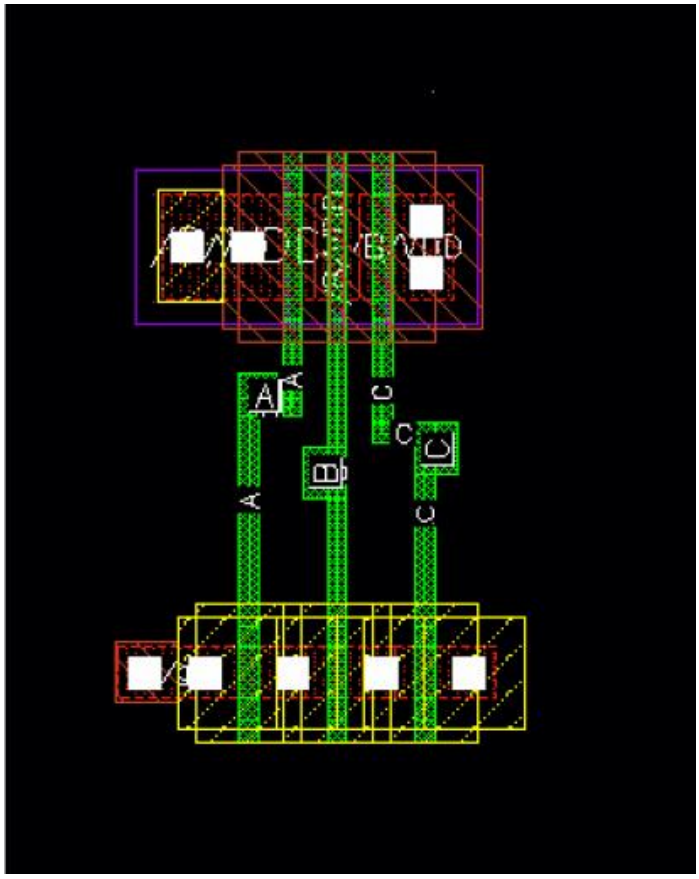

Fig 22: Putting in the contract window

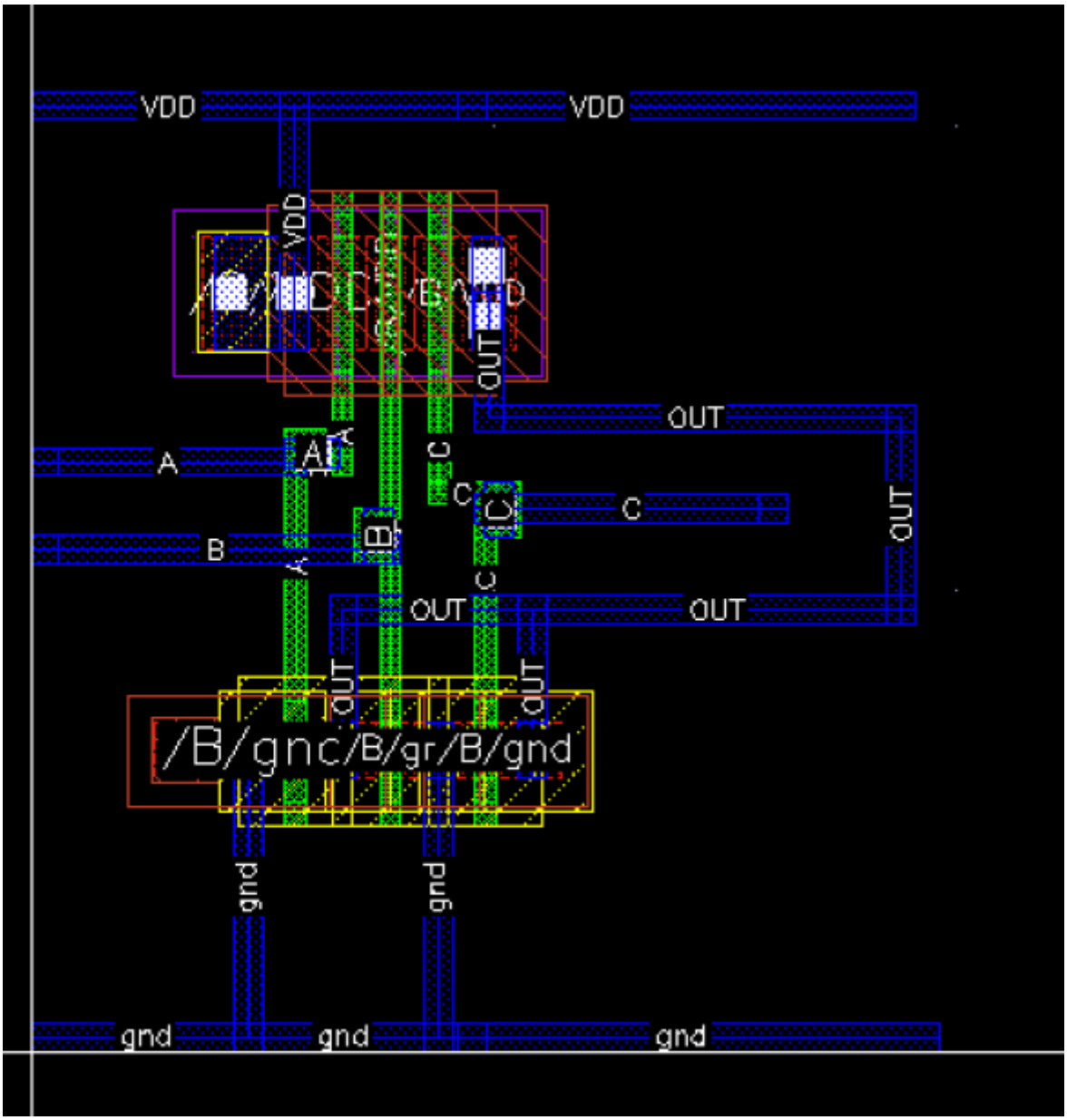

Fig 23: Final layout after providing connection with metal layer1

Comments about the 45 nm technology.

The 45 nm CMOS technology was a major leap forward in semiconductor manufacturing introducing innovations like high-K metal gates to reduce gate leakge and improve performance. With a smaller feature size, it enabled higher transistor density, resulting in faster processors and more efficient power usage. This technology allowed for operating voltages around 1.V reducing overall power consumption. Challenges including managing short-channel effects and variability. Which were mitigated through advance strain engineering and precise. lithography.

Conclusion.

This project successfully designed and implemented a 3 input NOR gate using 45 nm CMOS technology, showcasing the efficiency of advanced semiconductor processes. The layout optimization and adherence to fabrication and requirements ensured functionality and reliability. By leveraging low power and high-density design techniques the project highlights the potential of 45 nm technology in modern digital circuits and provides insights for future advancements in VLSI systems.