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# INVERTER LAYOUT PROJECT

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Layout and Schematic Images & Results



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In this project, I was able to create an inverter based on the following specifications:

- $W_P$ : 1.4  $\mu\text{m}$
- $W_N$ : 1.0  $\mu\text{m}$
- $C_{LOAD}$ : 22 fF

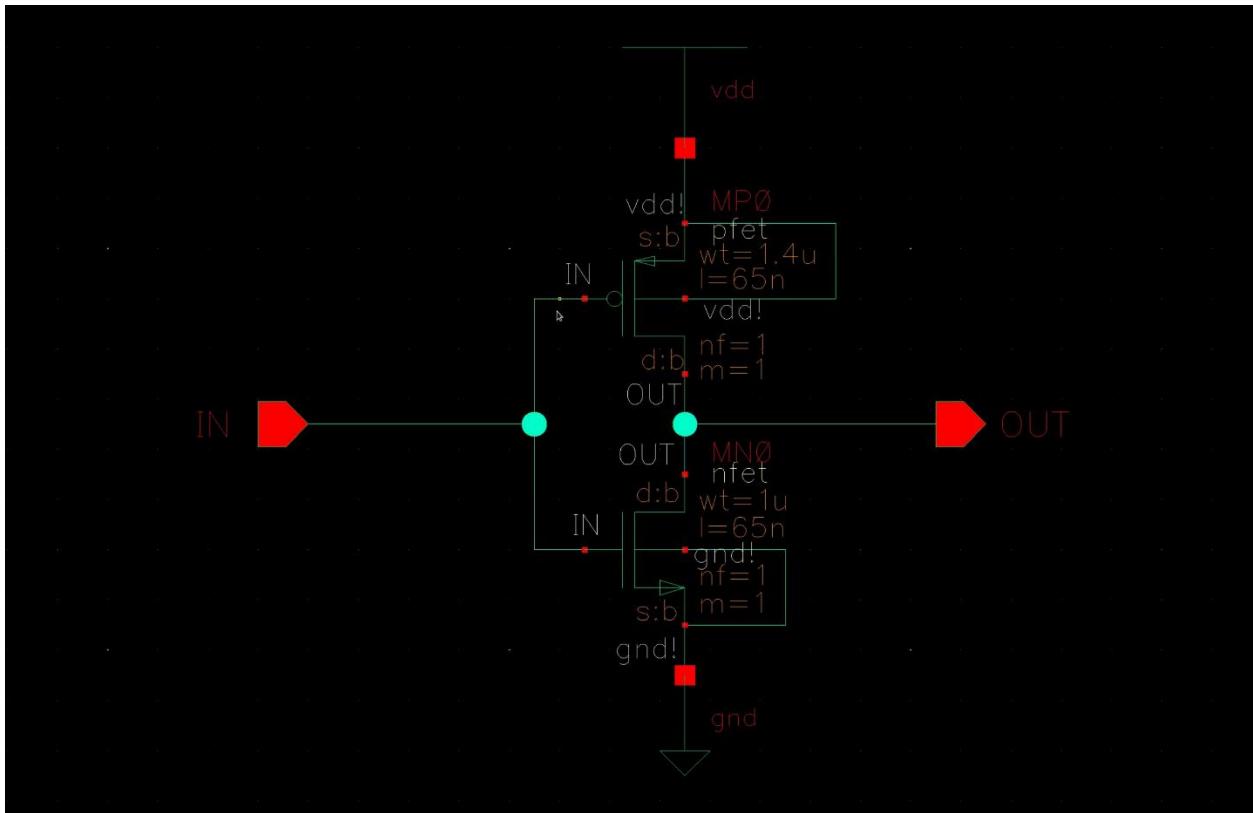


Figure 1: Inverter Schematic

With my design, I was able to achieve a height and width of 3.42  $\mu\text{m}$  by 0.705  $\mu\text{m}$ , measuring from the outer edges of VDD to GND.

The pin pitch of the in and out pads is 0.26  $\mu\text{m}$ ,

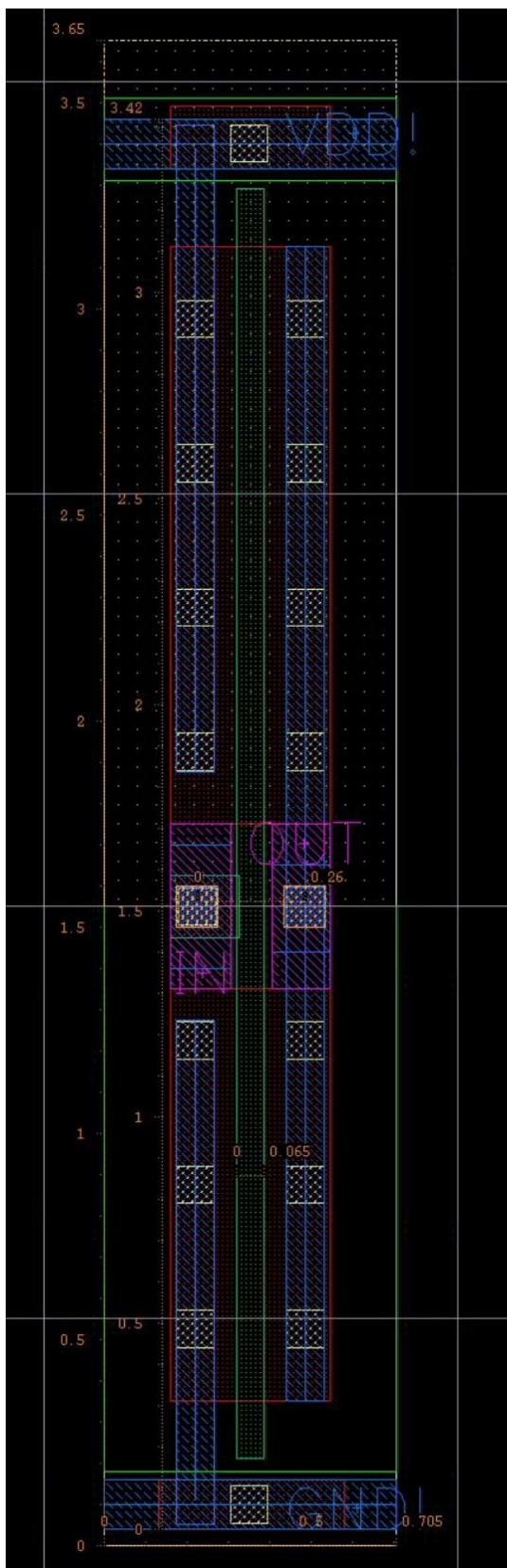


Figure 2: Inverter Layout

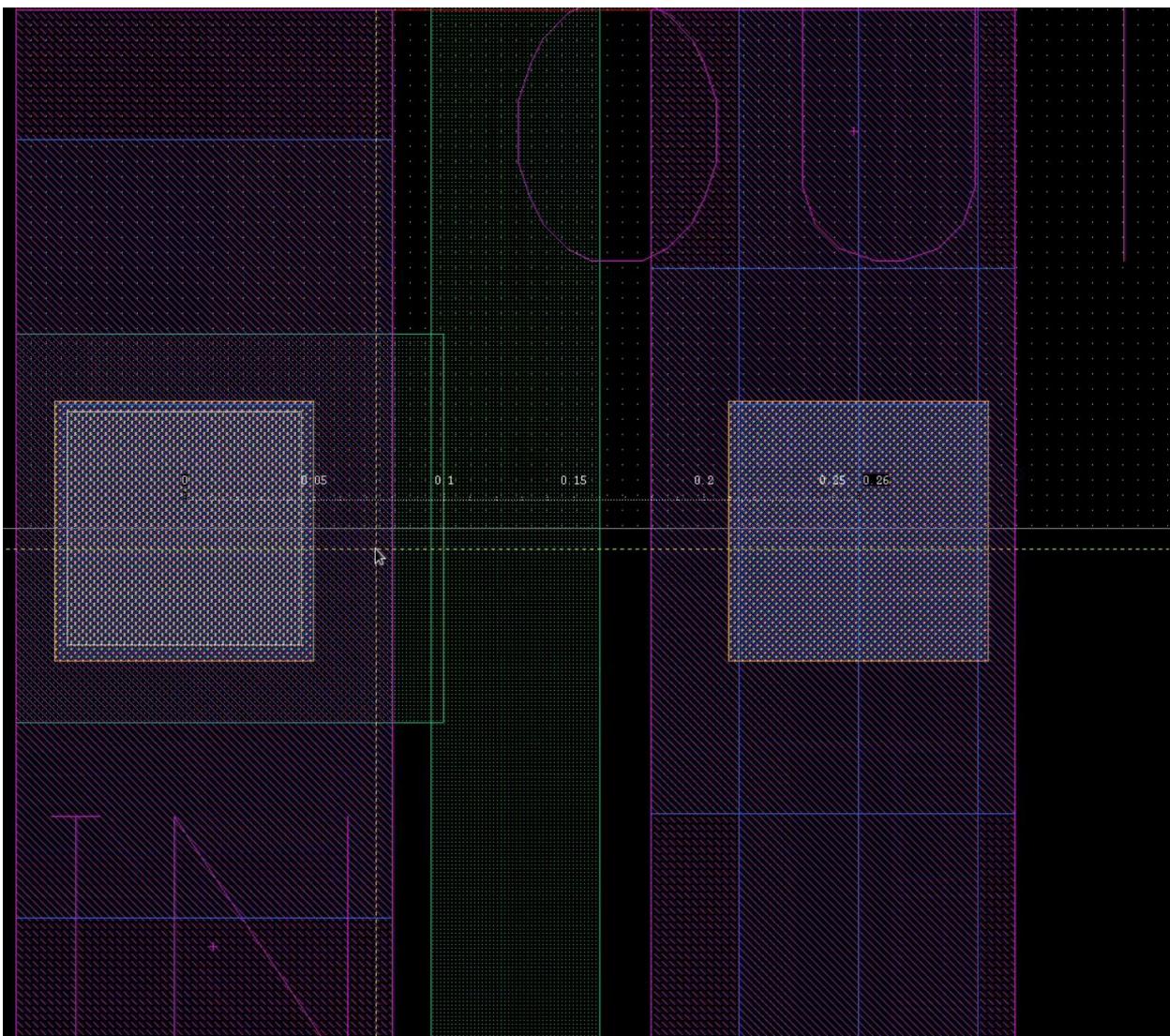


Figure 3: Pin pitch of  $0.26 \mu\text{m}$

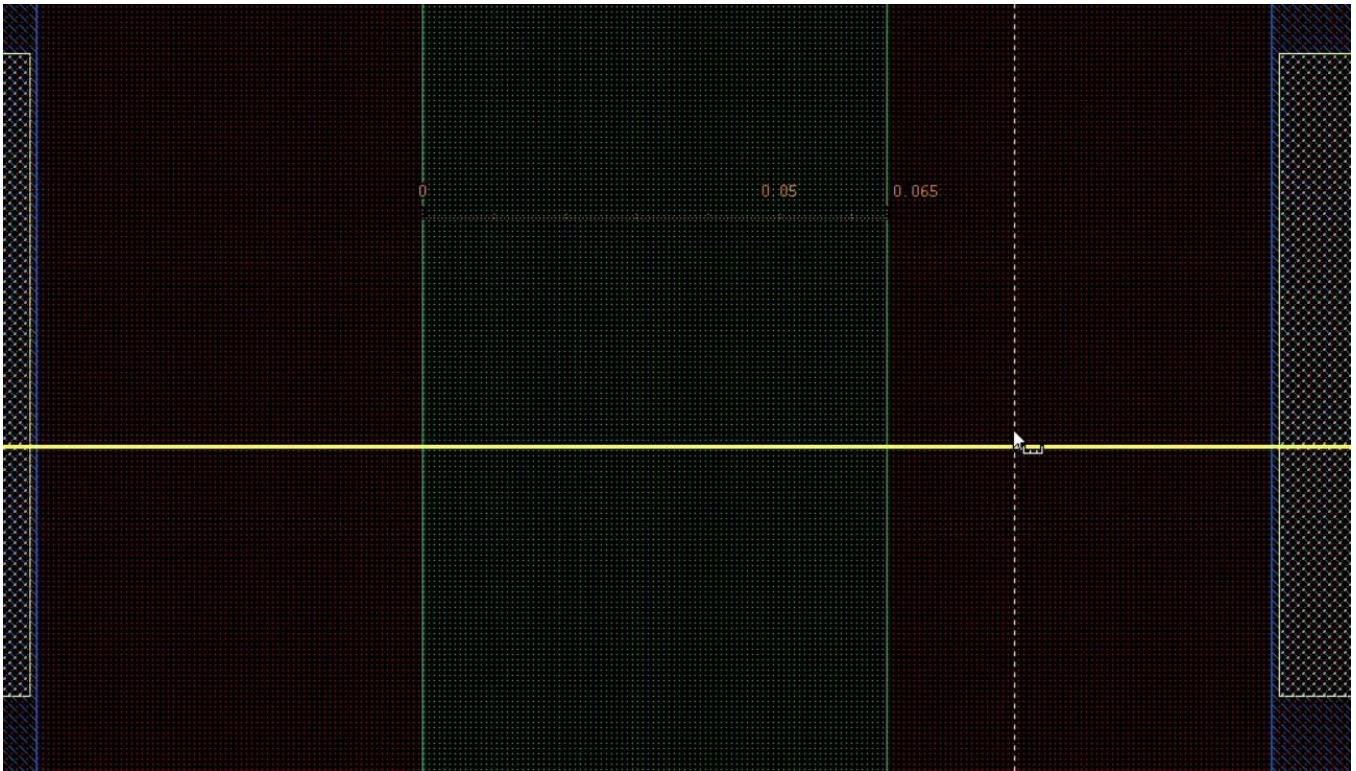


Figure 4: Gate Width

```

5008 :.res
      RULECHECK GRESD25d ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD26 ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD27 ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD30 ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD34 ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD34a ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD34b ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD34c ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD39 ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD39a ..... TOTAL Result Count = 0 (0)
      RULECHECK GRESD40 ..... TOTAL Result Count = 0 (0)

      ---- RULECHECK RESULTS STATISTICS (BY CELL)
      ----
      ---- SUMMARY
      ----
      TOTAL CPU Time:          0
      TOTAL REAL Time:         1
      TOTAL Original Layer Geometries: 78 (78)
      TOTAL DRC RuleChecks Executed: 2076
      TOTAL DRC Results Generated:   0 (0)

      Edit Row 3838 Col 39

```

Figure 5: DRC Summary

```

#####
##          C A L I B R E      S Y S T E M      ##
##          L V S      R E P O R T      ##
#####
REPORT FILE NAME:           inv.lvs.report
LAYOUT NAME:                /home/eng/m/mxi240020/cad/gf65/inv.sp ('inv')
SOURCE NAME:                /home/eng/m/mxi240020/cad/gf65/inv.src.net ('inv')
RULE FILE:                  /home/eng/m/mxi240020/cad/gf65/_Calibre_LVS_rules_
CREATION TIME:              Thu Oct 10 15:51:17 2024
CURRENT DIRECTORY:          /home/eng/m/mxi240020/cad/gf65
USER NAME:                  mxi240020
CALIBRE VERSION:            v2013.2_18.13    Thu May 16 13:38:27 PDT 2013

OVERALL COMPARISON RESULTS

#
#          #####
#          #      CORRECT      #
#          #          #
#          #####
#          #      *      *
#          #      |      /
#          #####
***** CELL SUMMARY *****
Result      Layout      Source
-----      -----      -----
CORRECT     inv         inv


```

Figure 6: LVS Report

Using HSpice, I was able to show the inverter has the following characteristics:

- Delay:
  - o  $t_{pHL}$ : 40.6 ps
  - o  $t_{pLH}$ : 60.9 ps
- Slew Rate:
  - o  $t_{HL}$ , 20 to 80%: 44.1 ps
  - o  $t_{LH}$ , 80 to 20%: 75.1 ps

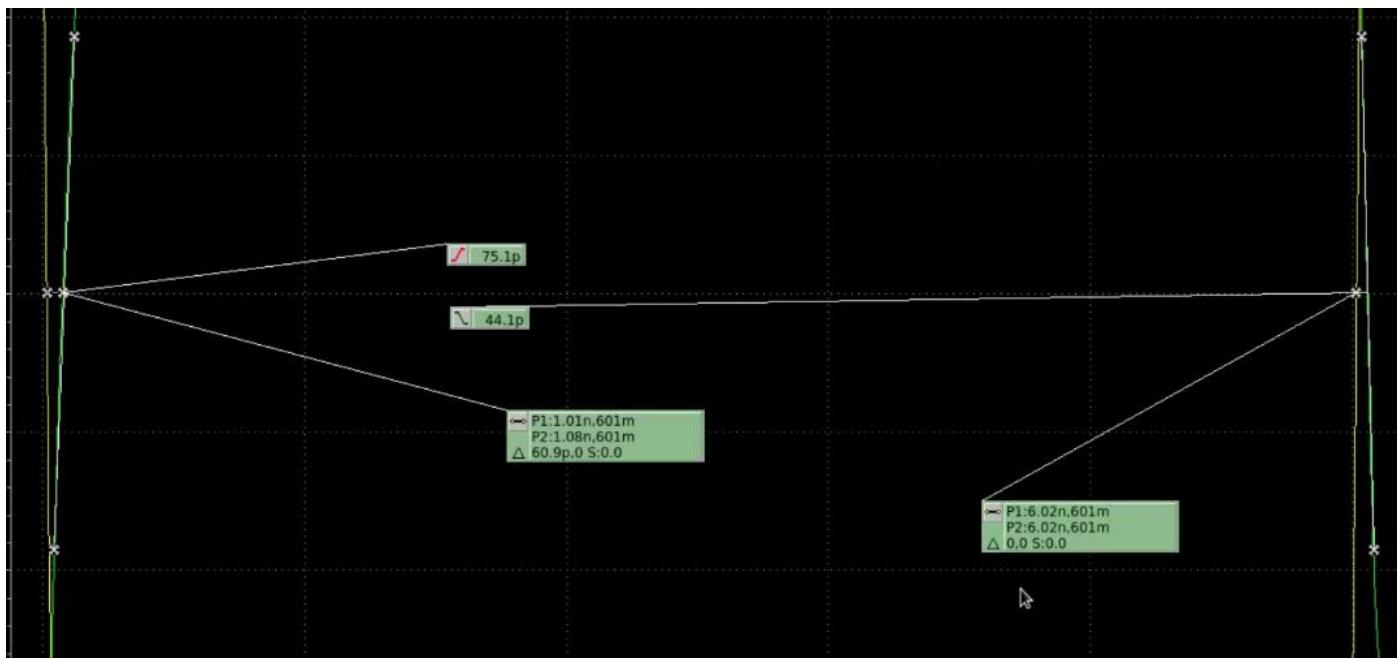


Figure 7: Slew and Delay

## Hspice Test Setup File

```
***** inverter test *****

.include
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_d1064_11_20160415/models/YI-
SM00030/Hspice/models/design.inc"

$ /home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp
.include "/home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp"

.option post runlvl=0

xmytele GND! OUT VDD! IN inv

vdd VDD! GND! 1.2v
vin IN GND pwl(0ns 1.2v 1ns 1.2v 1.03ns 0 6ns 0v 6.03ns 1.2v 7.2ns 1.2v)
cout OUT GND! 22f

$ my Transient analysis
.tr 100ps 7.2ns
.tr 100ps 7.2ns sweep WP 1u 9U 0.5u

.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val= 0.6v fall = 1

.measure tavg param = '(trise + tfall)/2'
.measure tdiff param = 'abs(trise - tfall)'
.measure delay param = 'max(trise, tfall)'

.end
```

## Extracted Spice Netlist

Inv.pex.sp

```
* File: /home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp
* Created: Sun Oct 6 17:56:57 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.include "/home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp.pex"
.subckt inv GND! OUT VDD! IN
*
* IN IN
* VDD! VDD!
* OUT OUT
* GND! GND!
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX AREA=2.15e-12
+ PERIM=6.3e-06
XMMN0 N_OUT_MMN0_d N_IN_MMN0_g N_GND!_MMN0_s N_GND!_D0_noxref_pos NFET L=6.5e-08
+ W=1e-06 AD=1.61e-13 AS=1.56e-13 PD=2.322e-06 PS=2.312e-06 NRD=0.1 NRS=0.095
+ M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=1.56e-07 SB=1.61e-07 SD=0
+ PANW1=6.5e-15 PANW2=3.25e-15 PANW3=3.25e-15 PANW4=3.25e-15 PANW5=3.25e-15
+ PANW6=6.5e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=1.3e-14 PANW10=0
XMMP0 N_OUT_MMP0_d N_IN_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6.5e-08
+ W=1.4e-06 AD=2.254e-13 AS=2.184e-13 PD=3.122e-06 PS=3.112e-06 NRD=0.0714286
+ NRS=0.0678571 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1 SA=1.56e-07
+ SB=1.61e-07 SD=0 PANW1=6.5e-15 PANW2=3.25e-15 PANW3=3.25e-15 PANW4=3.25e-15
+ PANW5=9.425e-14 PANW6=1.0075e-13 PANW7=2.6e-14 PANW8=2.6e-14 PANW9=5.2e-14
+ PANW10=4.875e-14
*
.include "/home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp.INV.pxi"
*
.ends
*
```

## Inv.pex.sp.pex

```
* File: /home/eng/m/mxi240020/cad/gf65/inv_LVS/inv.pex.sp.pex
* Created: Sun Oct  6 17:56:57 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
* Nominal Temperature: 27C
* Circuit Temperature: 27C
*
.subckt PM_INV%GND! 1 6 14 16 20
c27 14 0 4.40239e-19
r28 11 14 0.382777
r29 9 16 0.0289663
r30 9 11 0.0767497
r31 6 20 10
r32 4 16 0.0162764
r33 4 6 0.987955
r34 1 11 30
.ends

.subckt PM_INV%OUT 3 8 16 19 21 22
c34 16 0 1.70551e-19
r35 16 25 0.118479
r36 16 24 0.128621
r37 15 19 0.0398801
r38 15 16 1.7
r39 11 21 30
r40 8 11 0.868805
r41 8 25 0.77696
r42 8 21 10
r43 3 24 0.700008
r44 3 22 10
.ends

.subckt PM_INV%VDD! 1 6 17 22
r25 14 17 0.407065
r26 12 19 0.0289663
r27 12 14 0.0767497
r28 10 22 30
r29 6 10 0.868805
r30 6 22 10
r31 4 19 0.0162764
r32 4 10 0.55107
r33 1 14 30
.ends
```

```
.subckt PM_INV%IN 4 6 9 10 12 14 16 19 20
c44 20 0 1.20466e-19
c45 19 0 1.49221e-19
r46 20 23 25
r47 19 20 1.7
r48 16 19 0.0432845
r49 9 23 3.96633
r50 9 10 0.717752
r51 6 14 68.3465
r52 5 10 4.92266
r53 5 6 12.2047
r54 4 10 4.92266
r55 3 12 48.8189
r56 3 4 12.2047
.ends
```