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# PROJECT FOUR

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Combinational Gate Layout



NOVEMBER 8, 2024  
MARK IVEY  
UTD EECT 6325, Fall 2024

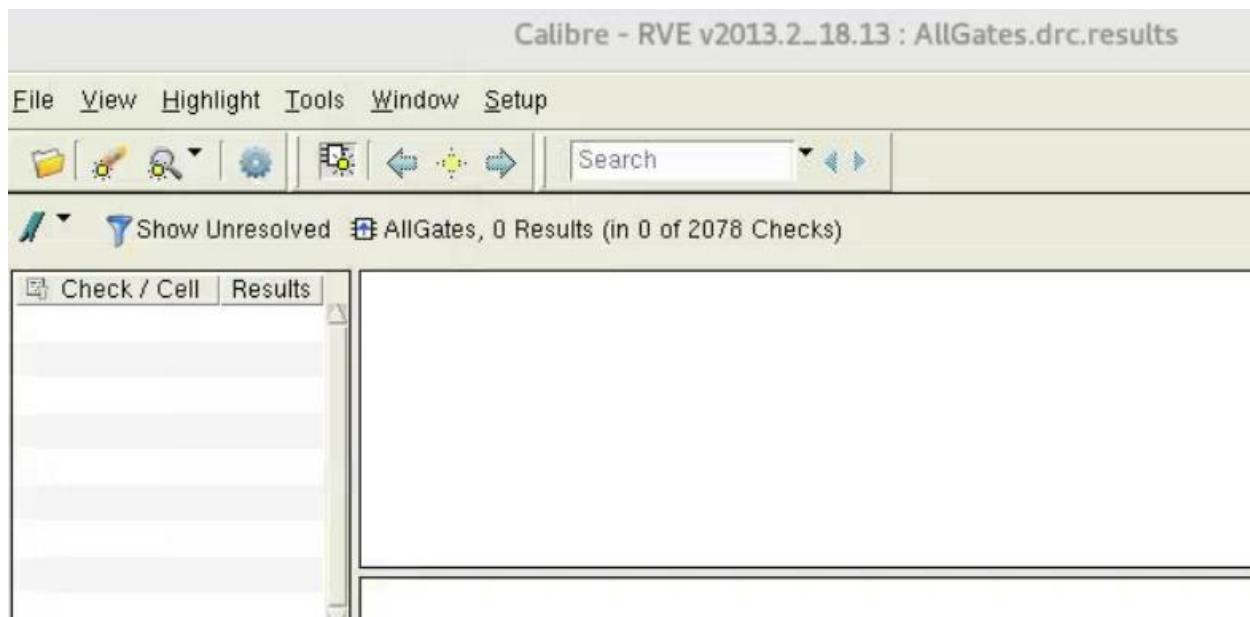
In this project, I did the schematic and layout for 16 different gates. They are as follows:

- 1) AOI22
- 2) AOI32
- 3) AOI41
- 4) AOI221
- 5) NAND2
- 6) NAND3
- 7) NAND4
- 8) INVETER
- 9) NOR4
- 10) NOR3
- 11) NOR2
- 12) OAI221
- 13) OAI41
- 14) OAI32
- 15) OAI22
- 16) XOR2

In this report, I will show the measurements of each gate, the abstract view, gate spacing, and the Hspice simulation results of  $t_{pHL}$ ,  $t_{pLH}$ ,  $t_{HL}$ , and  $t_{LH}$ . The PC spacing is  $0.262 \mu\text{m}$ , while metal 2 spacing, or the pin pitch, was set to  $0.26 \mu\text{m}$ .

## All Gates

DRC Results:



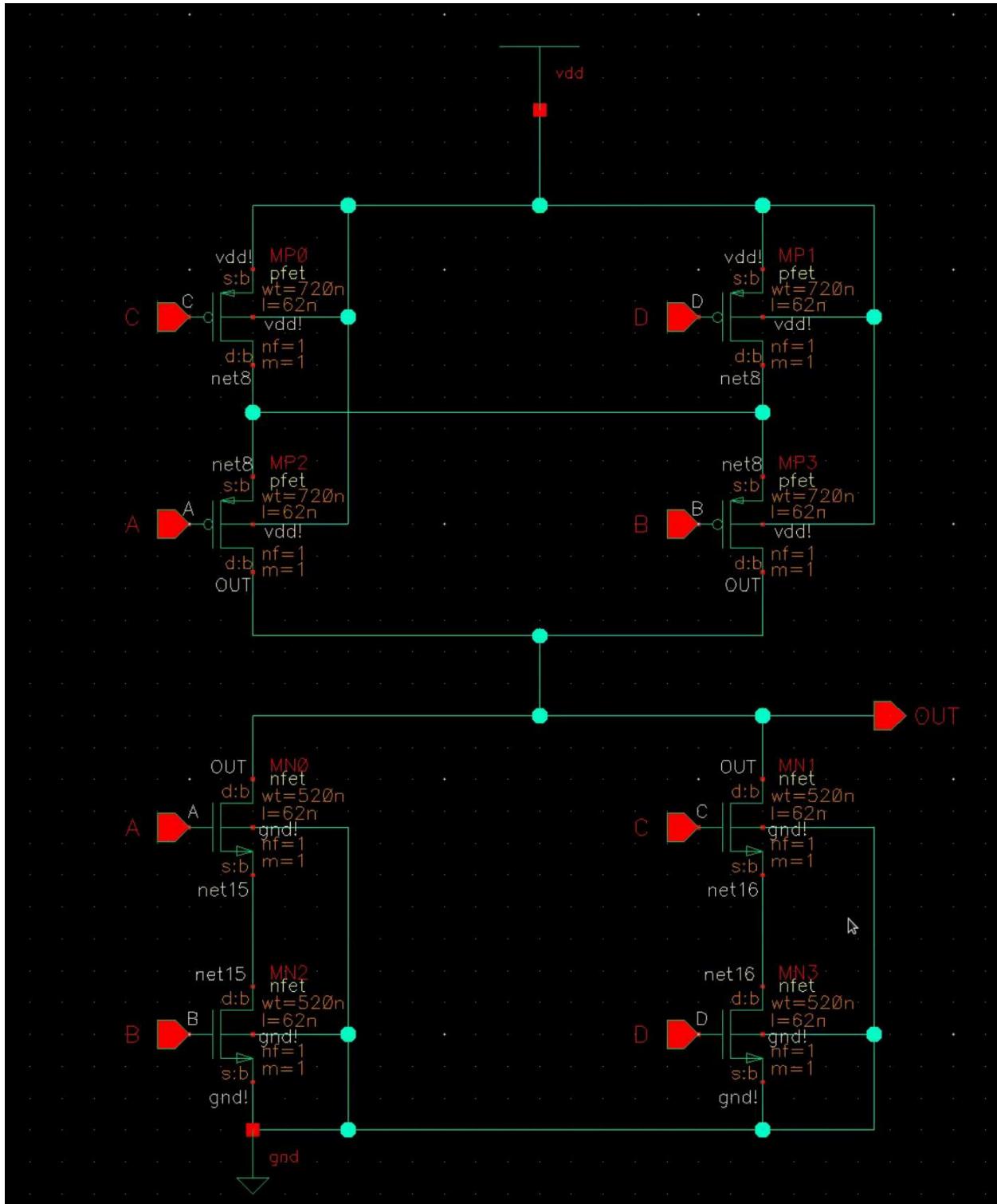
## Gates Together:

Note: After the technology file was restored on Thursday, I was unable to click into and show all the gates together. I don't know of a better way to show this.

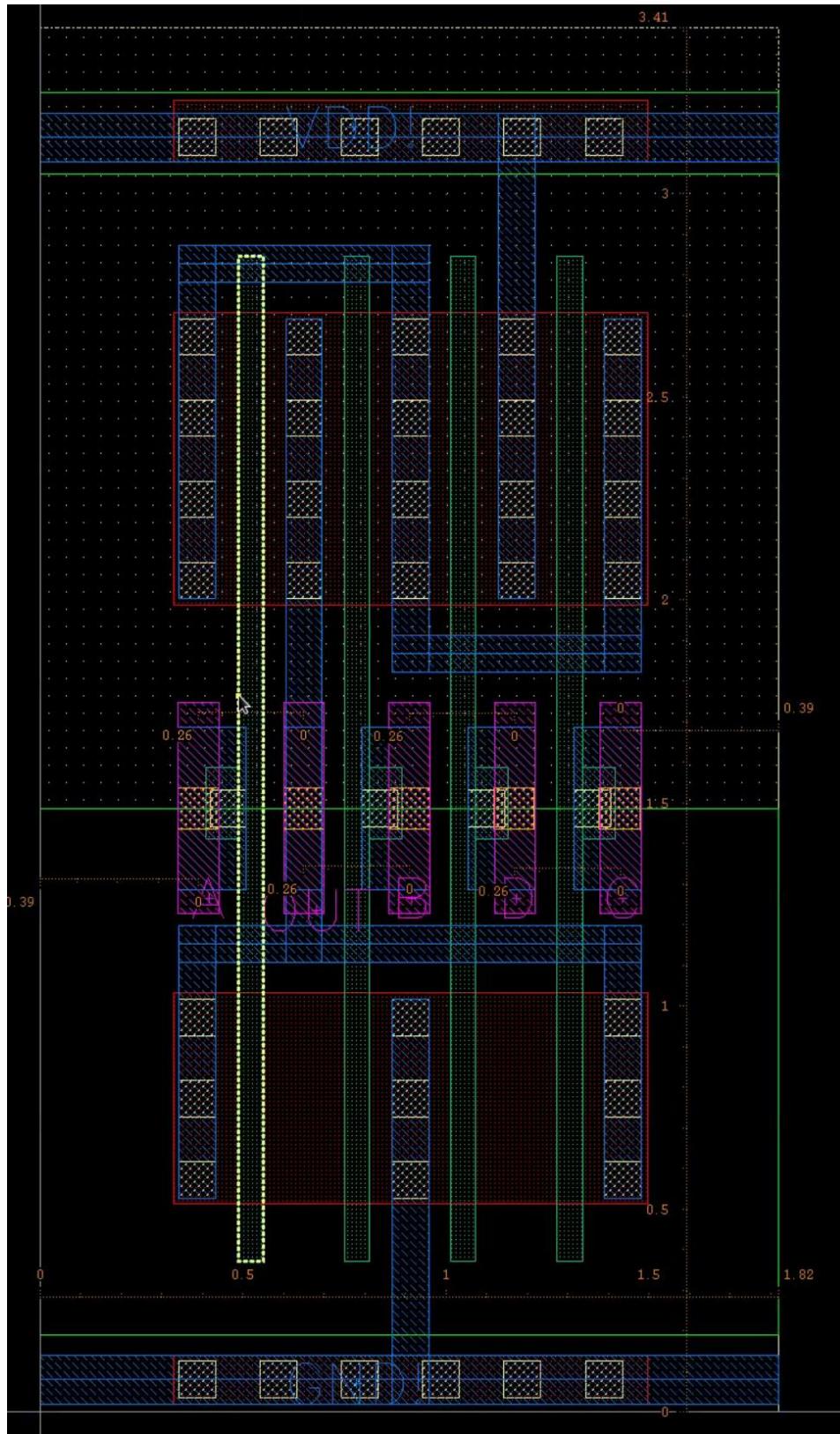


## AOI22

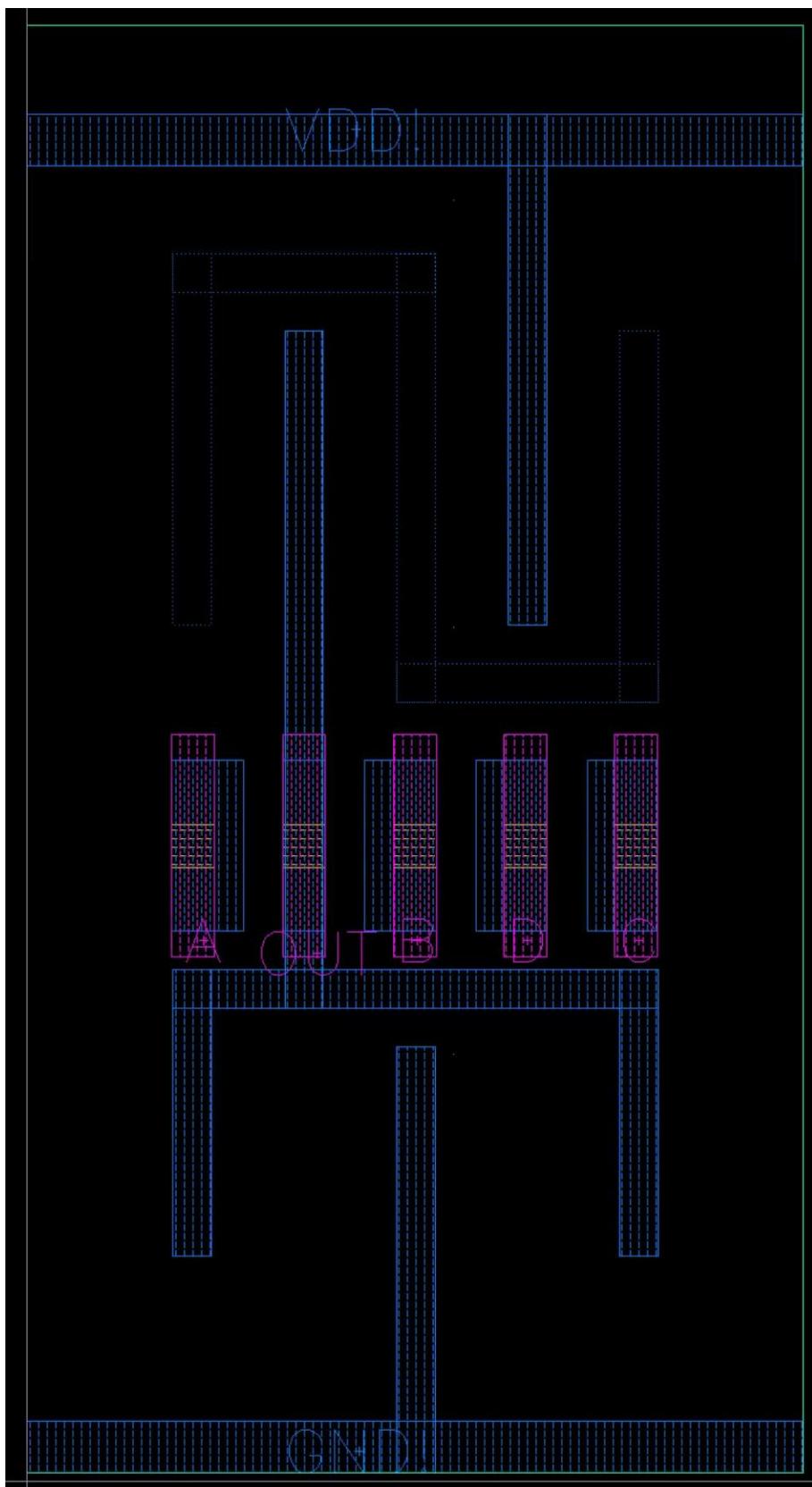
Schematic:



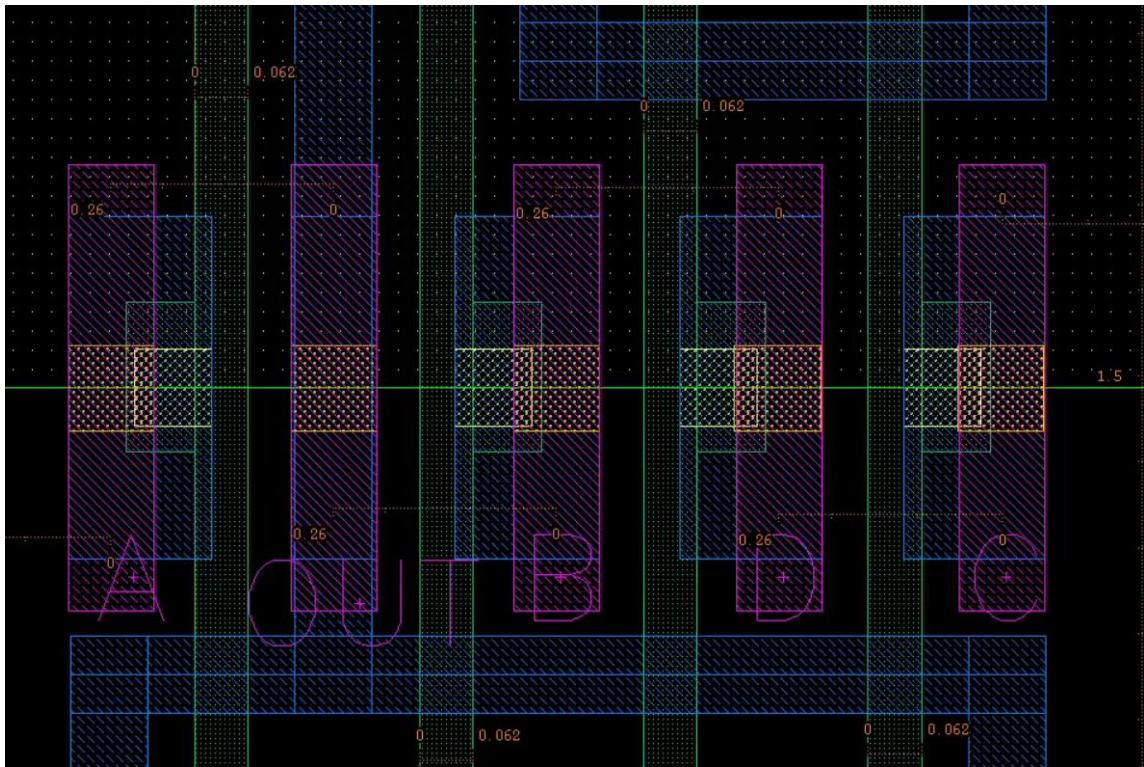
Layout:



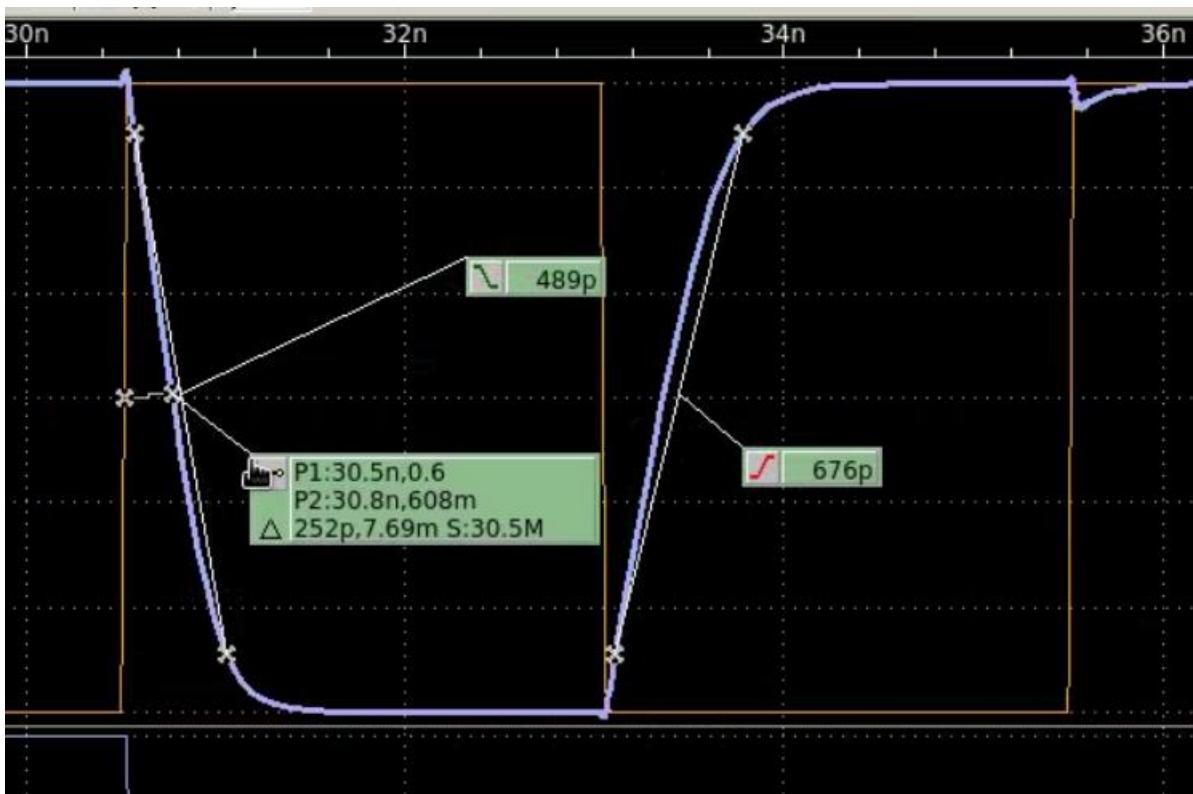
## Abstract View



Gate spacing:

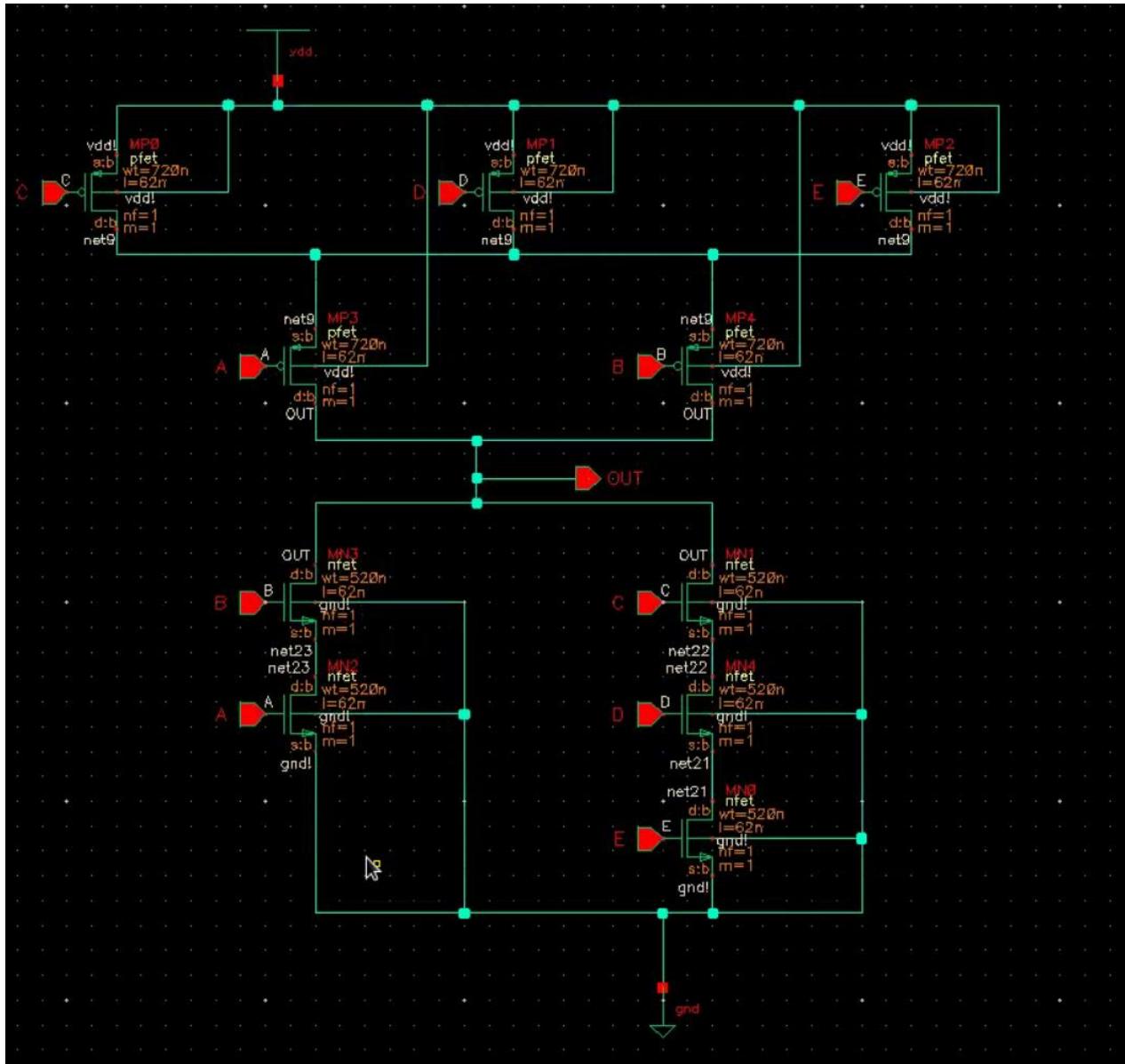


Hspice Simulation:

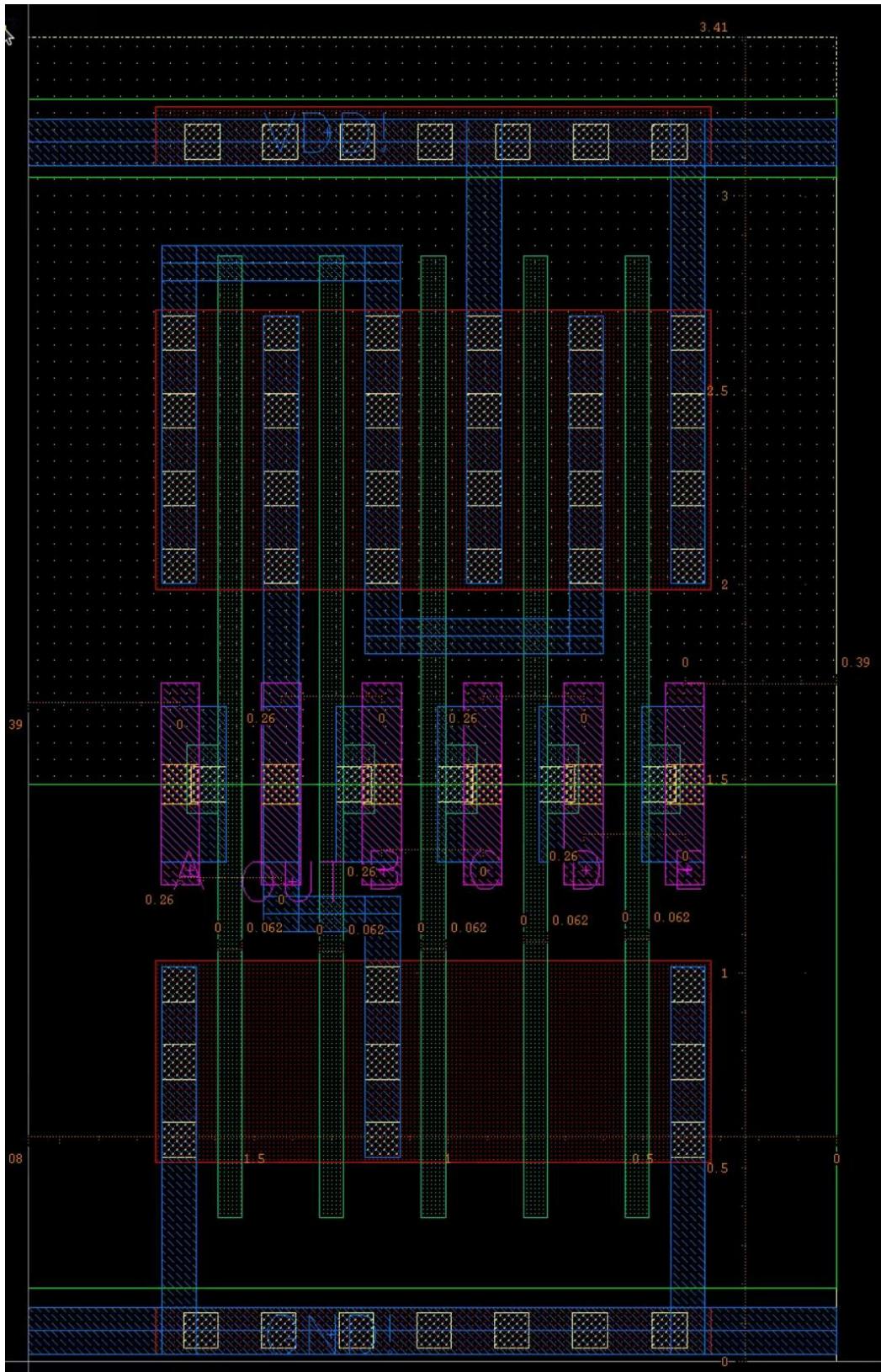


# AOI32

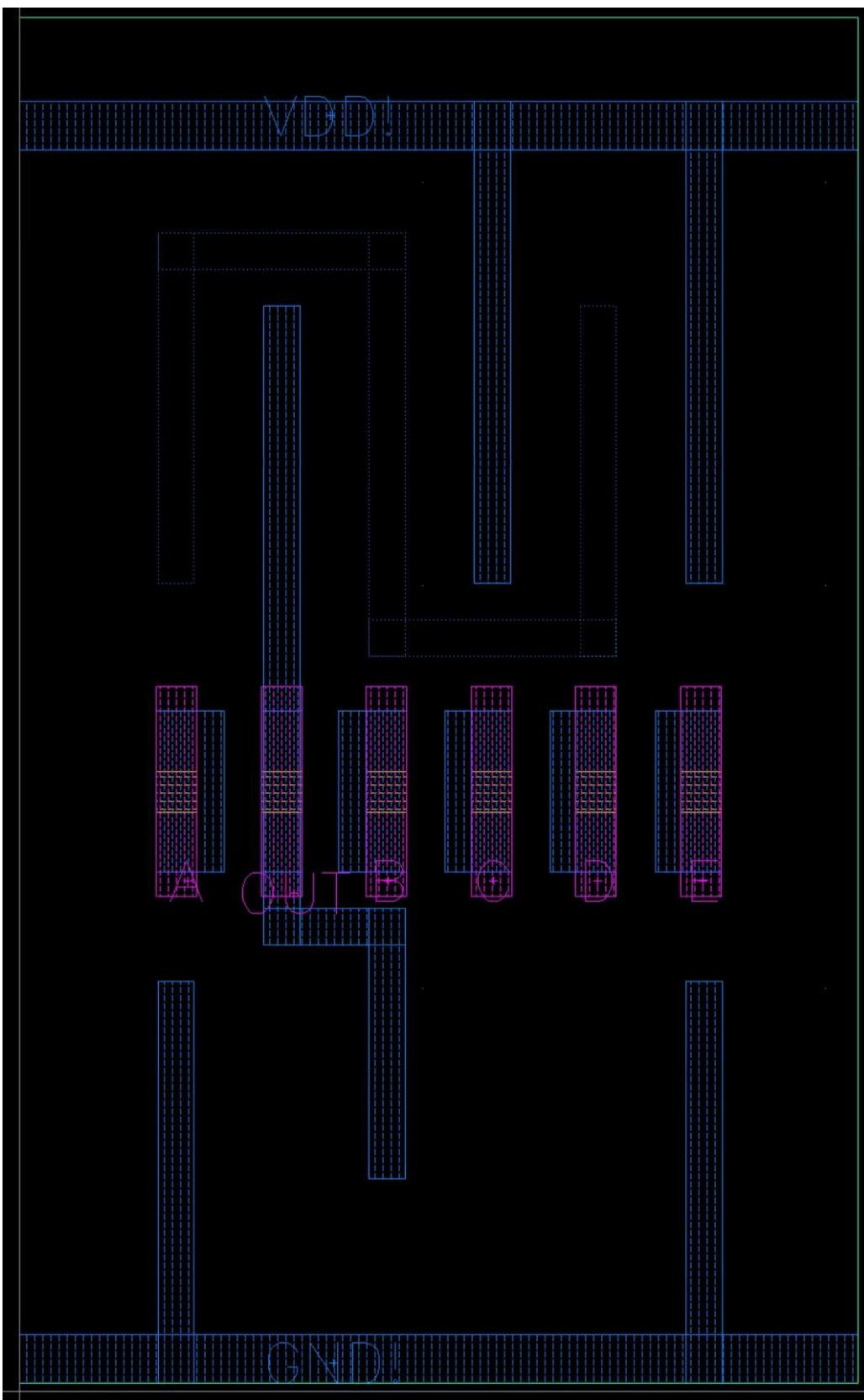
Schematic:



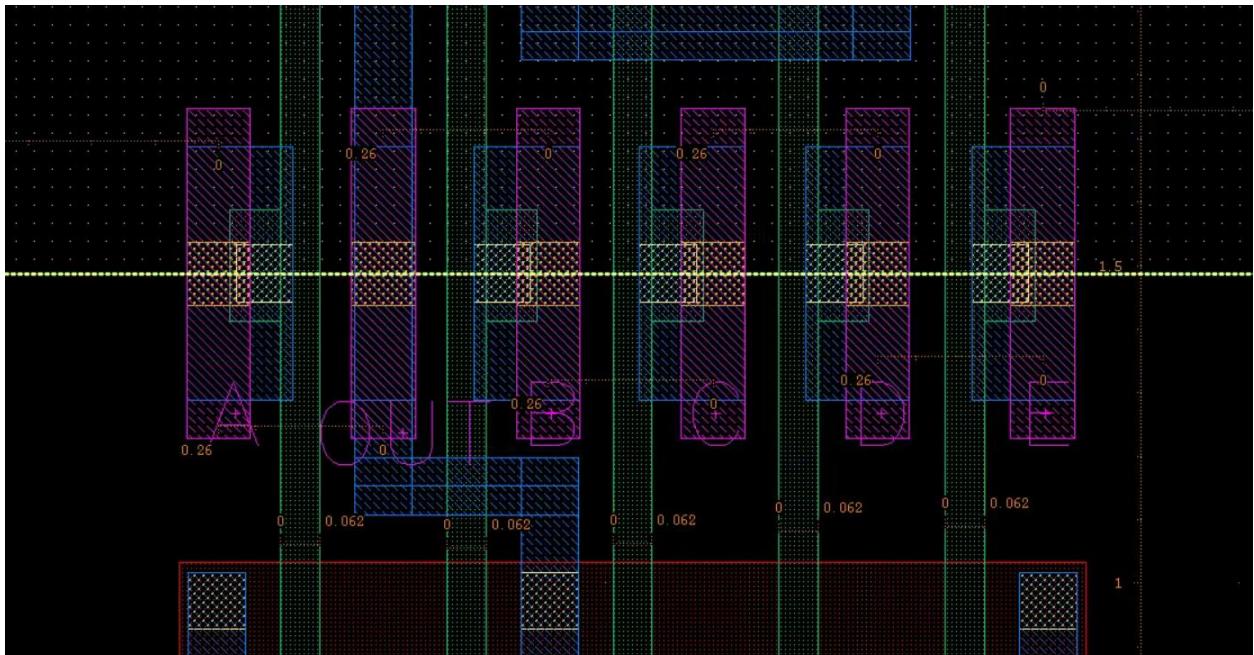
Layout:



Abstract View:



Gate spacing:

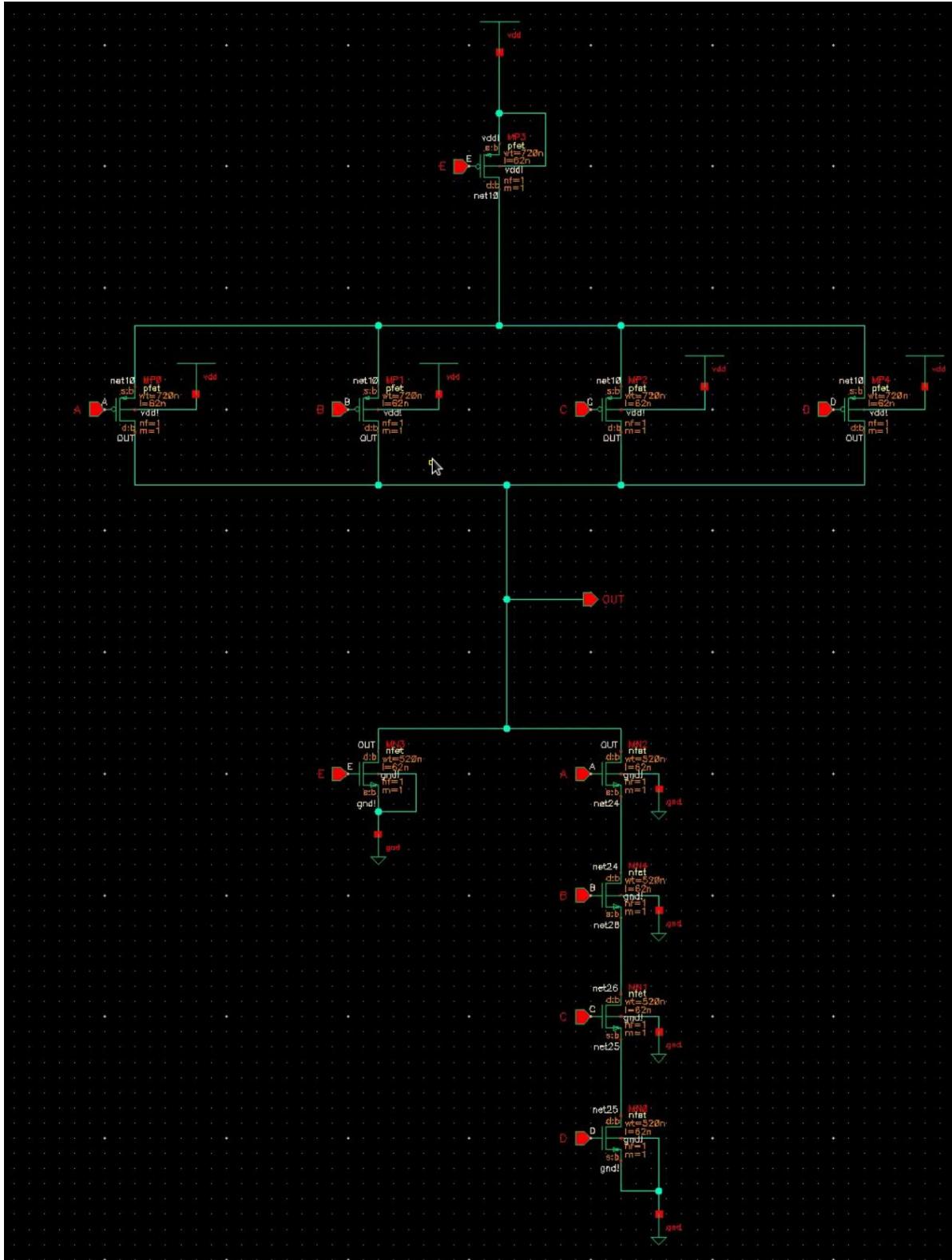


Hspice Simulation:

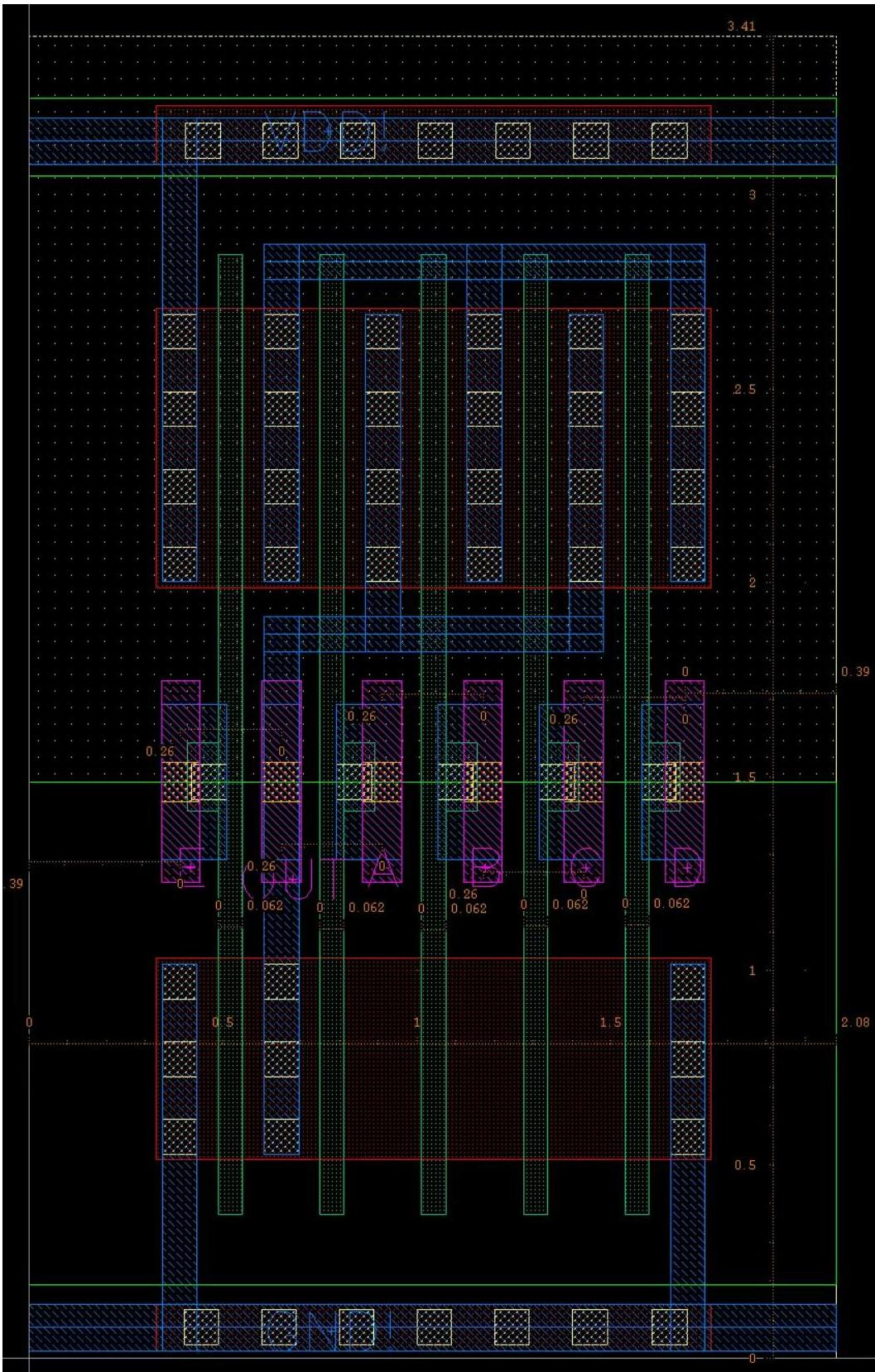


# AOI41

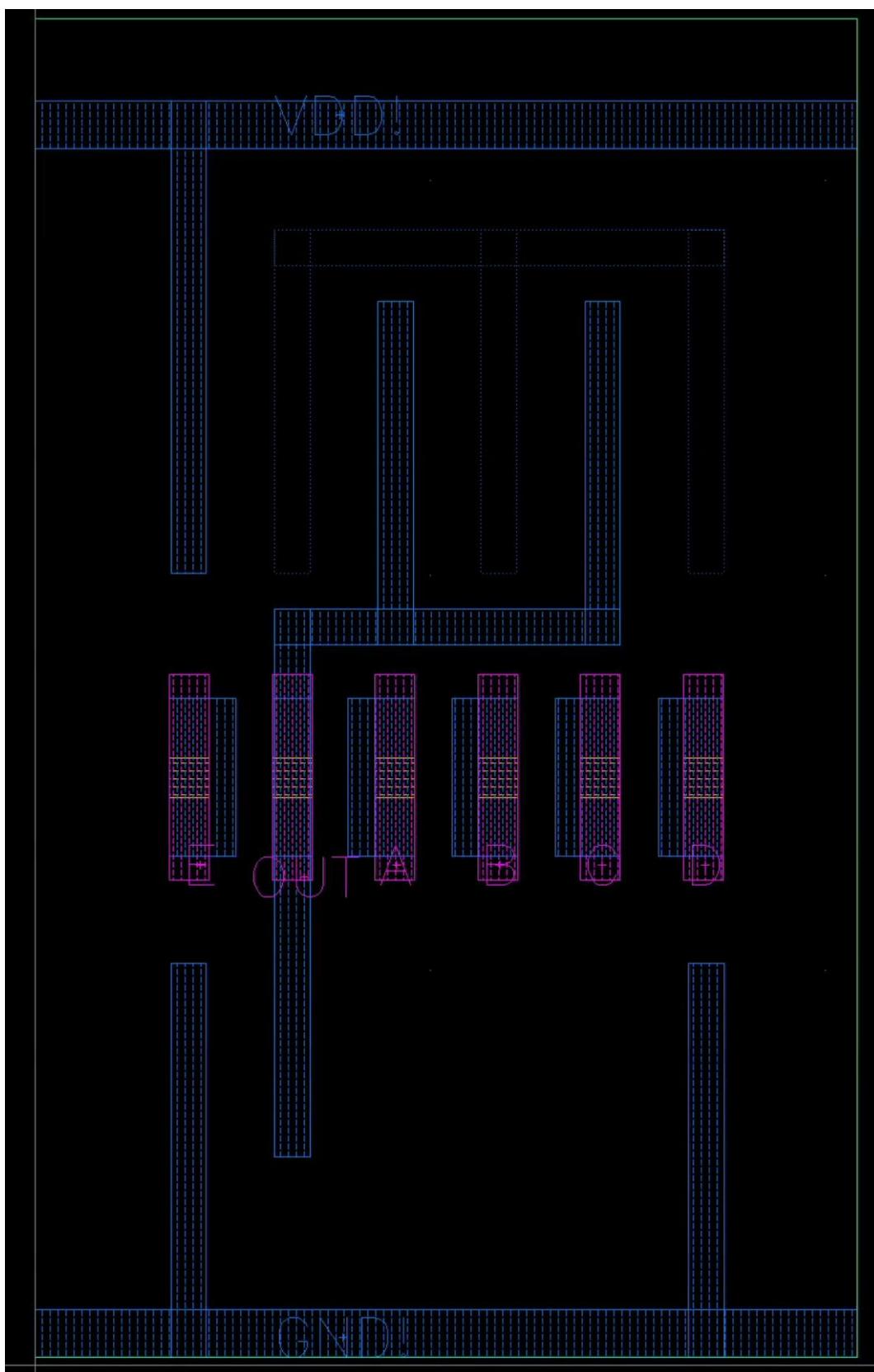
Schematic:



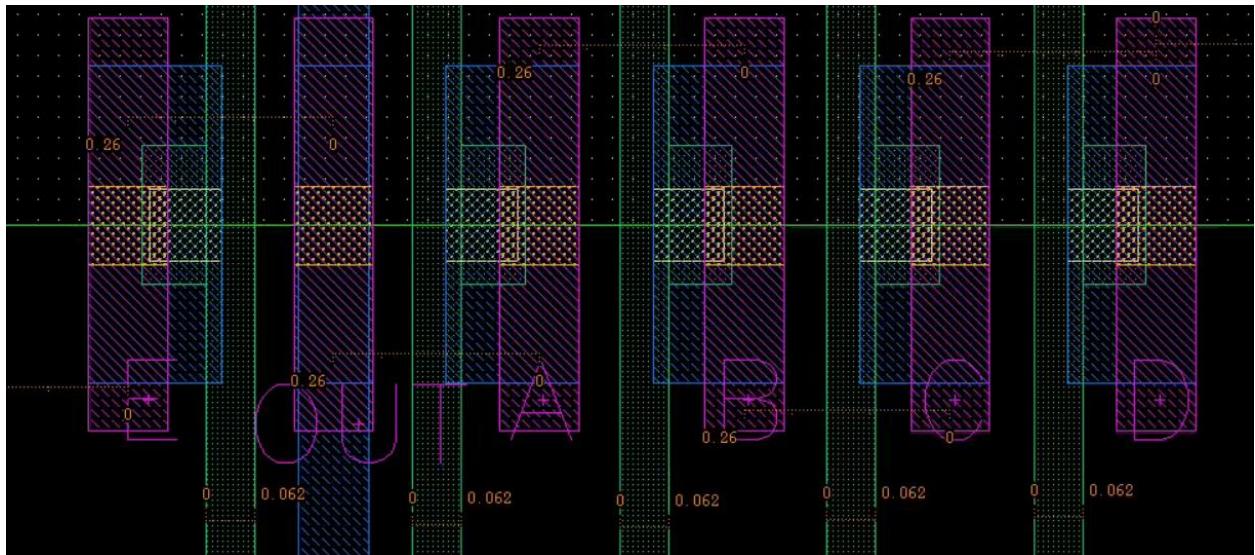
Layout:



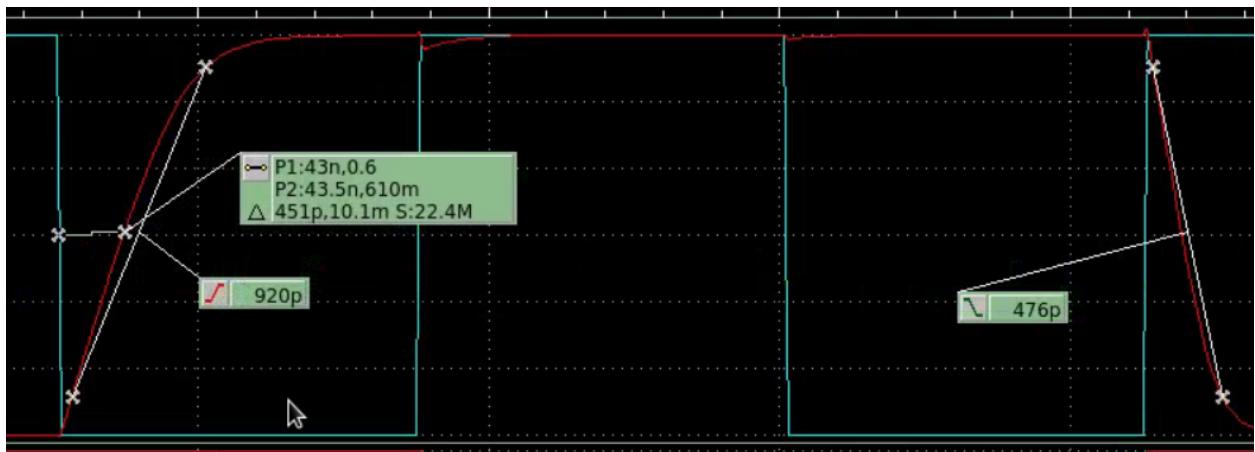
Abstract View:



Gate spacing:

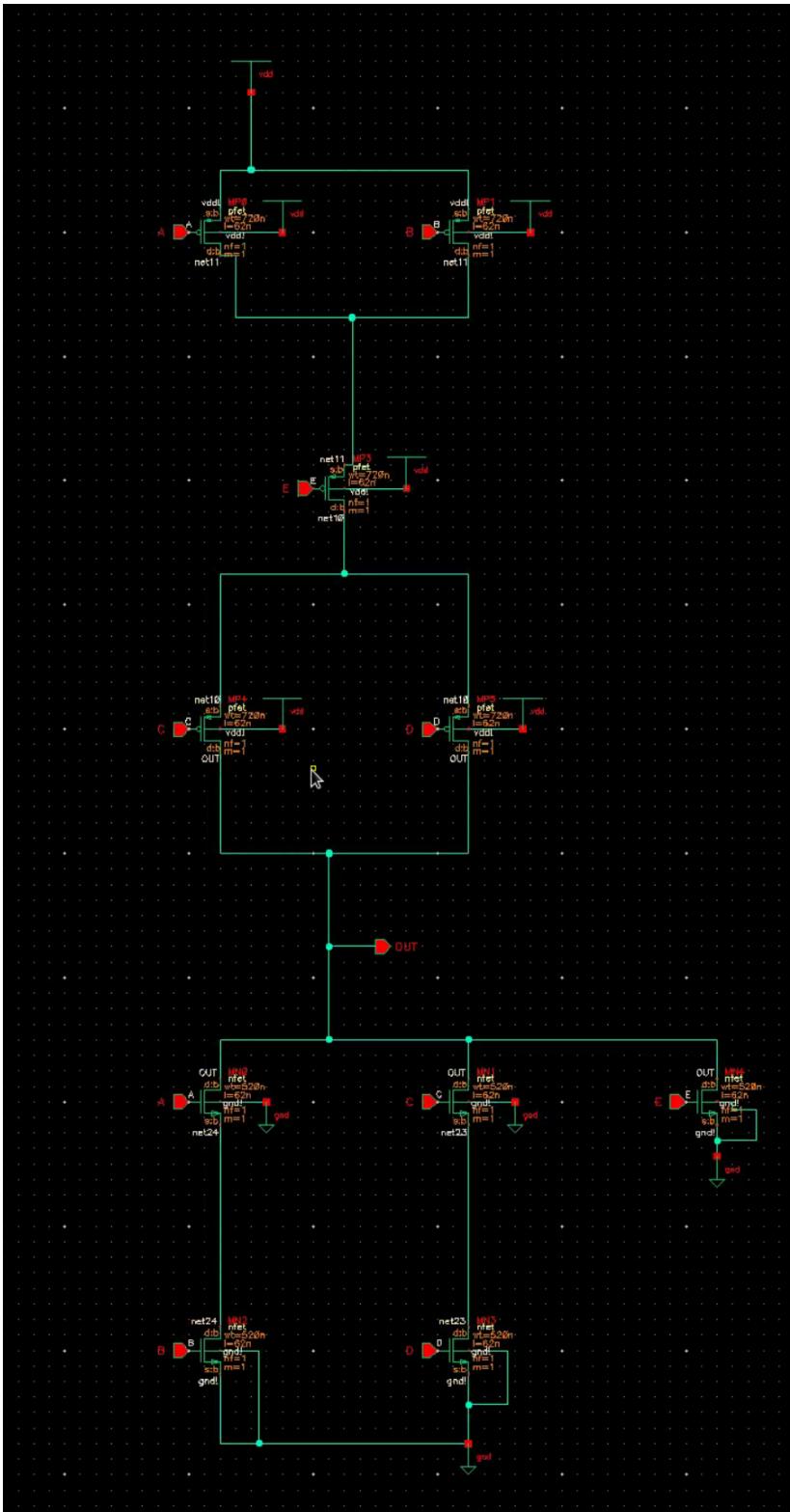


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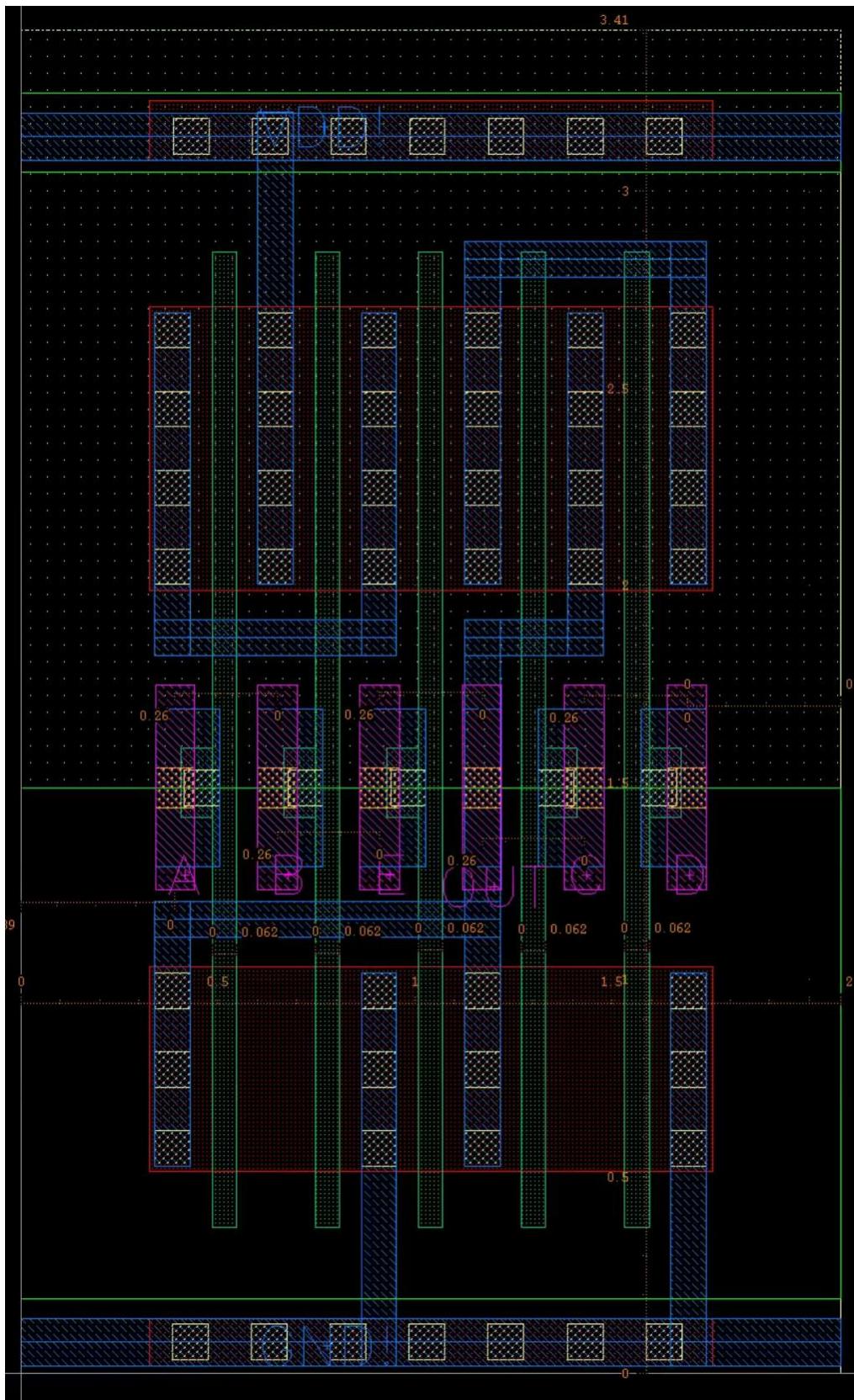


# AOI221

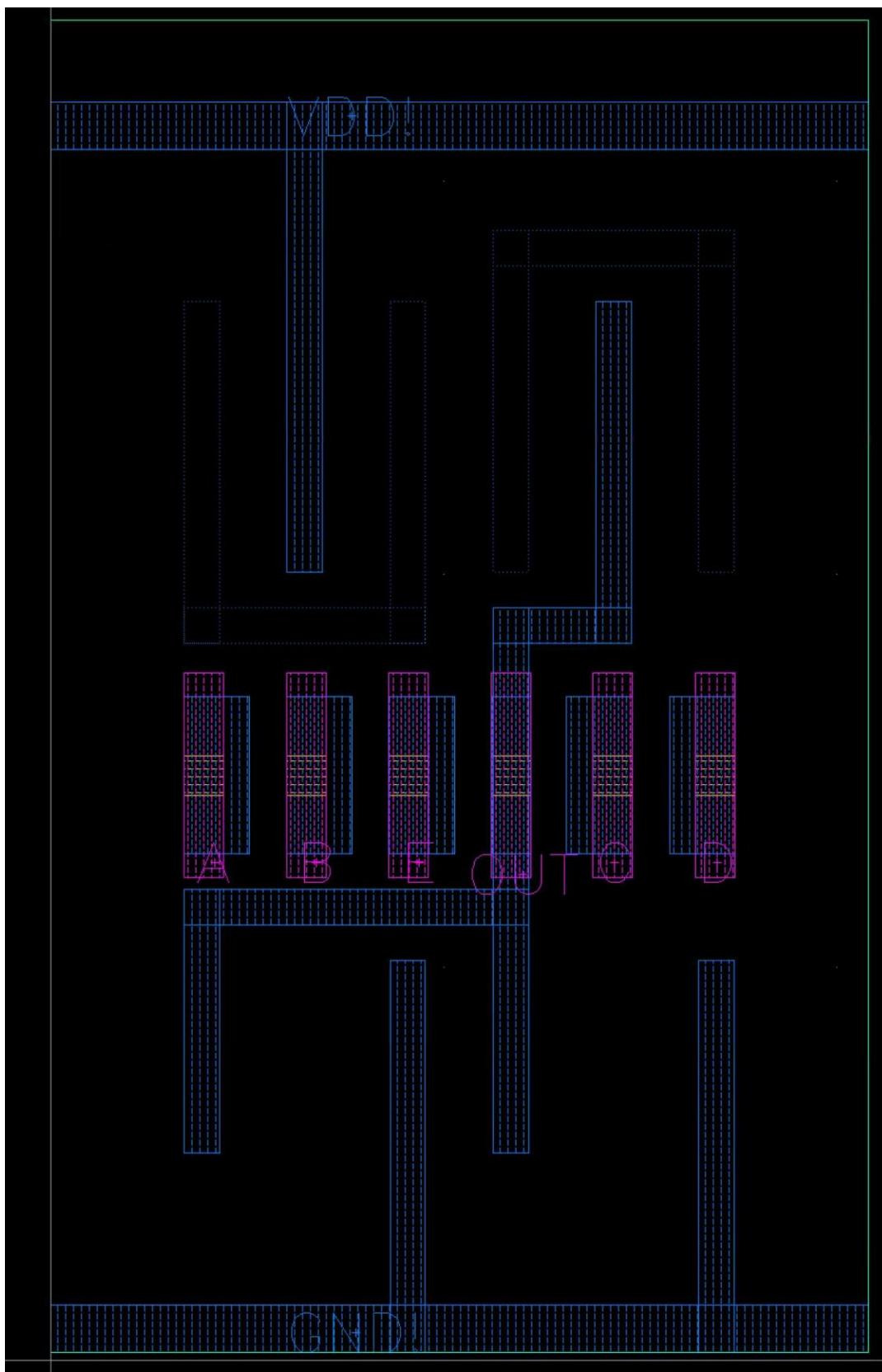
Schematic:



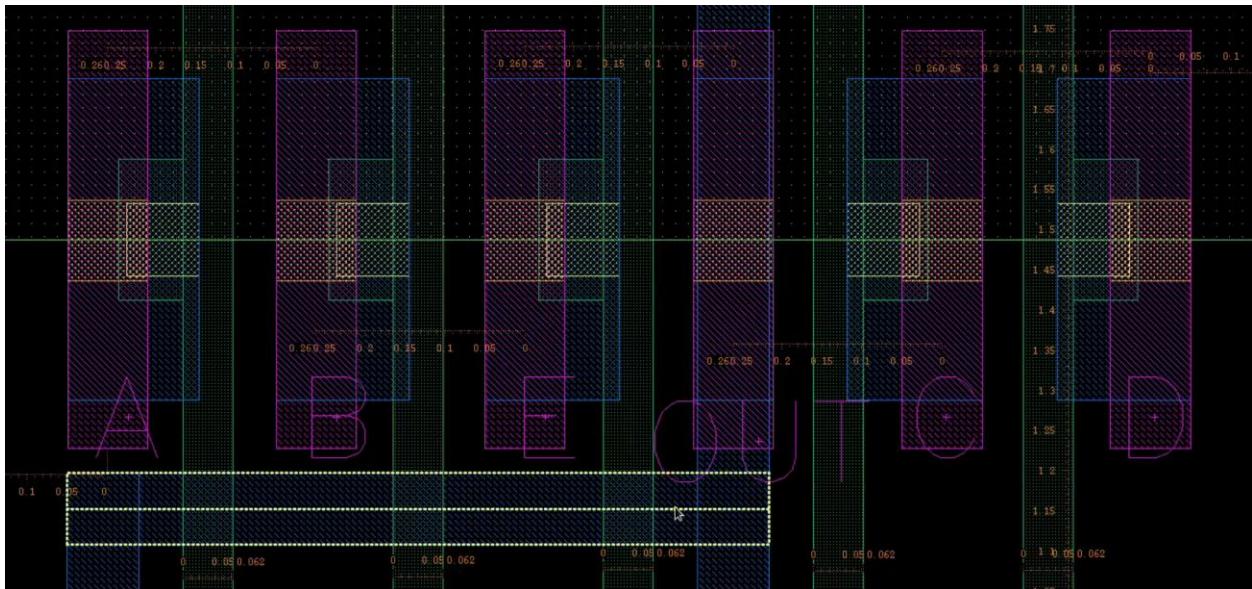
Layout:



Abstract View:



Gate spacing:

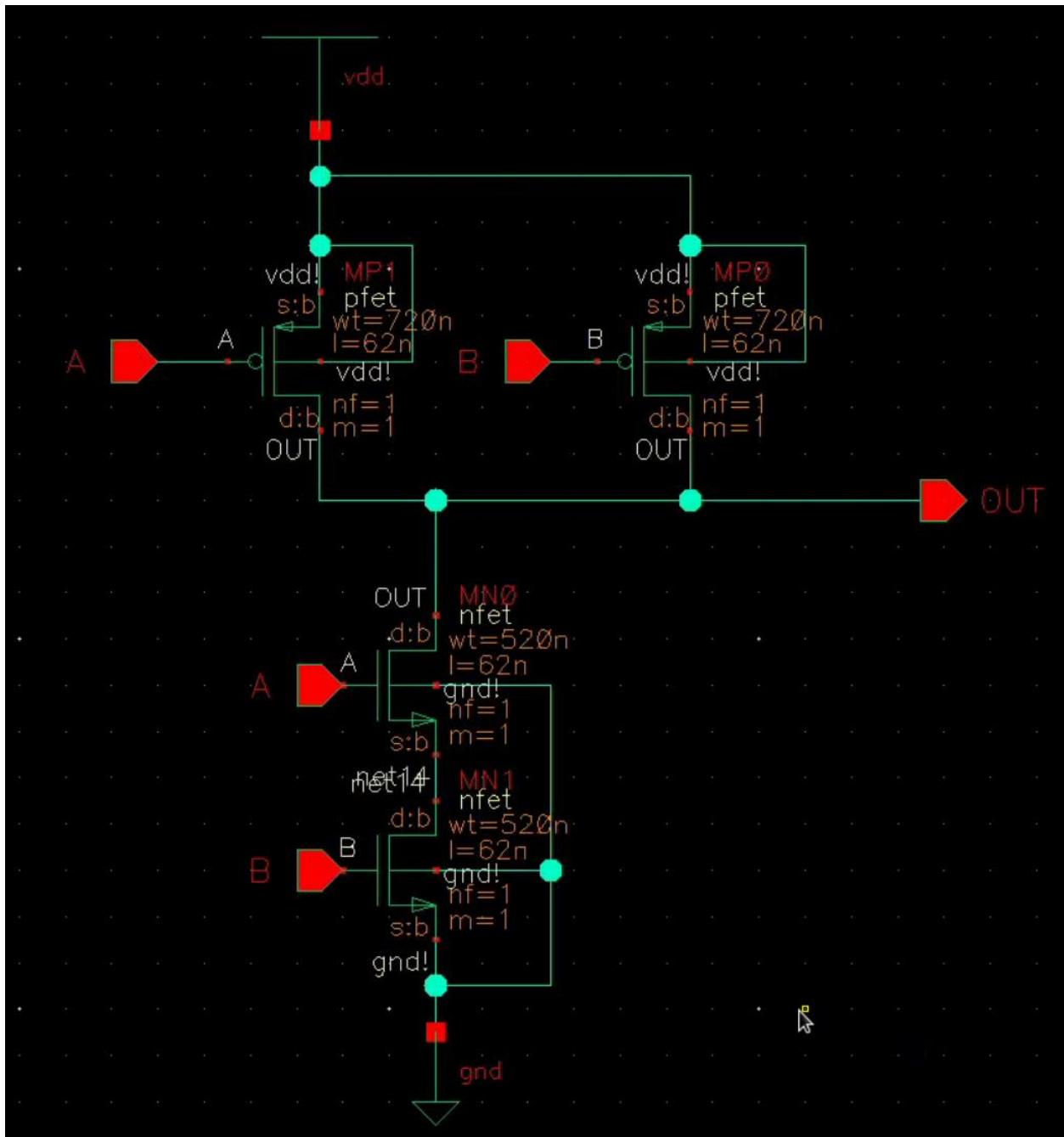


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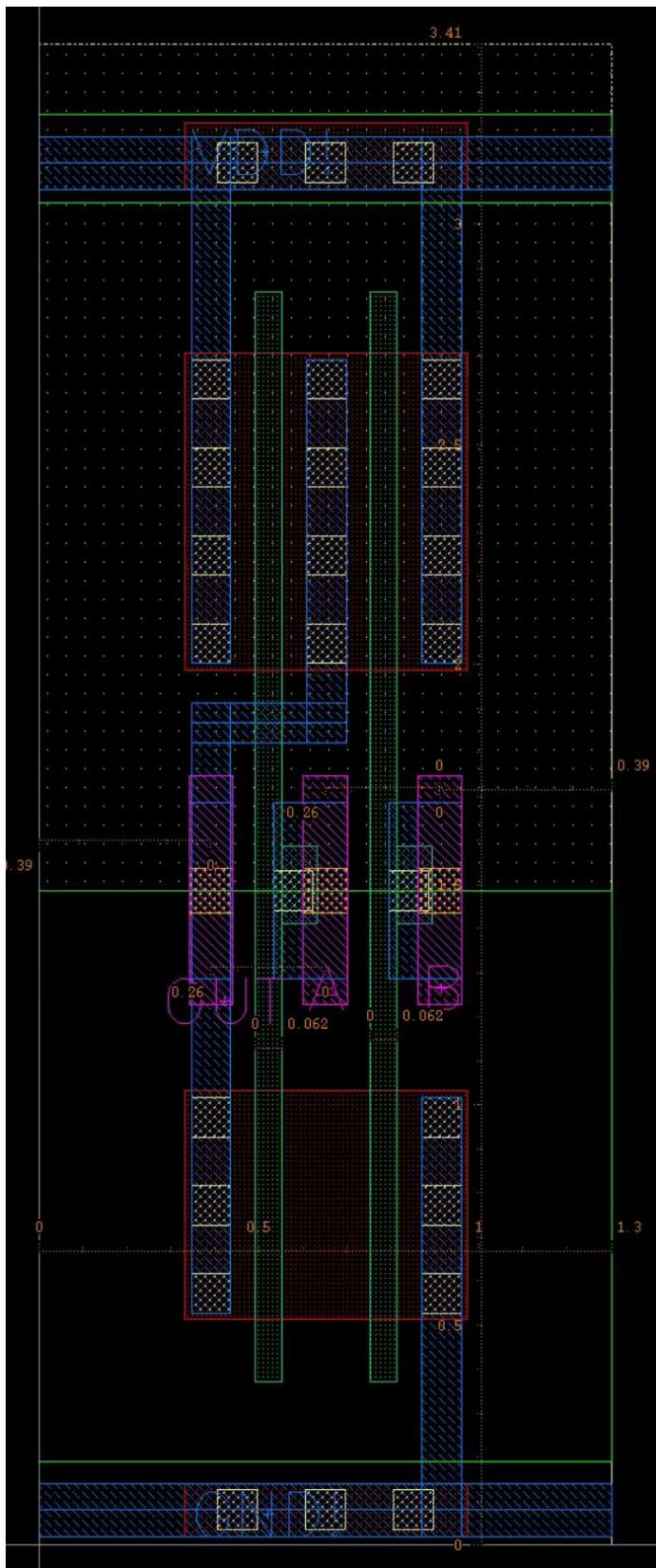


## NAND2

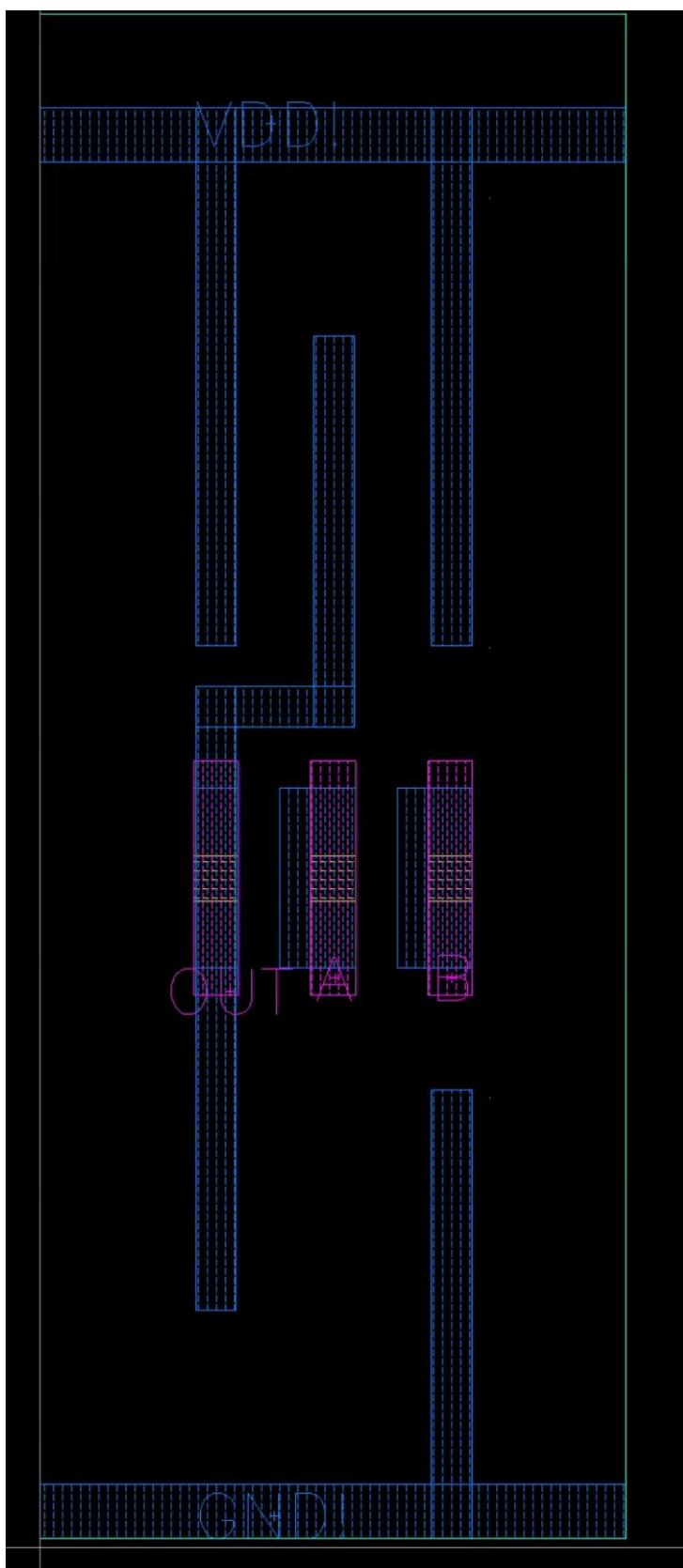
Schematic:



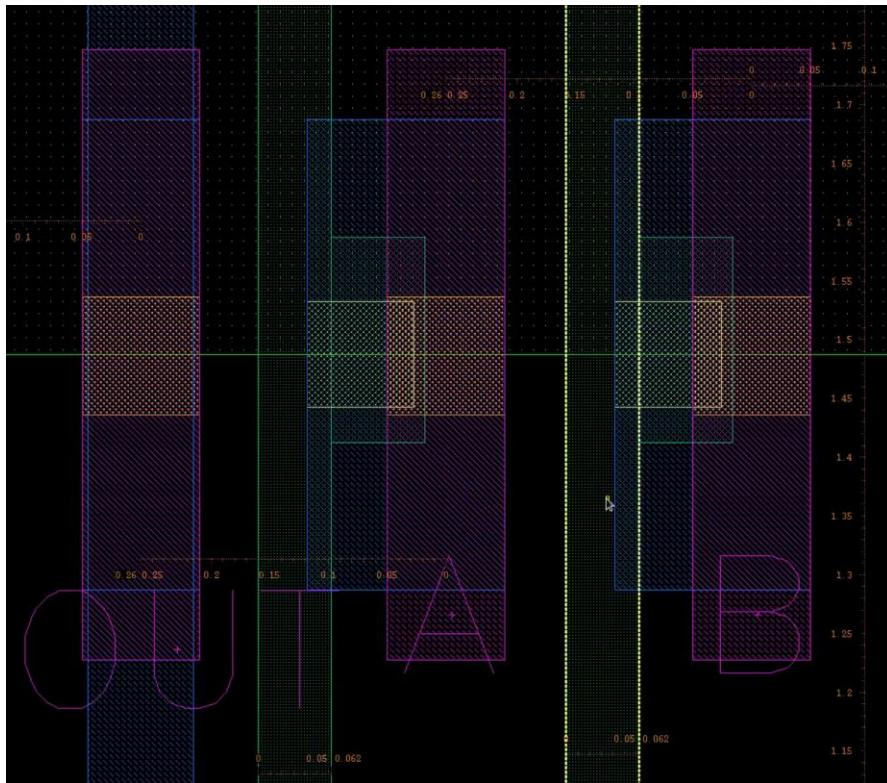
Layout:



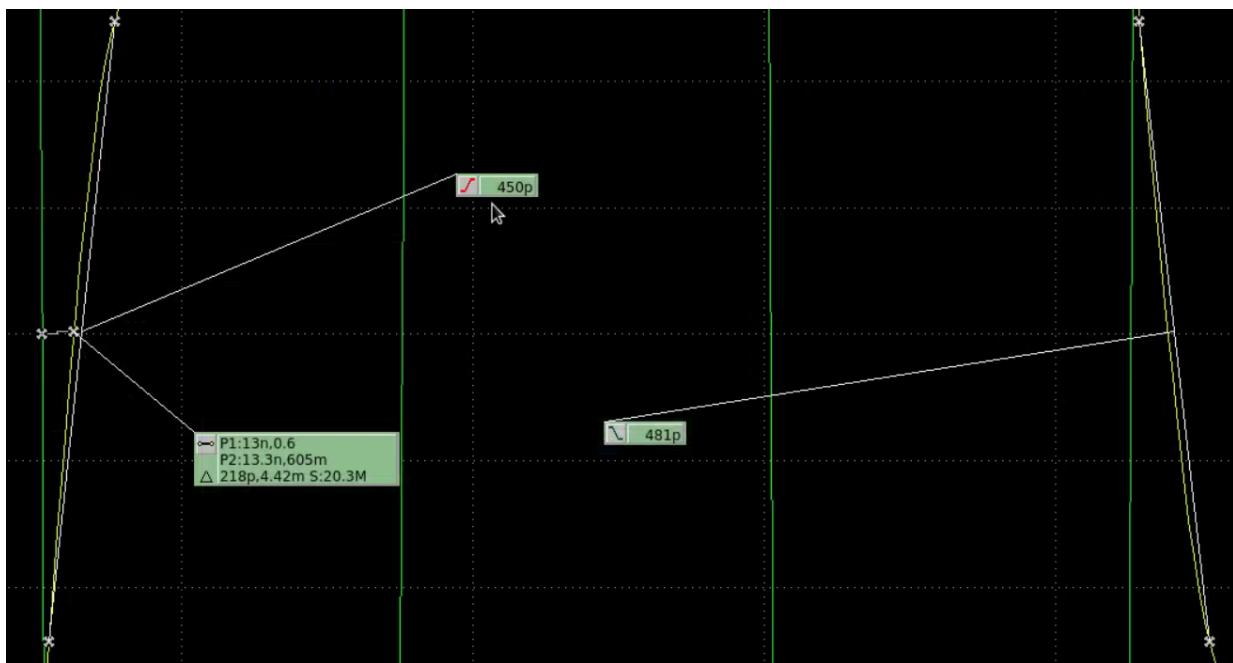
Abstract View:



Gate spacing:

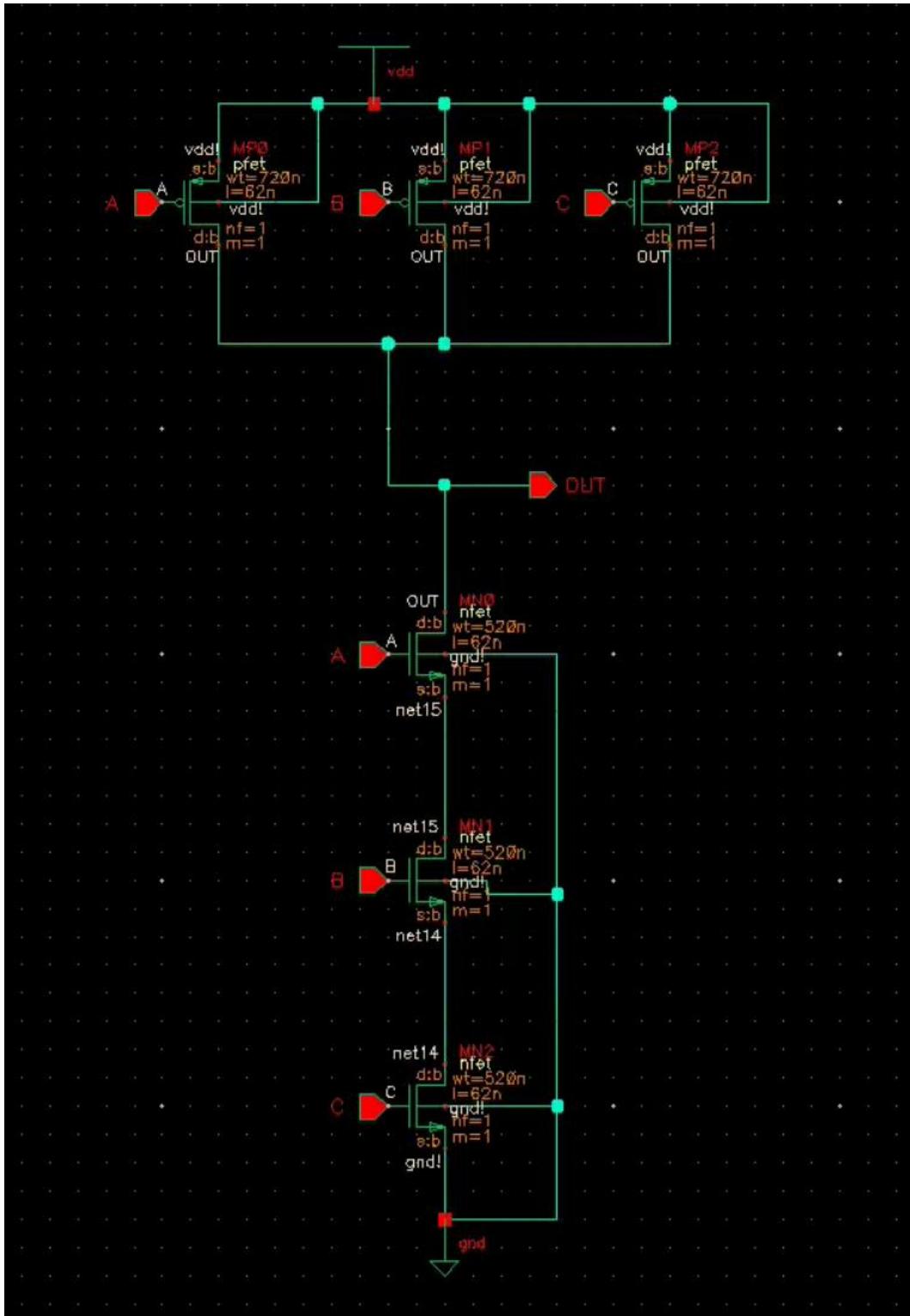


Hspice Simulation:

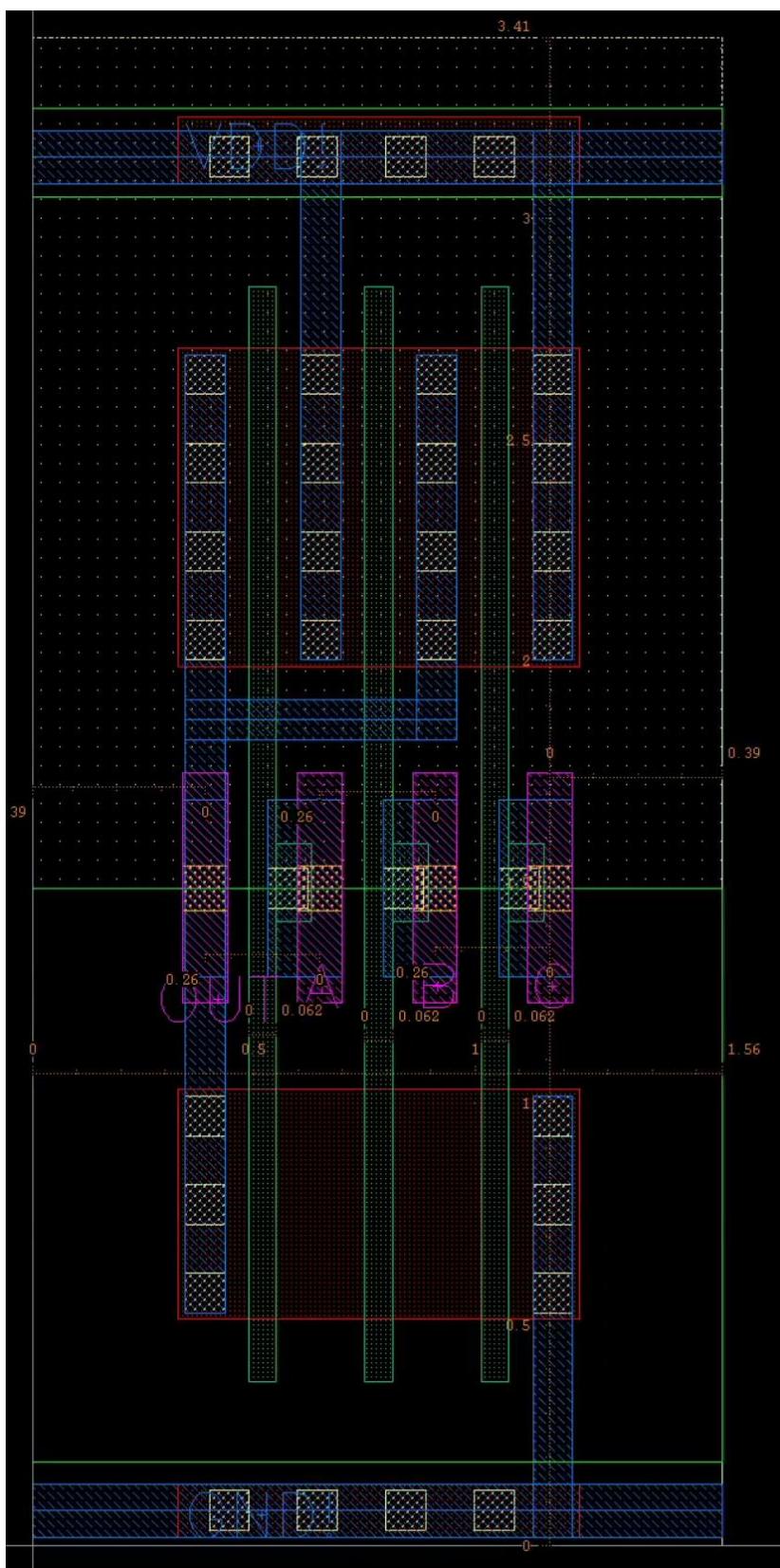


## NAND3

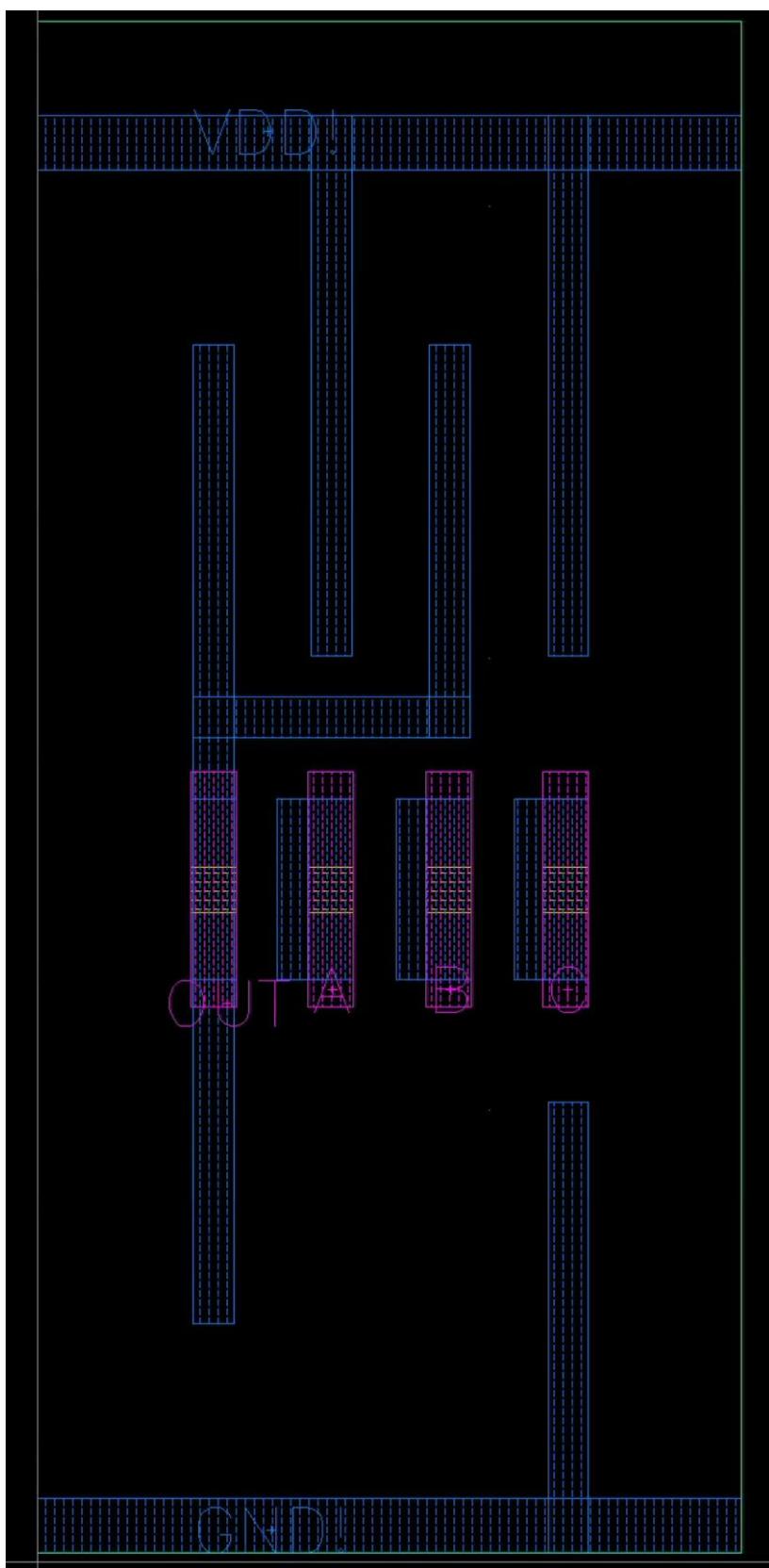
Schematic:



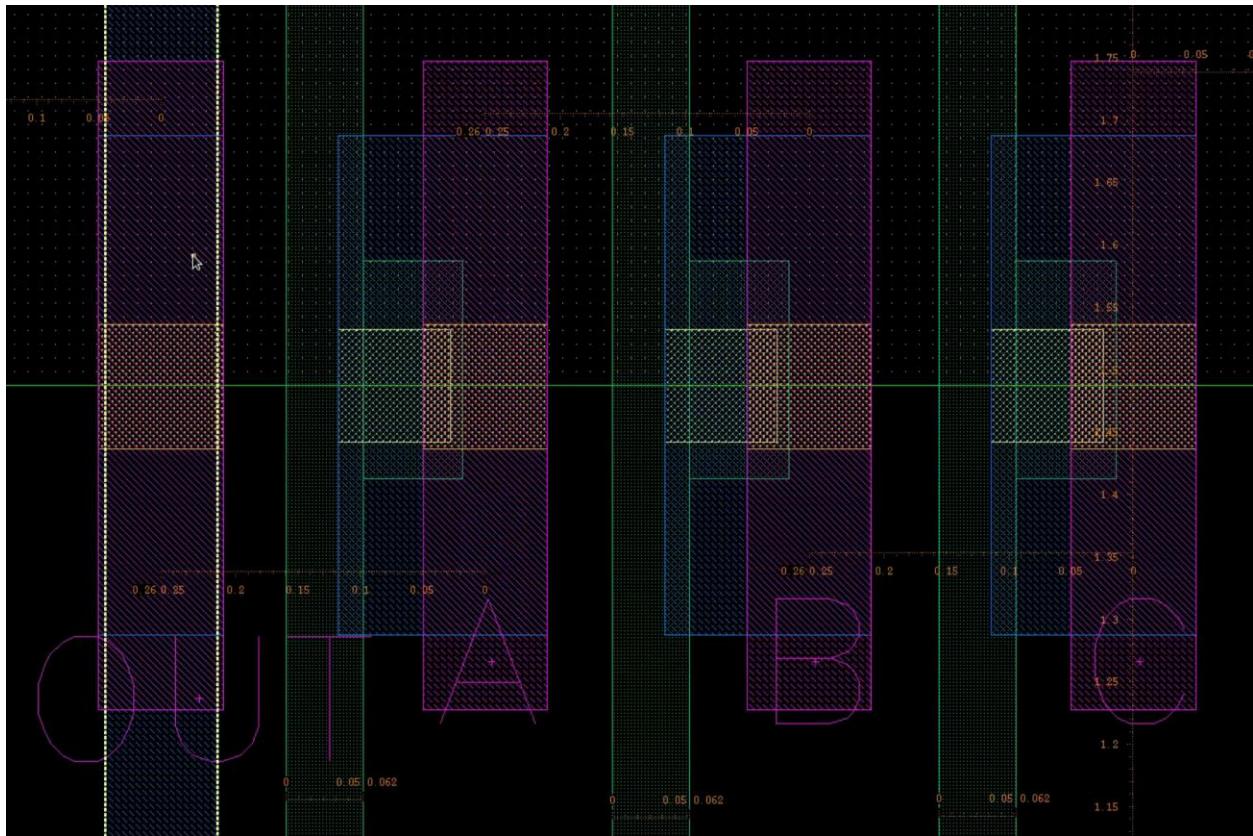
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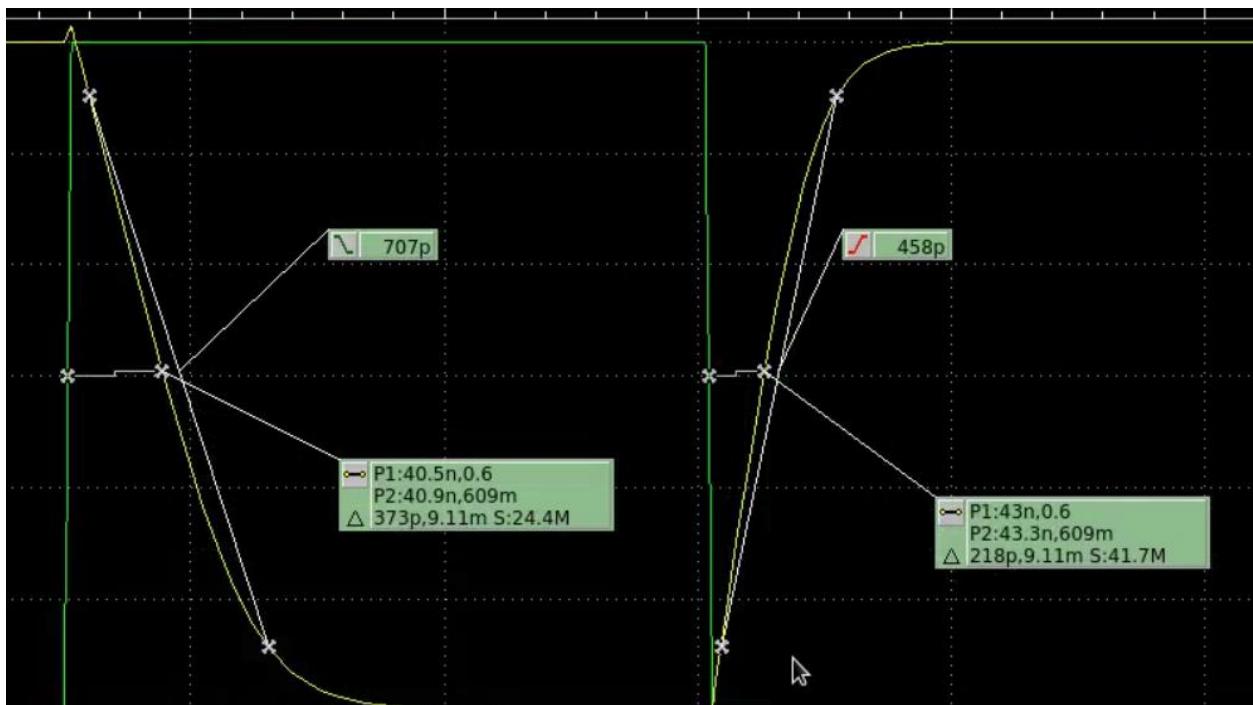
Abstract View:



Gate spacing:

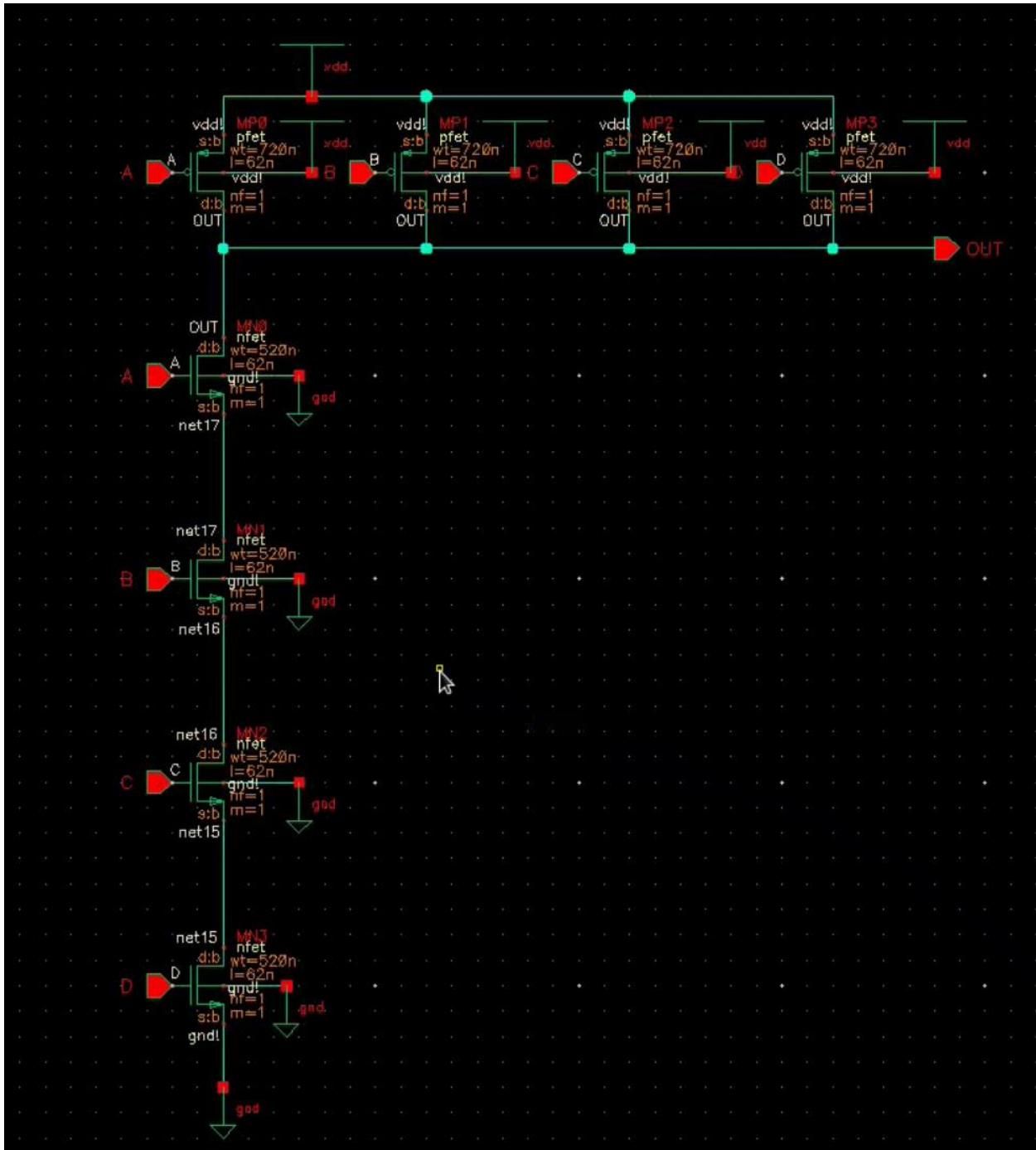


Hspice Simulation:

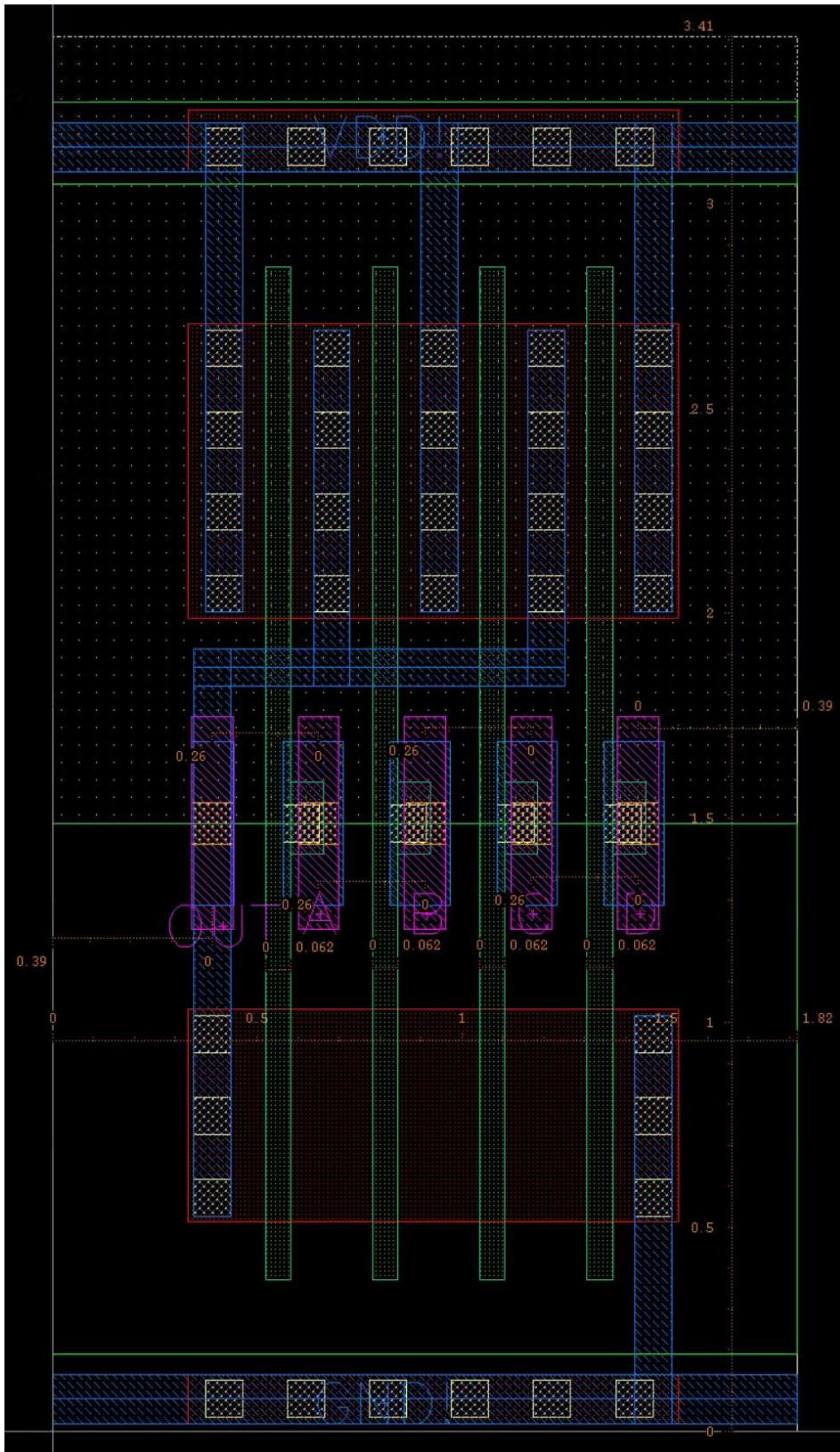


## NAND4

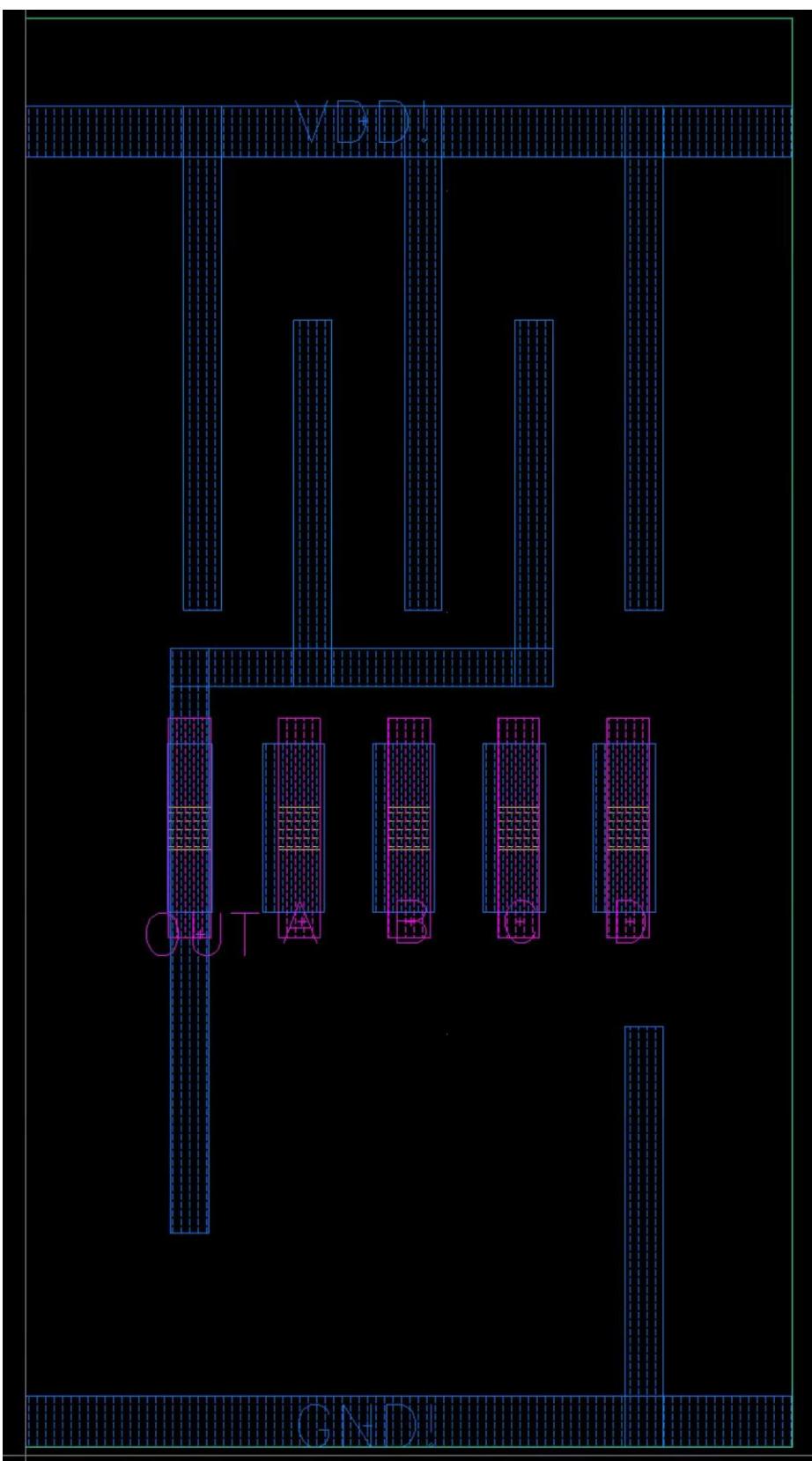
Schematic:



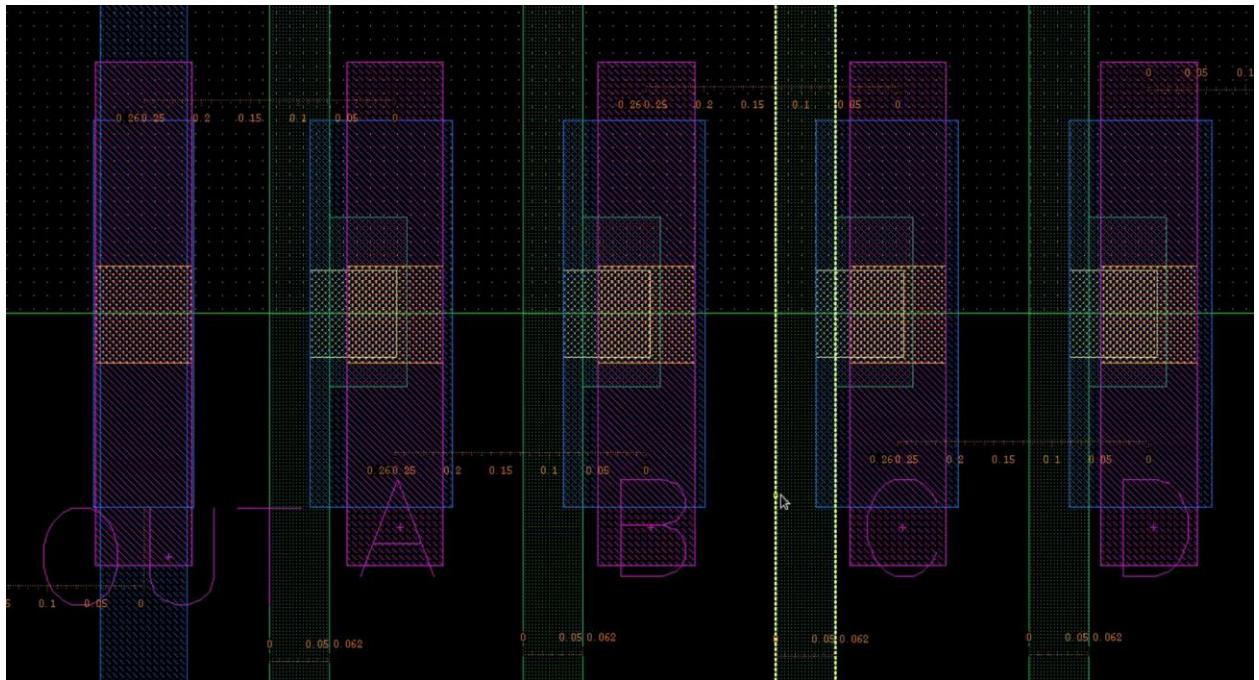
## Layout:



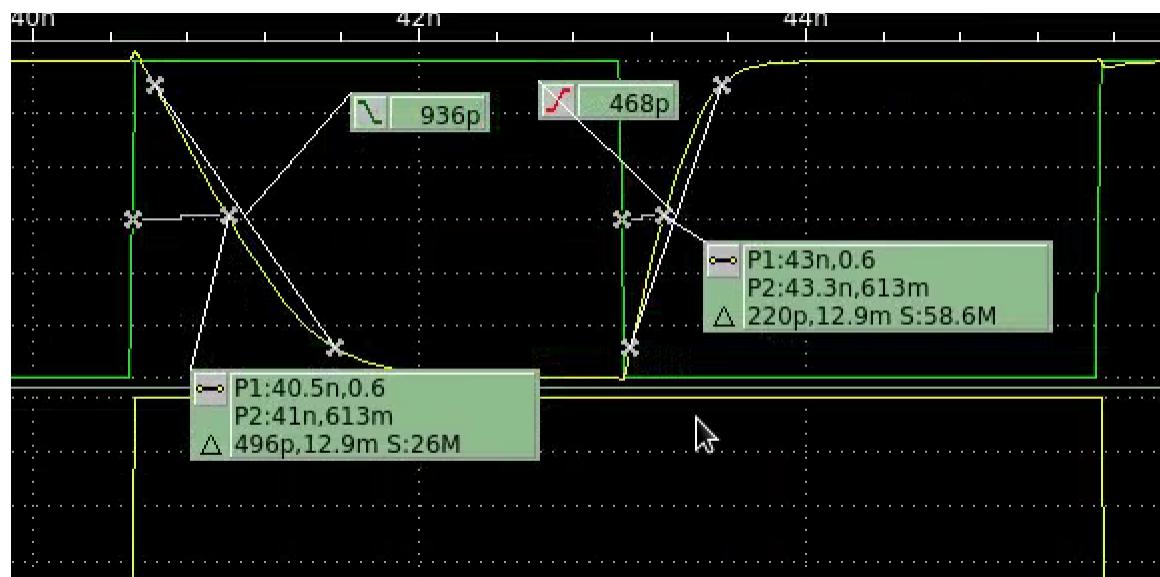
Abstract View:



Gate spacing:

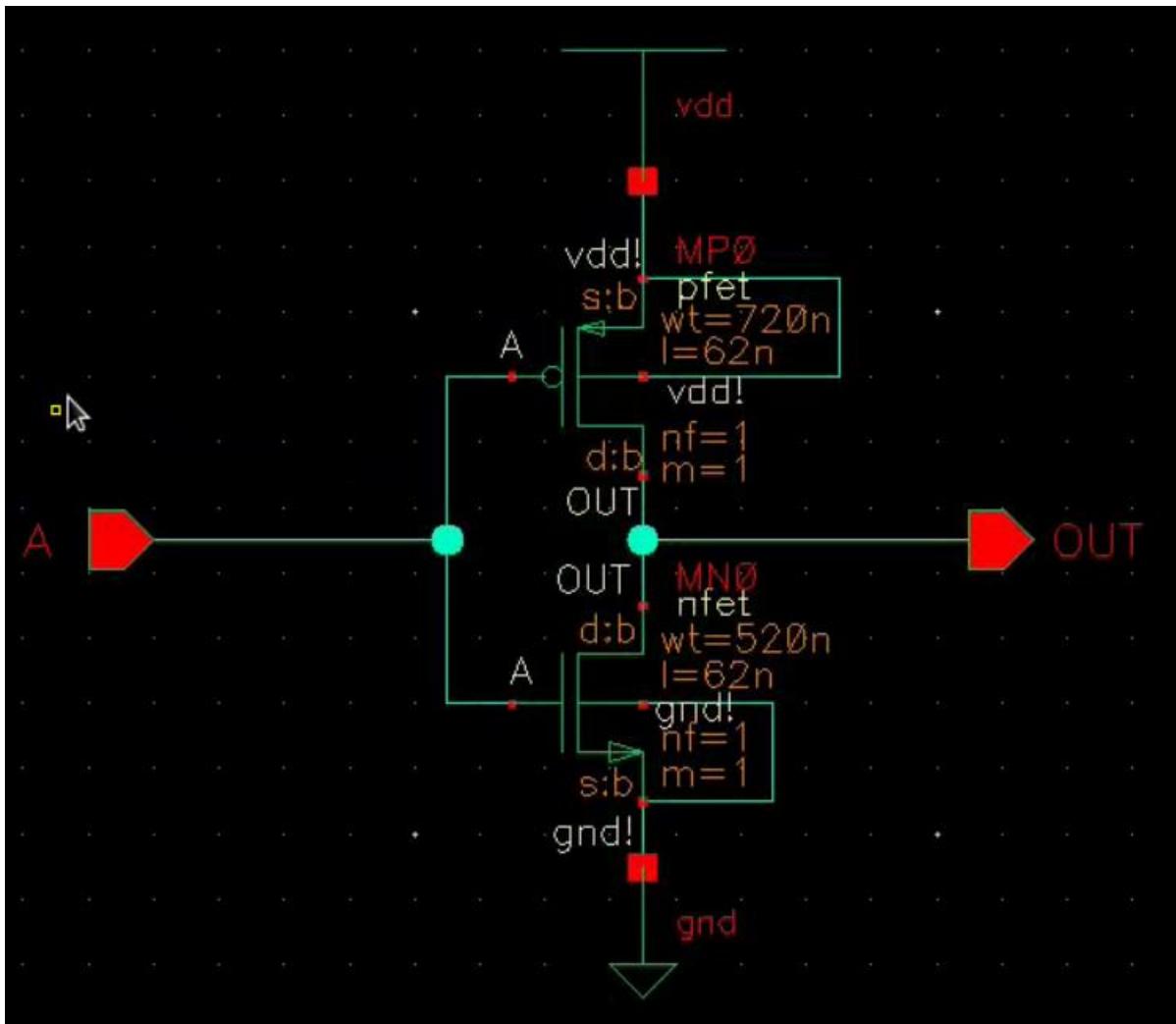


Hspice Simulation:

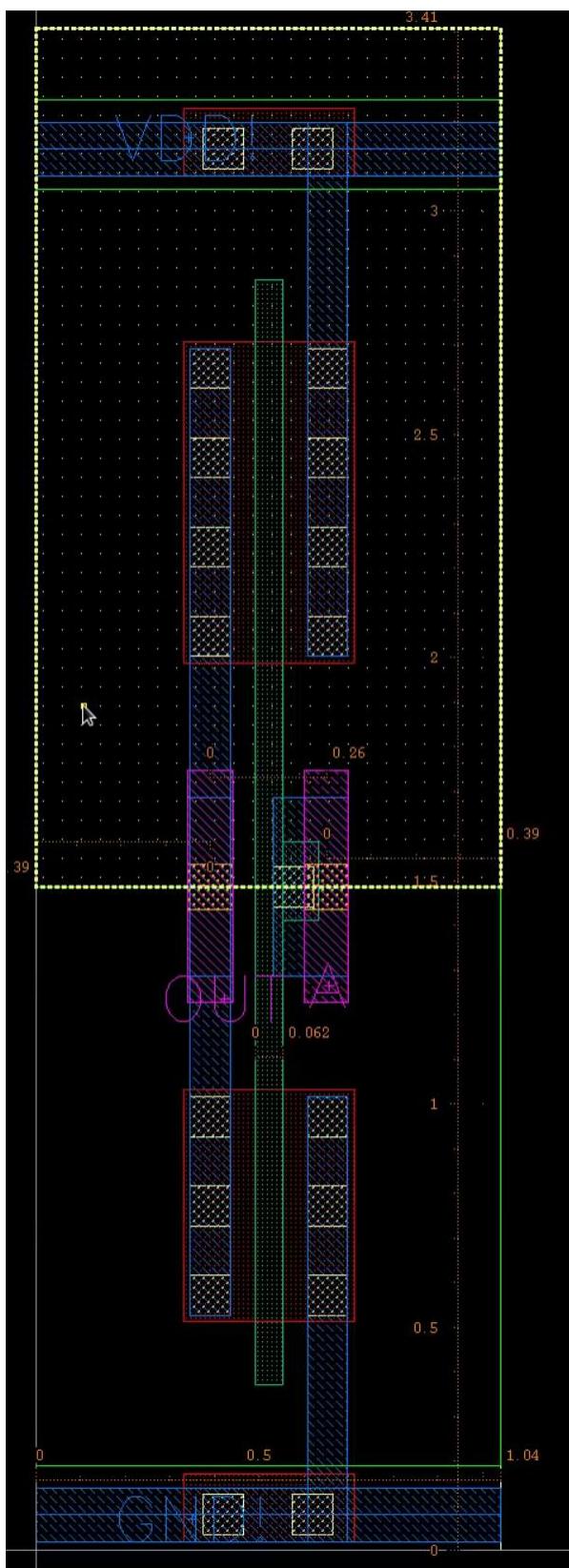


## INVERTER

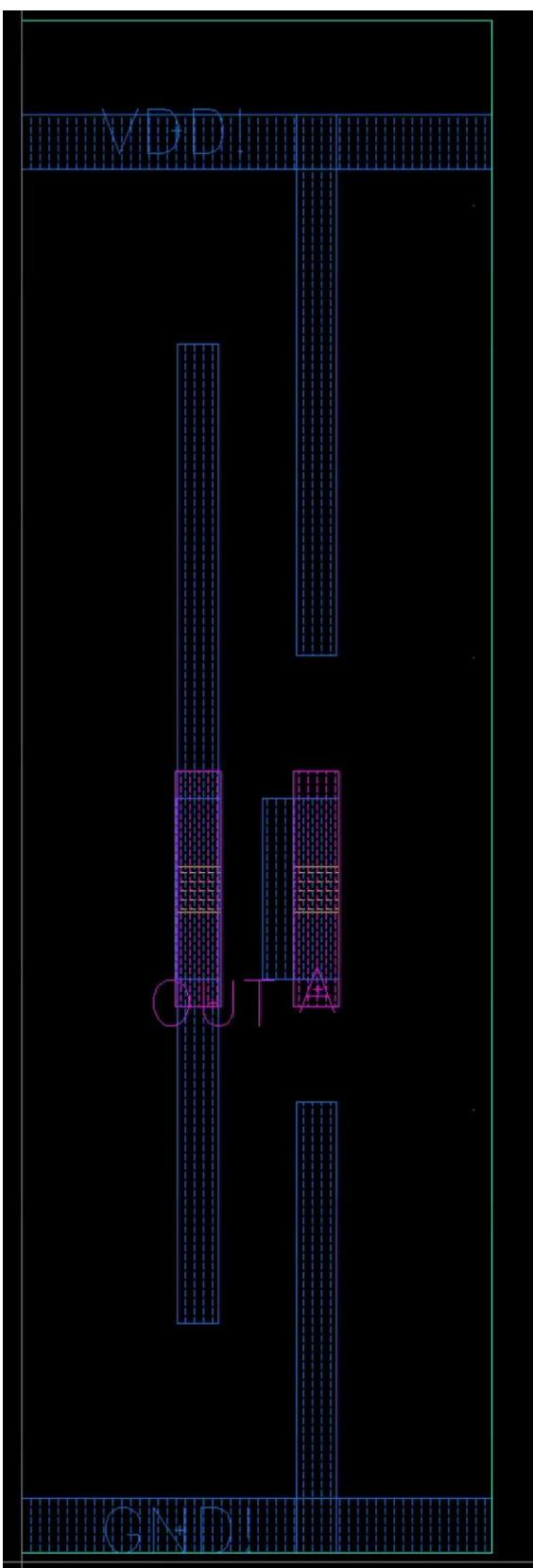
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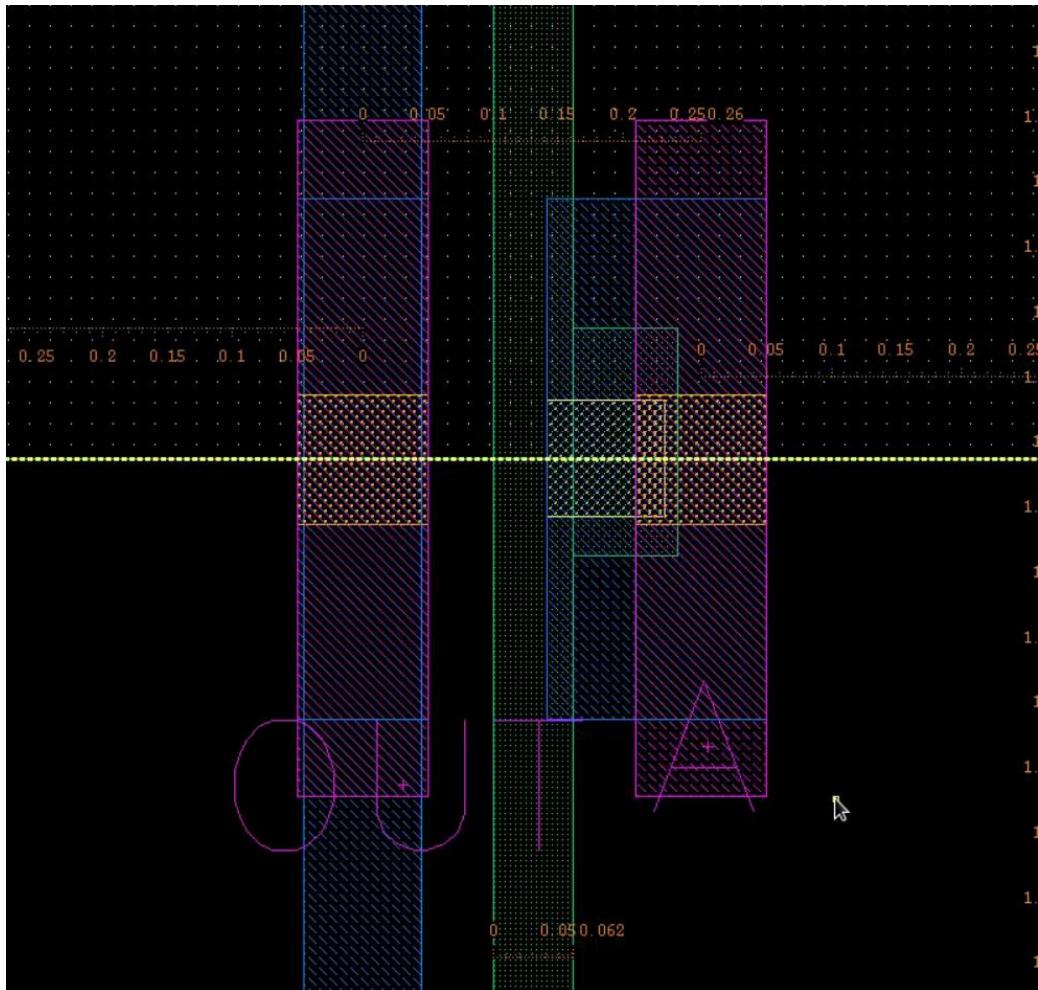
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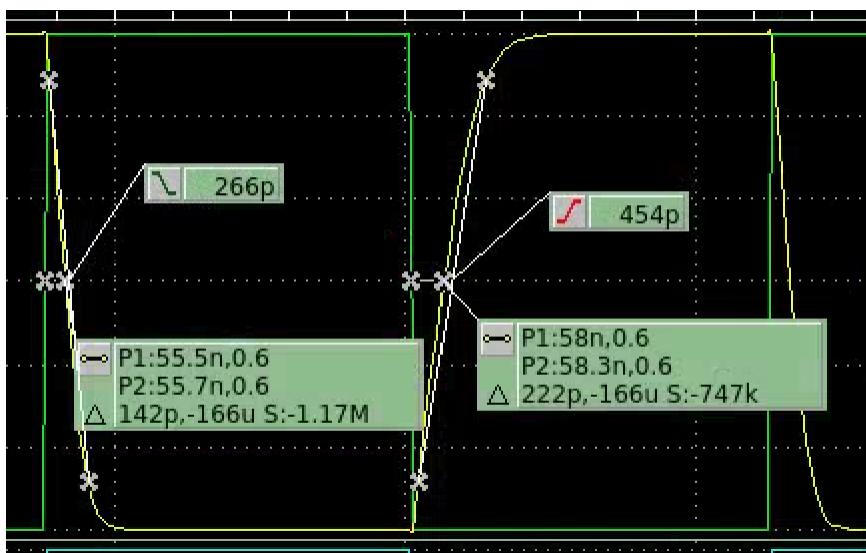
Abstract View:



Gate spacing:

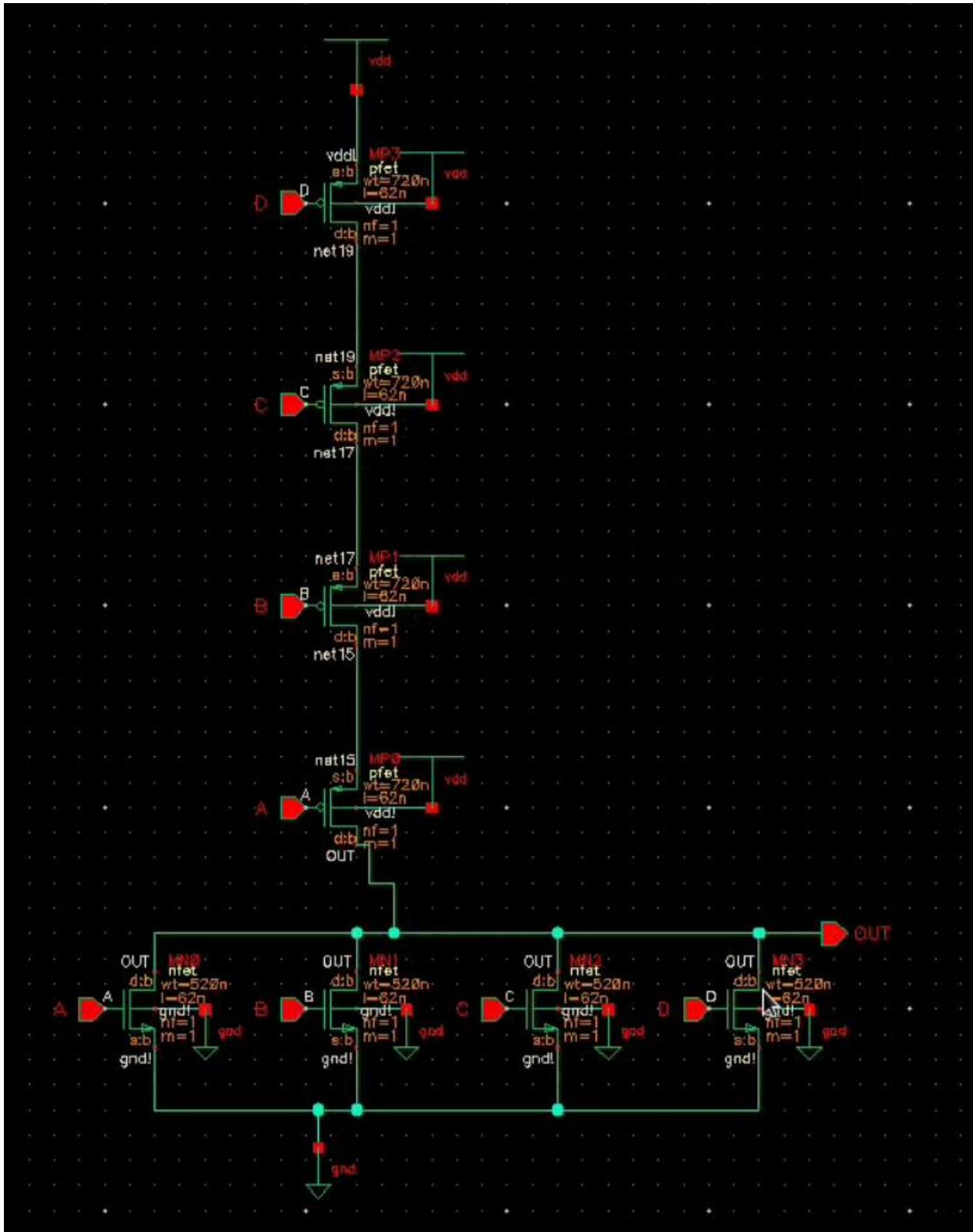


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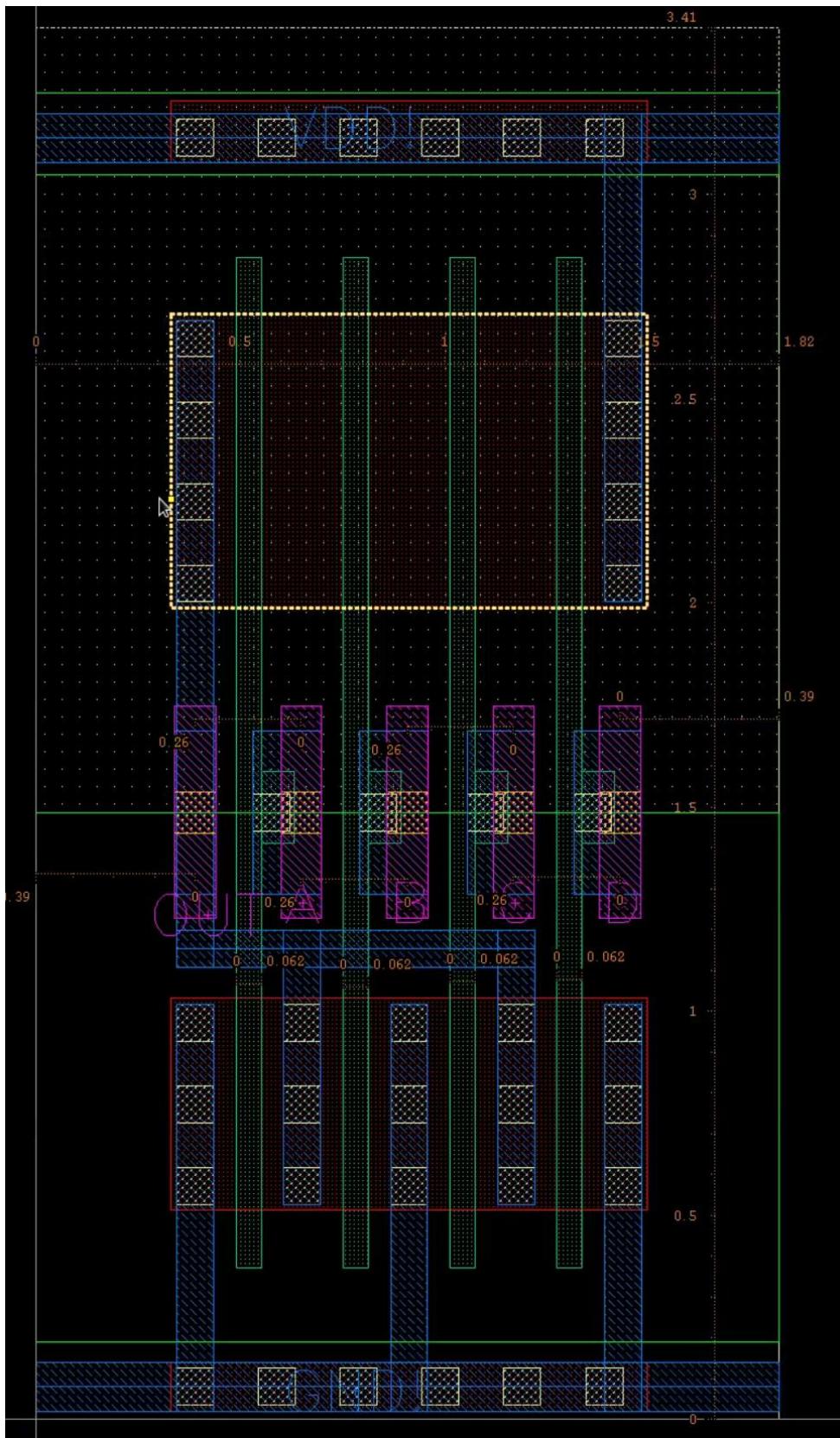


## NOR4

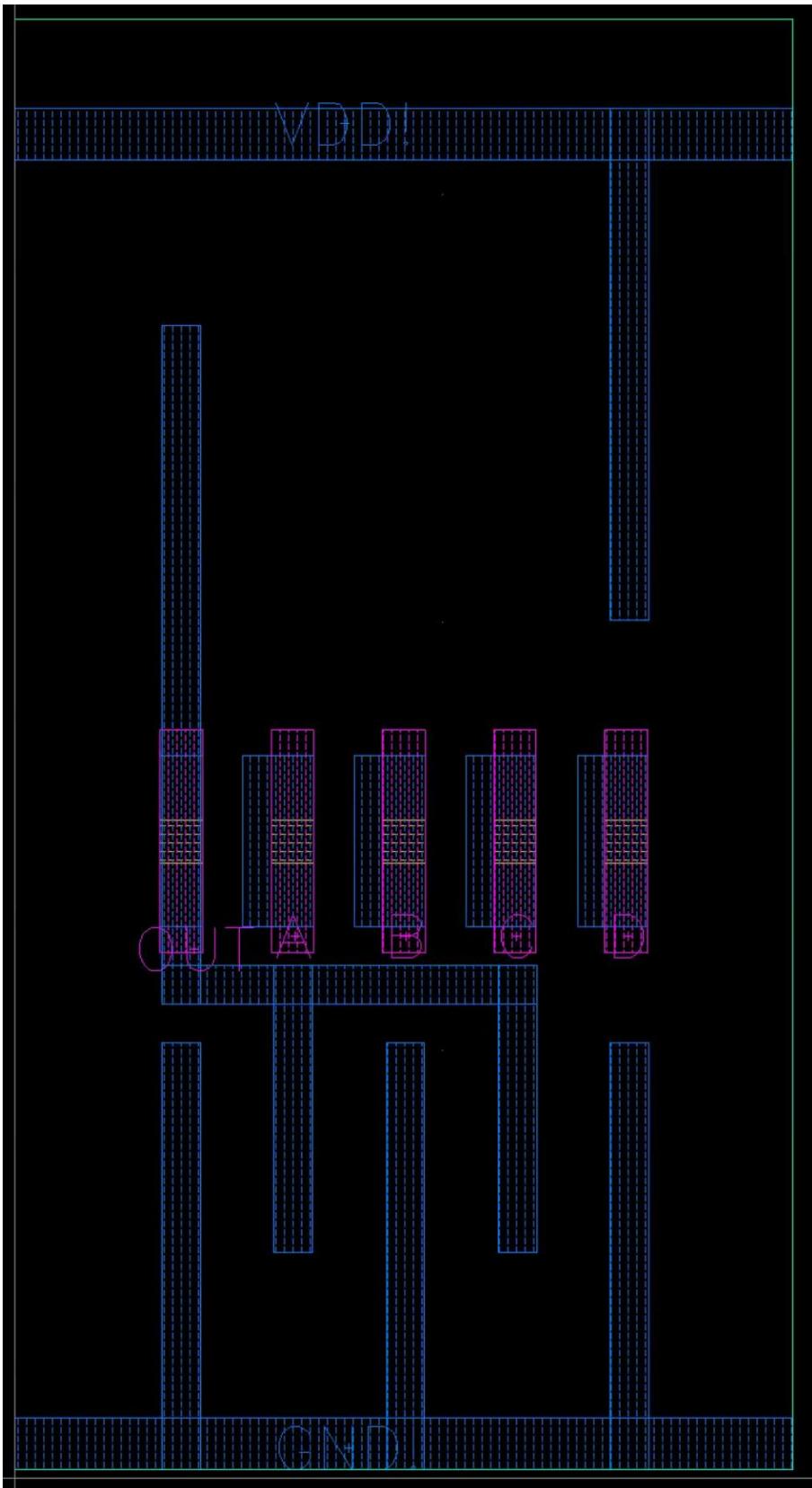
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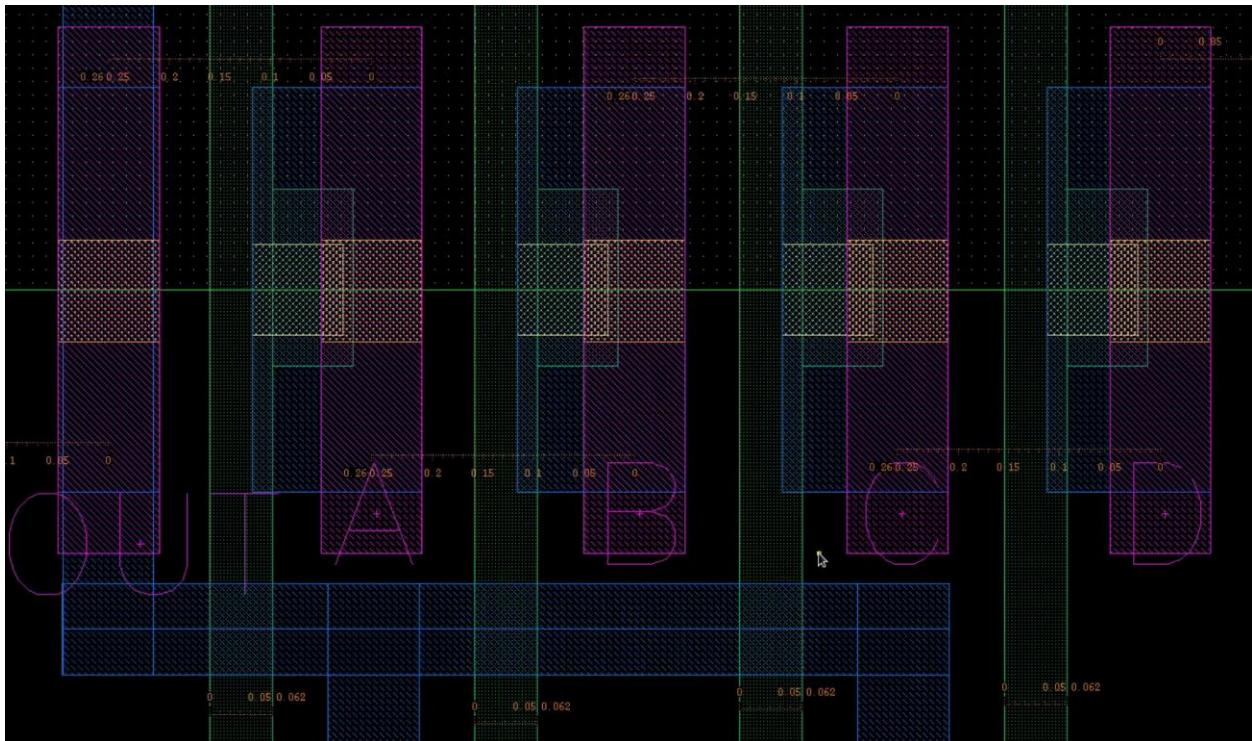
Layout:



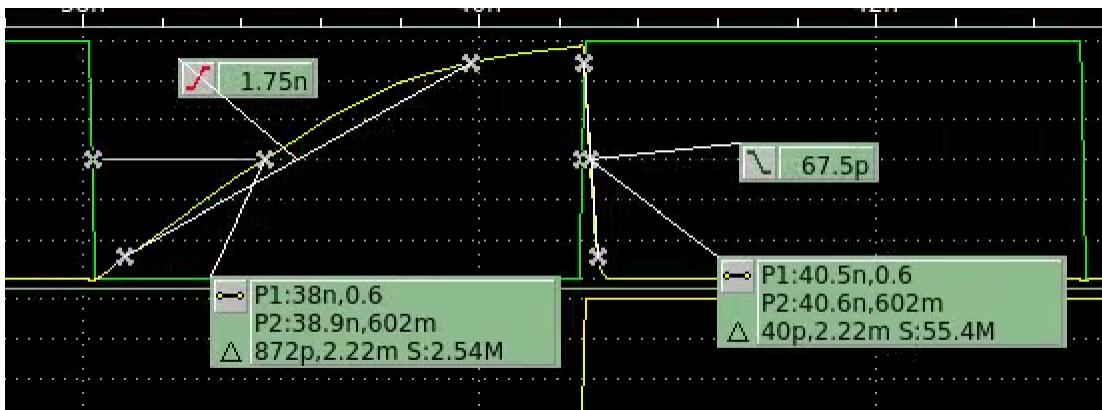
Abstract View:



Gate spacing:

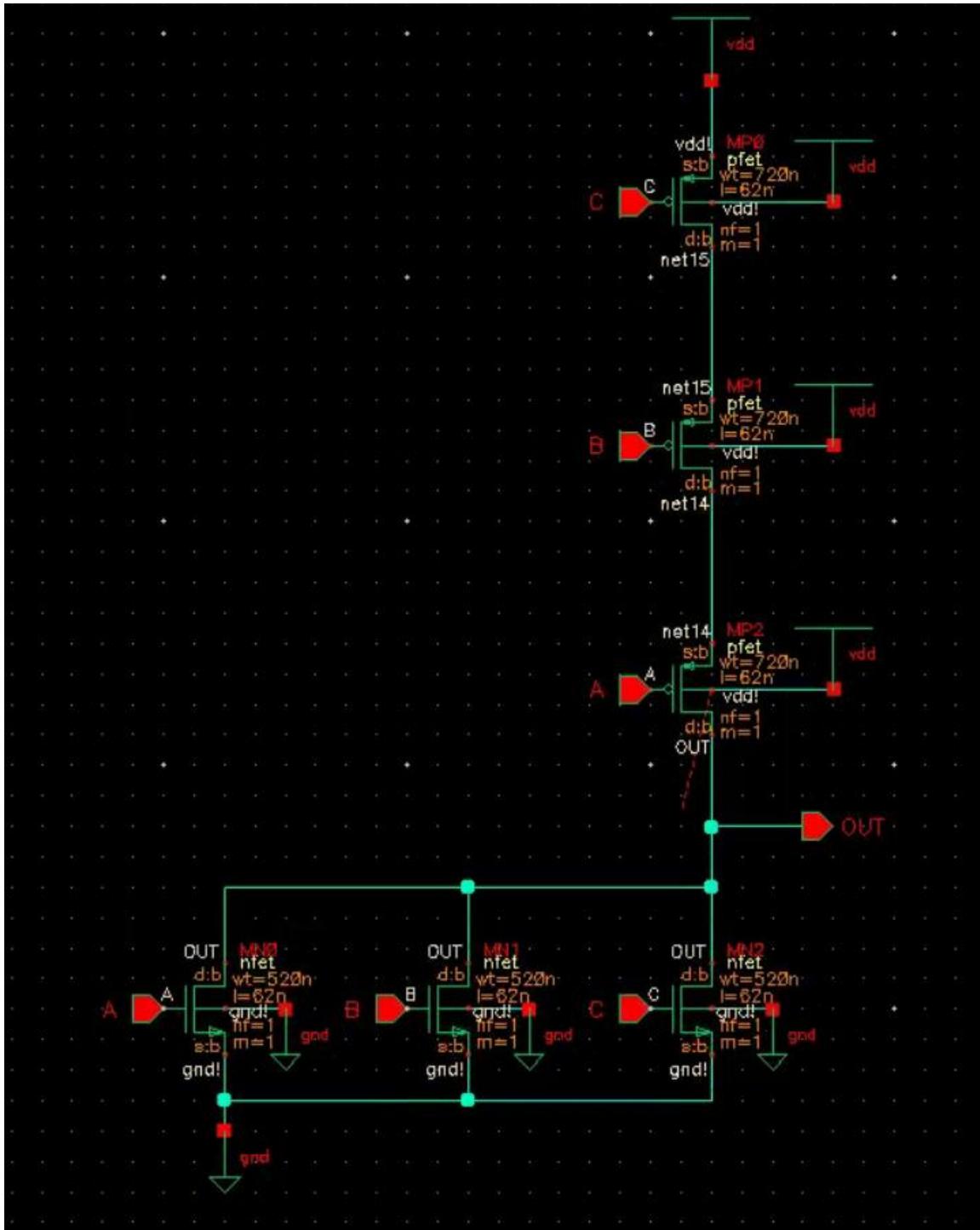


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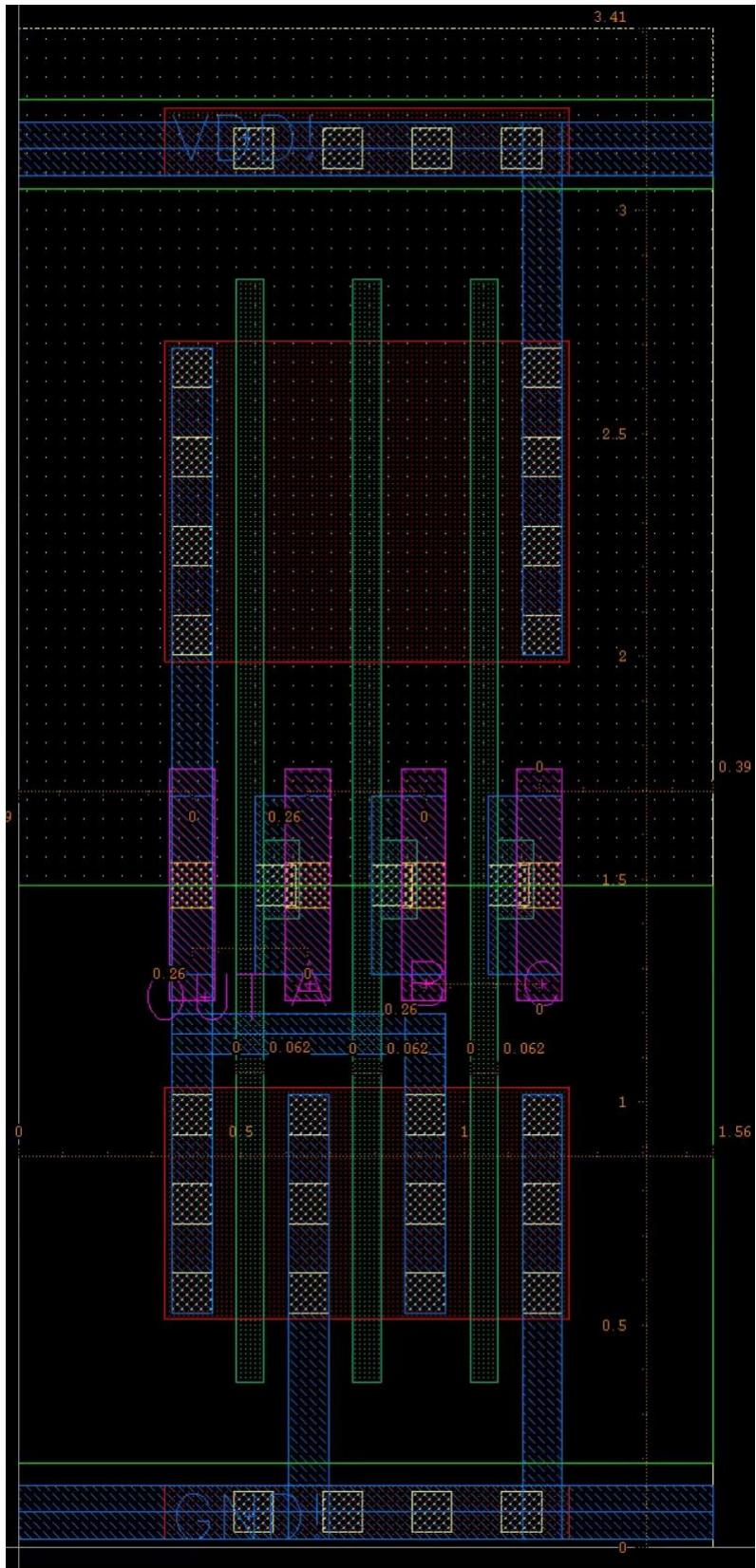


## NOR3

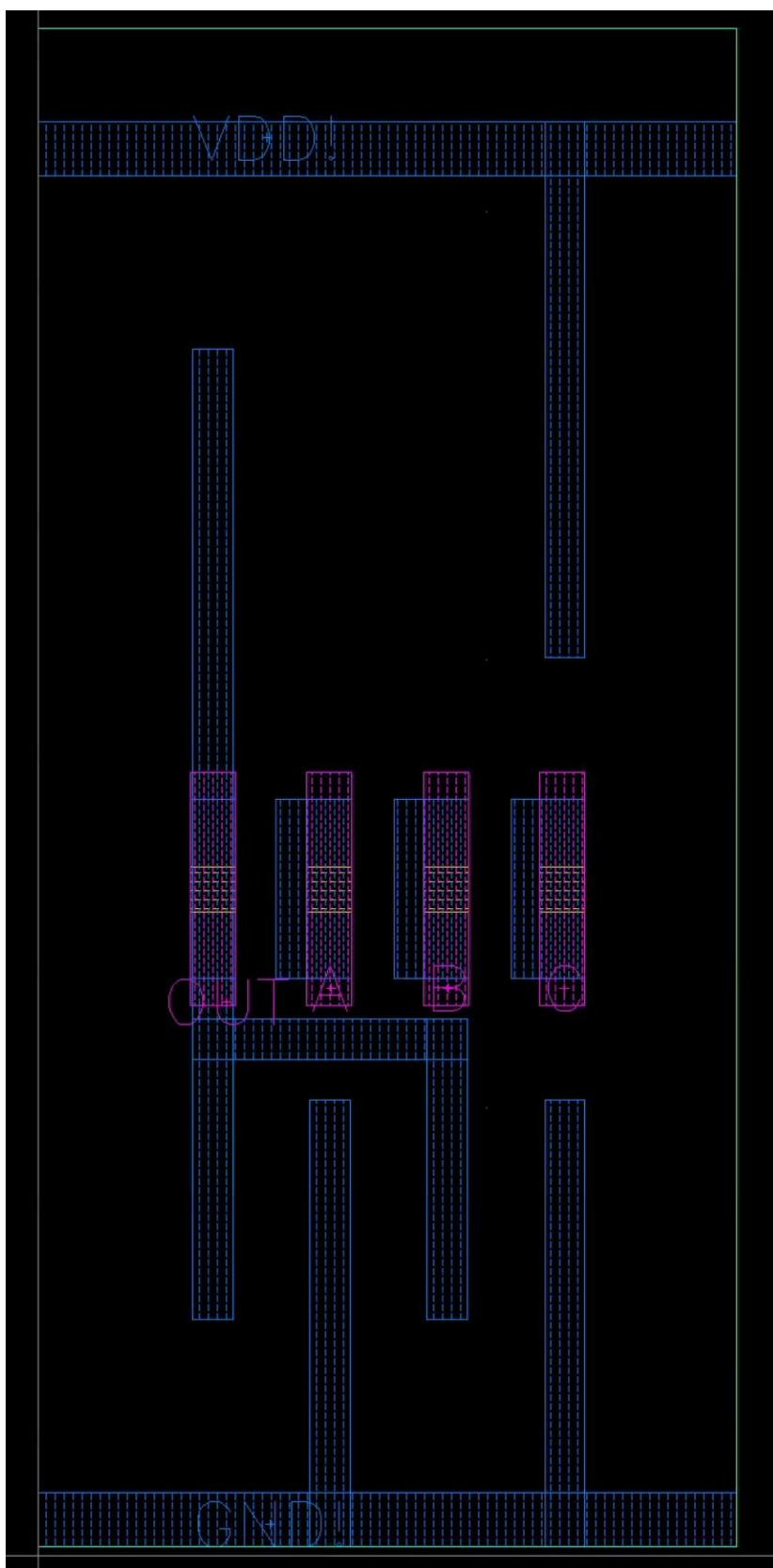
Schematic:



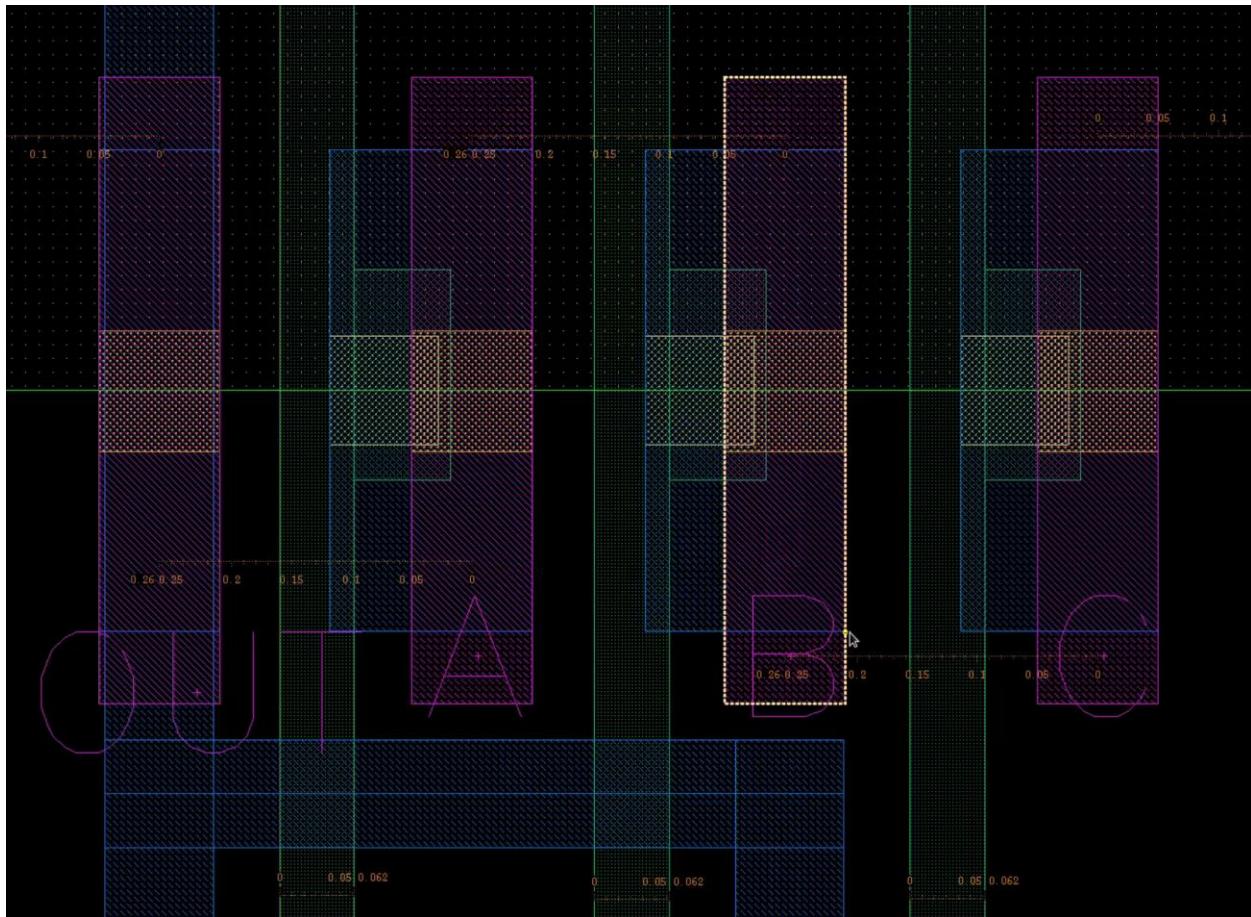
Layout:



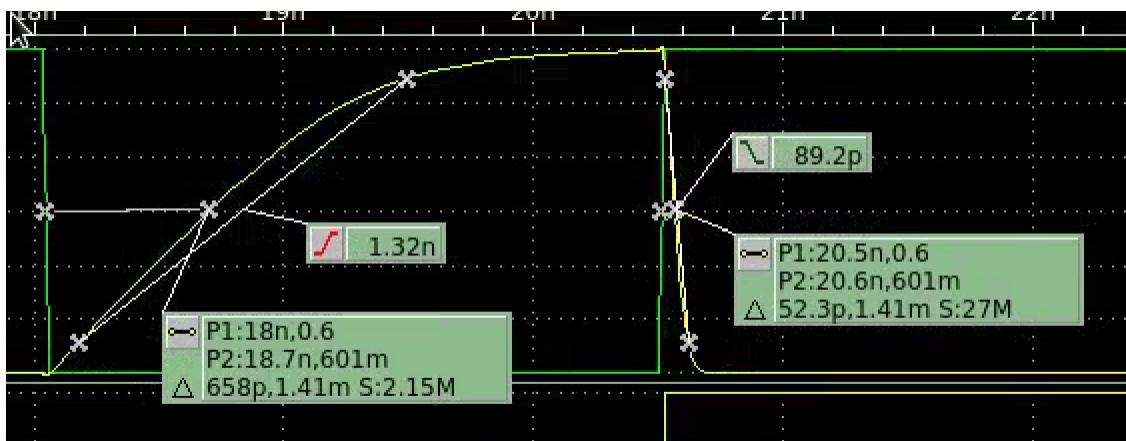
Abstract View:



Gate spacing:

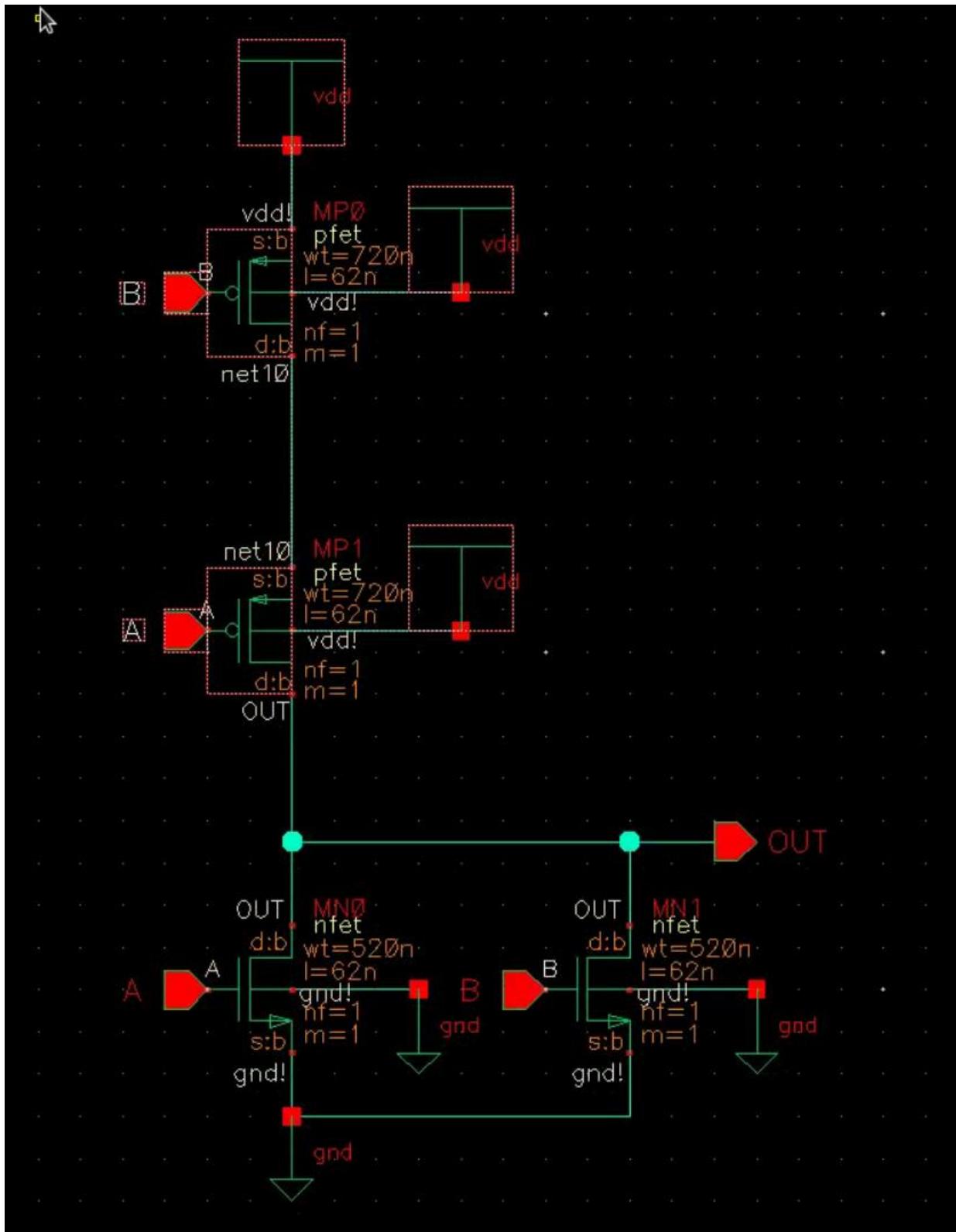


Hspice Simulation:

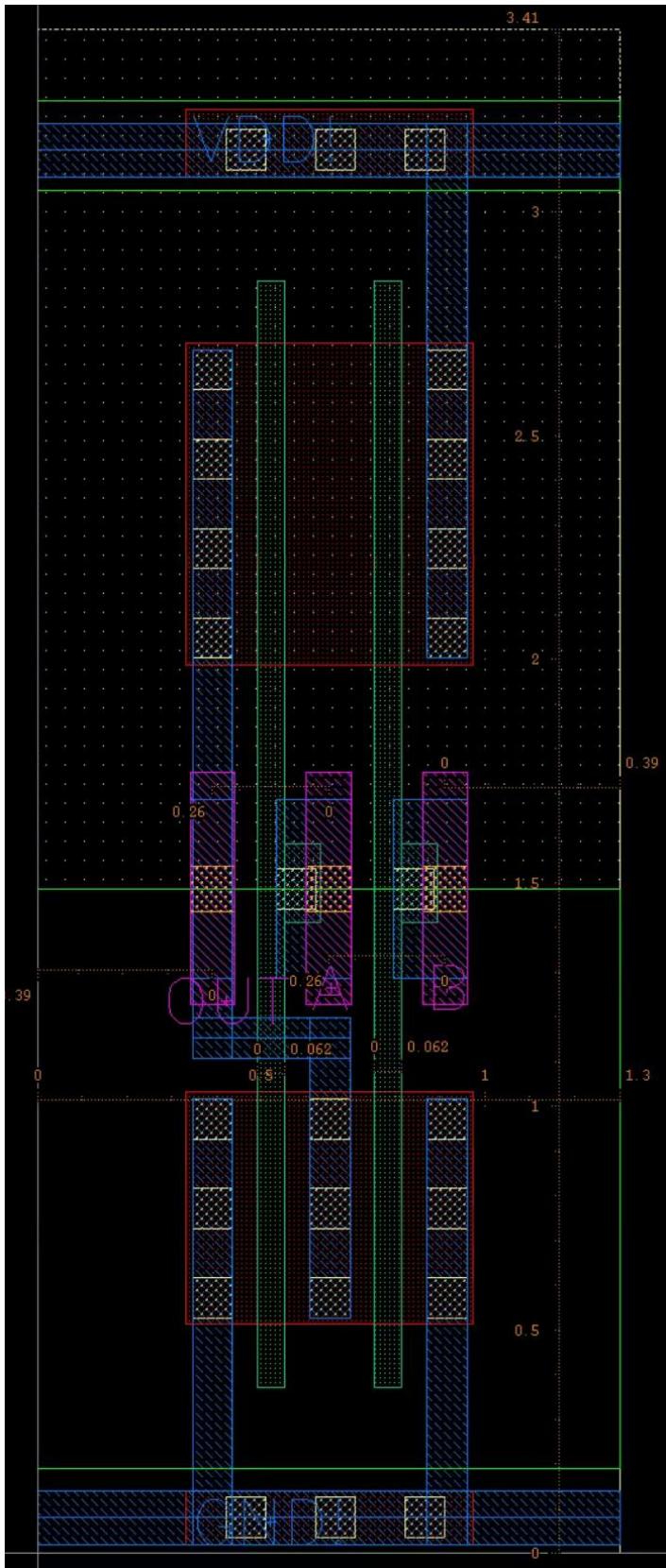


## NOR2

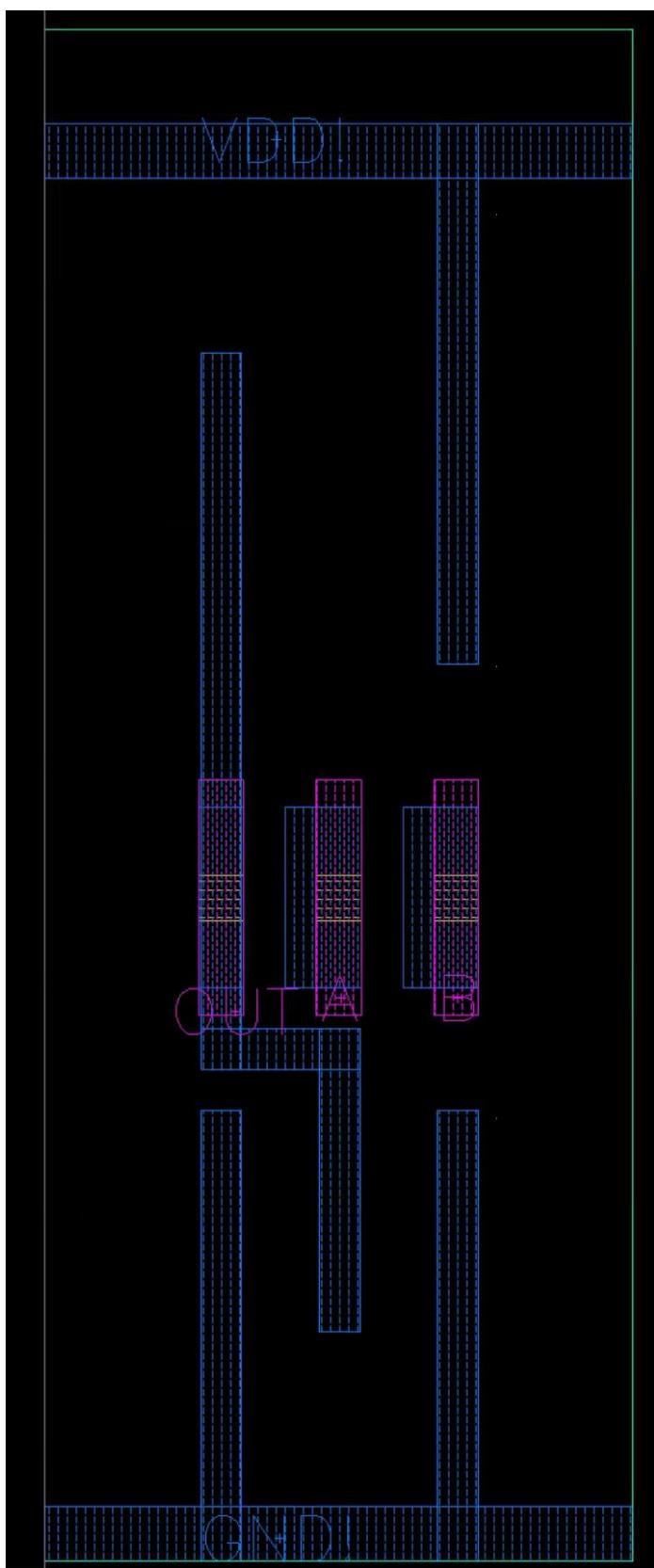
Schematic:



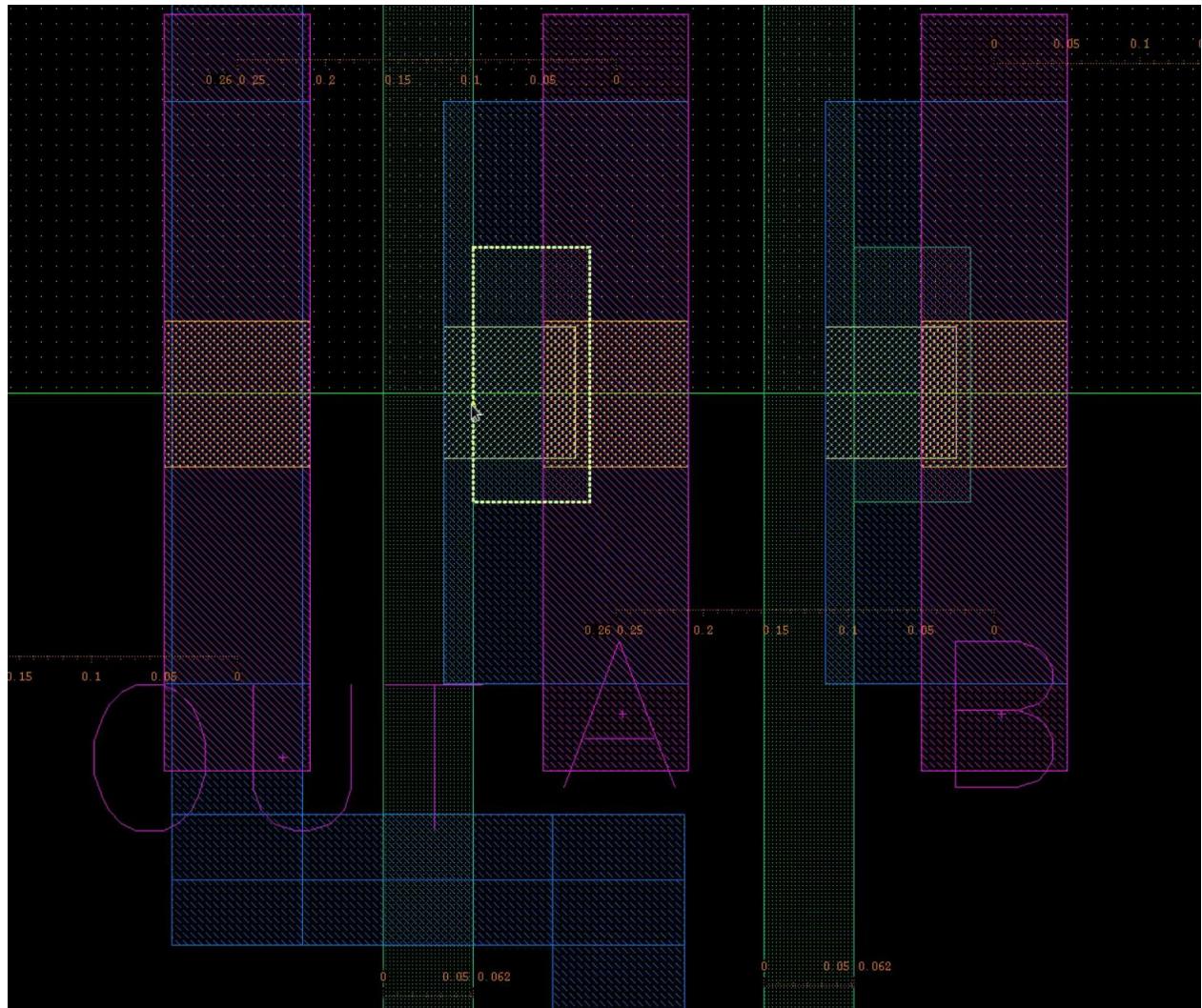
## Layout:



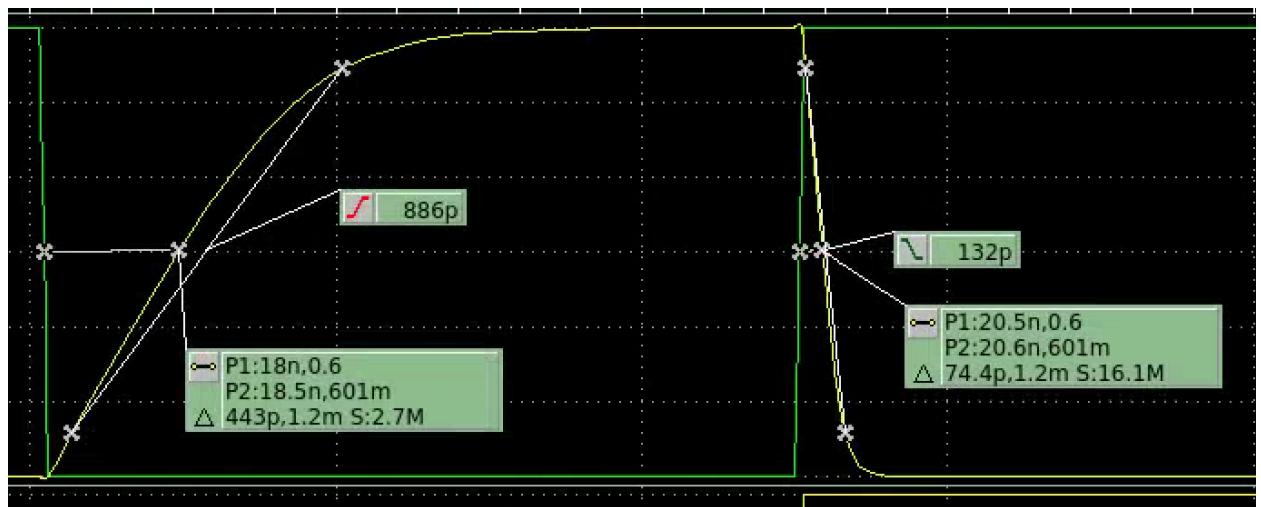
Abstract View:



Gate spacing:

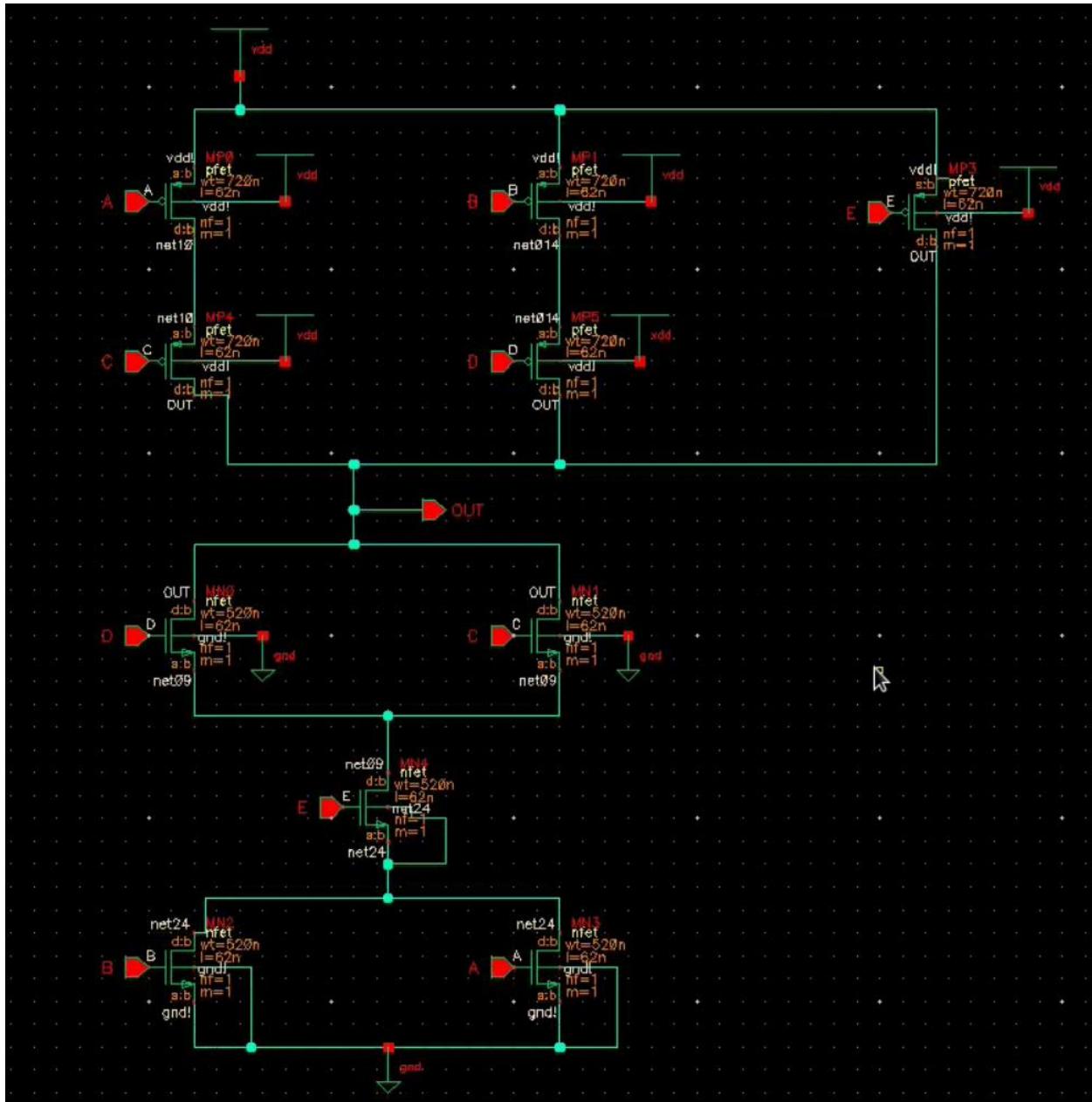


Hspice Simulation:

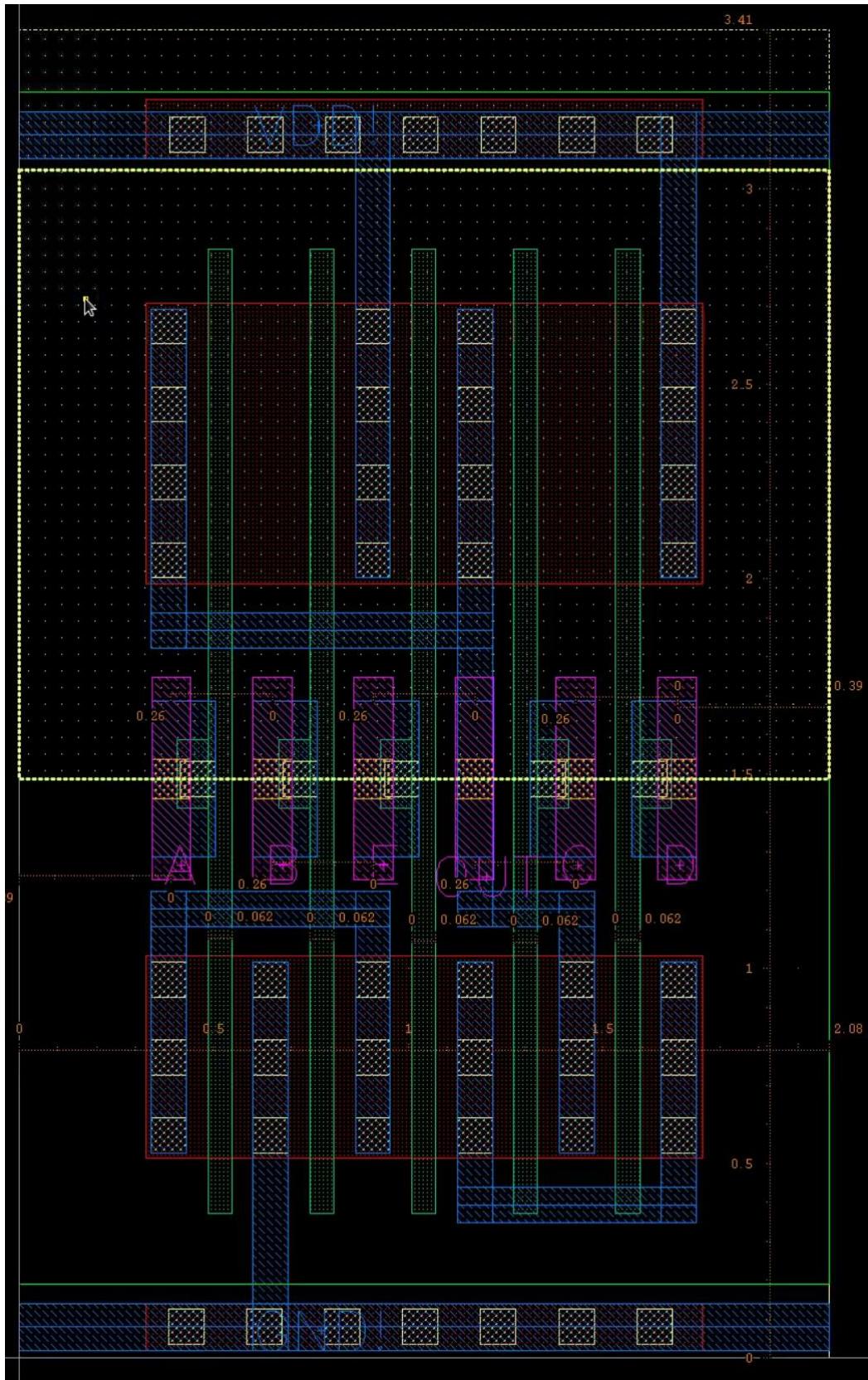


# OAI221

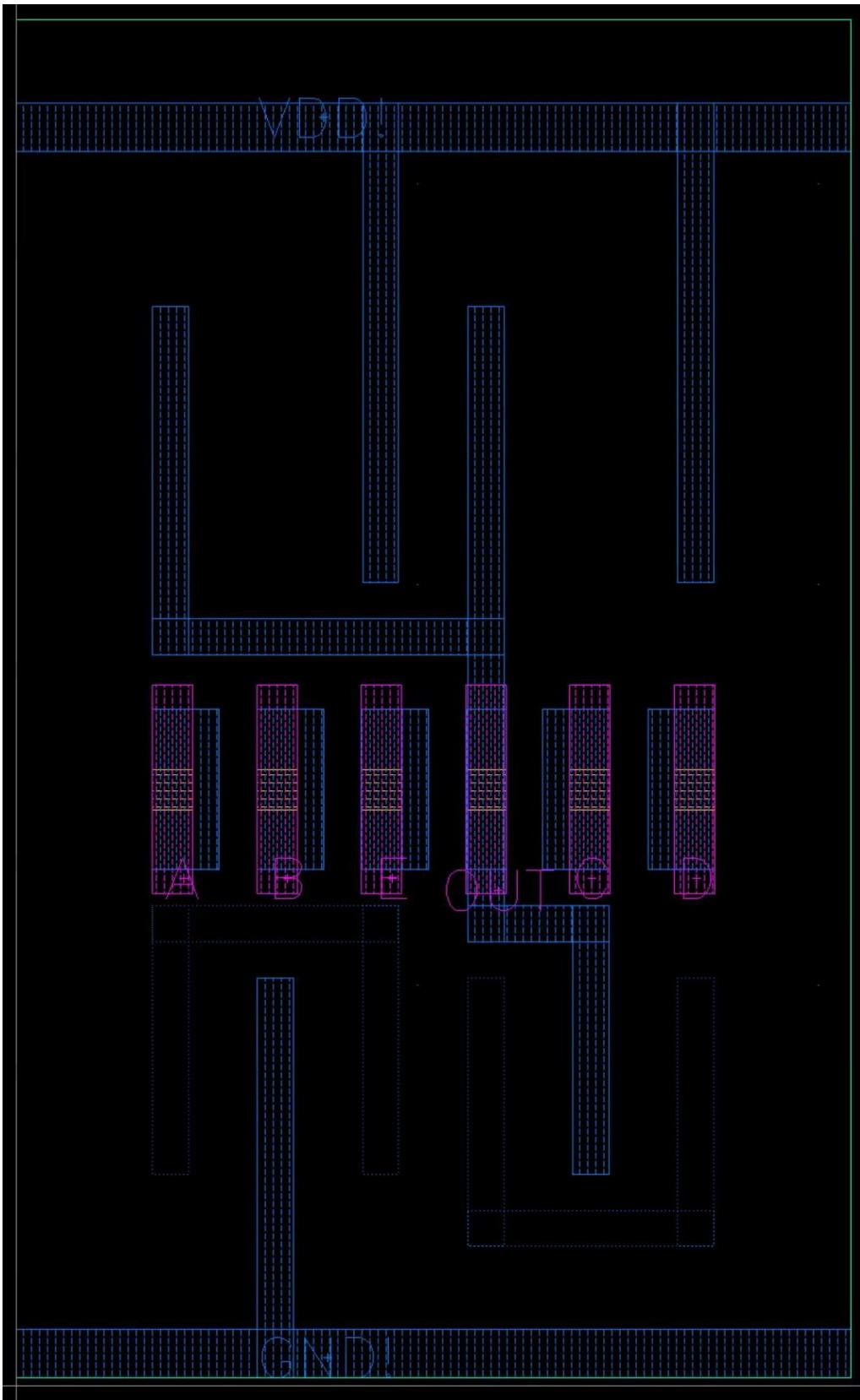
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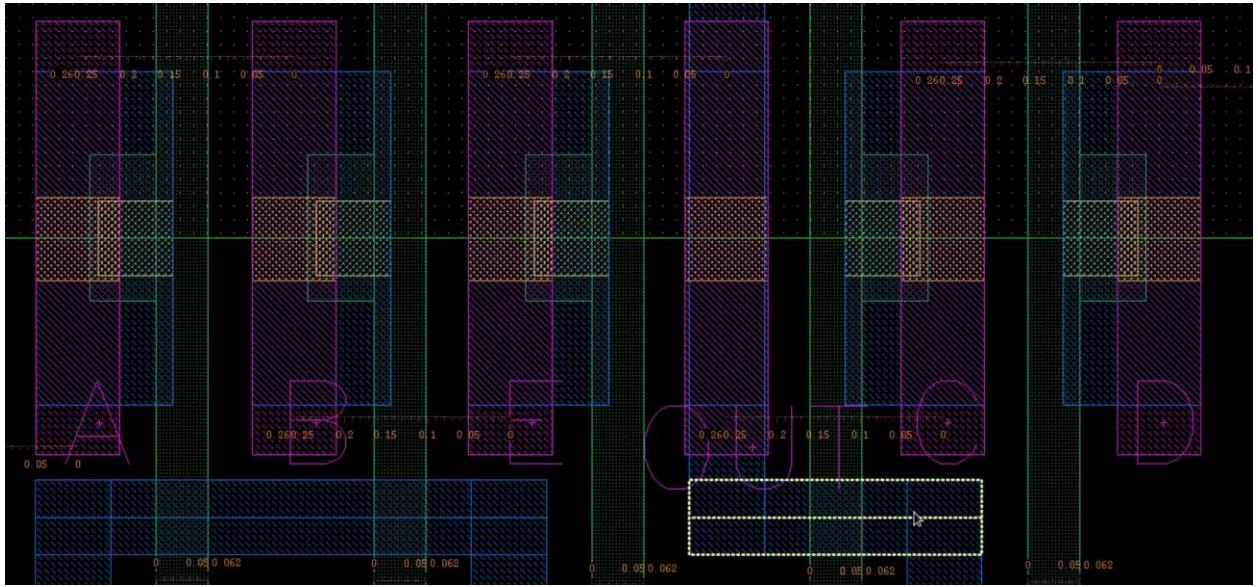
Layout:



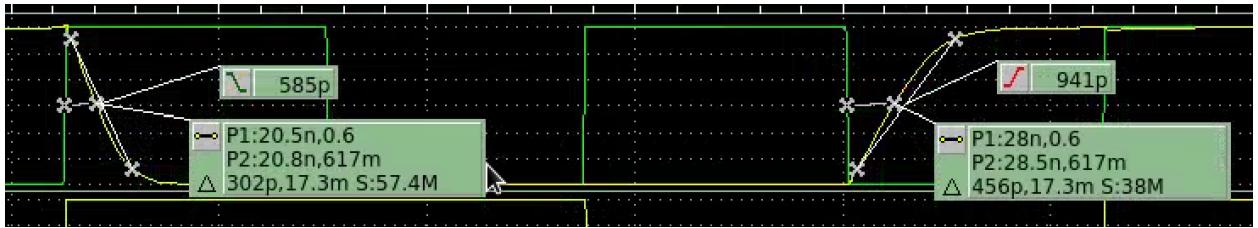
Abstract View:



Gate spacing:

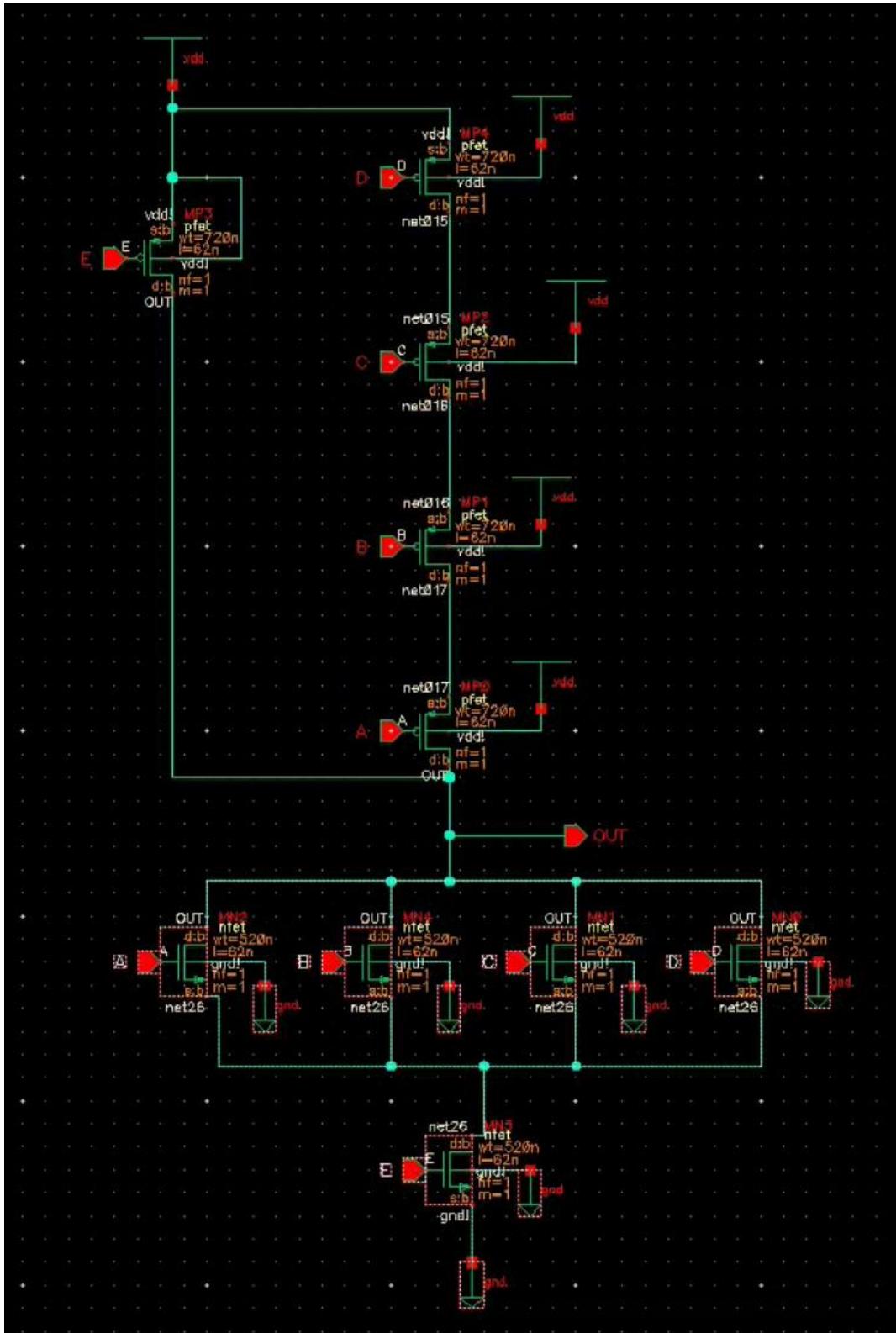


Hspice Simulation:

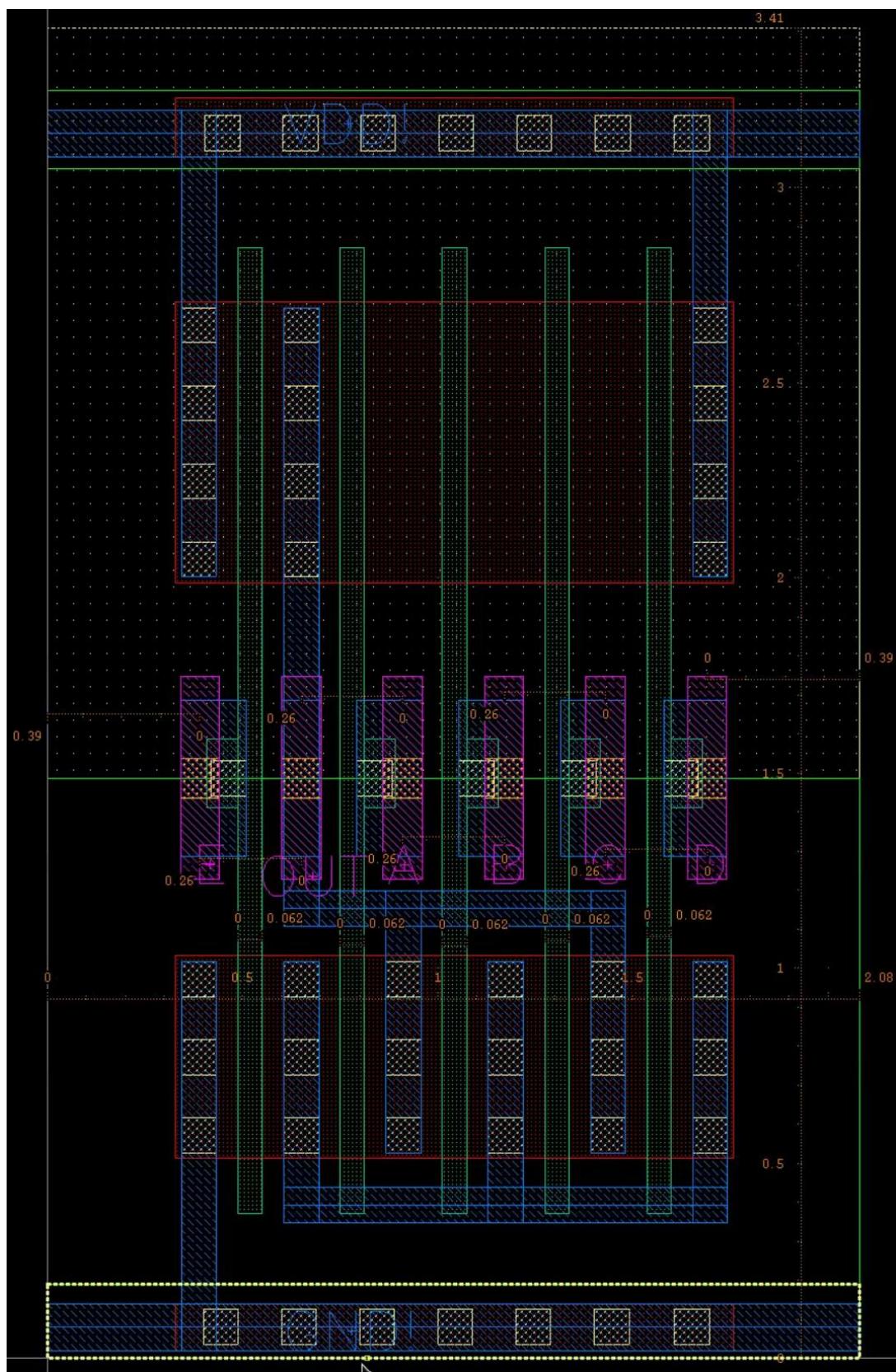


# OAI41

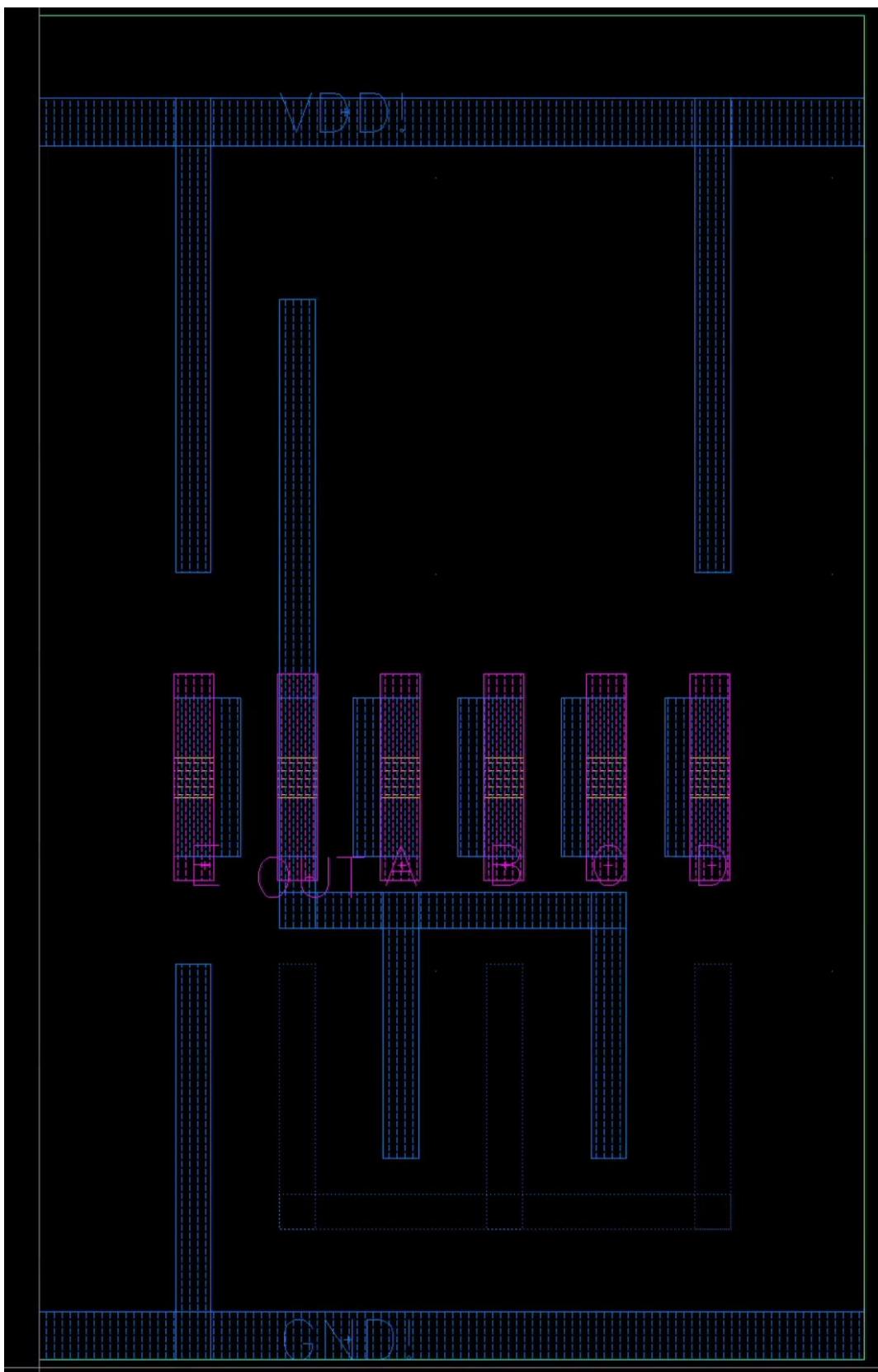
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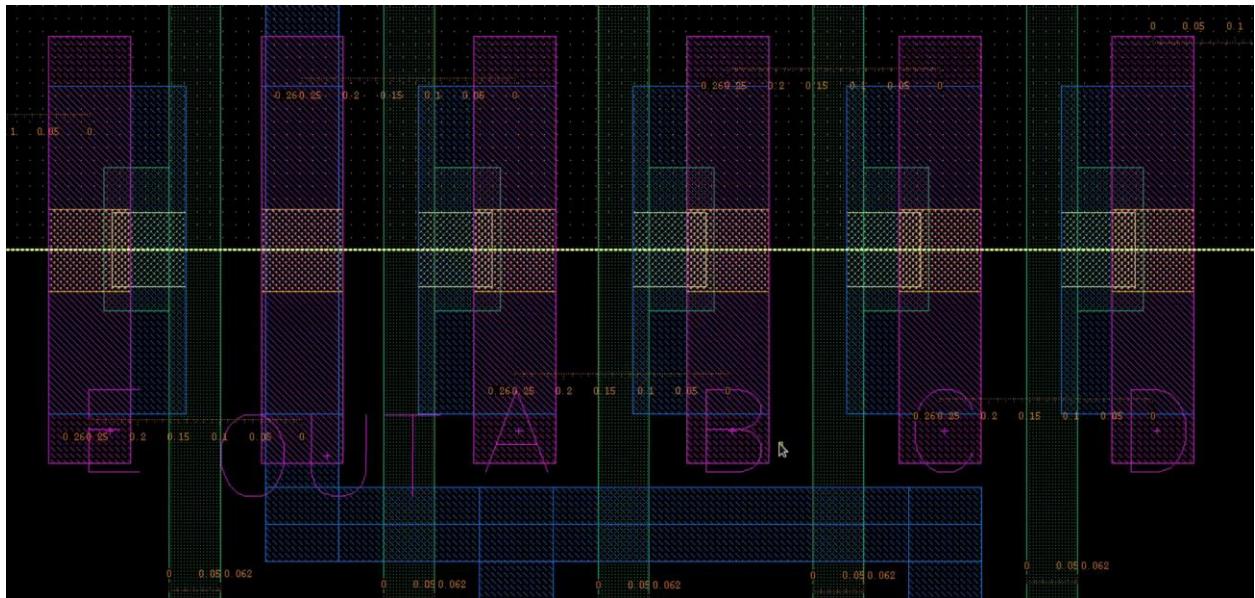
Layout:



Abstract View:



Gate spacing:

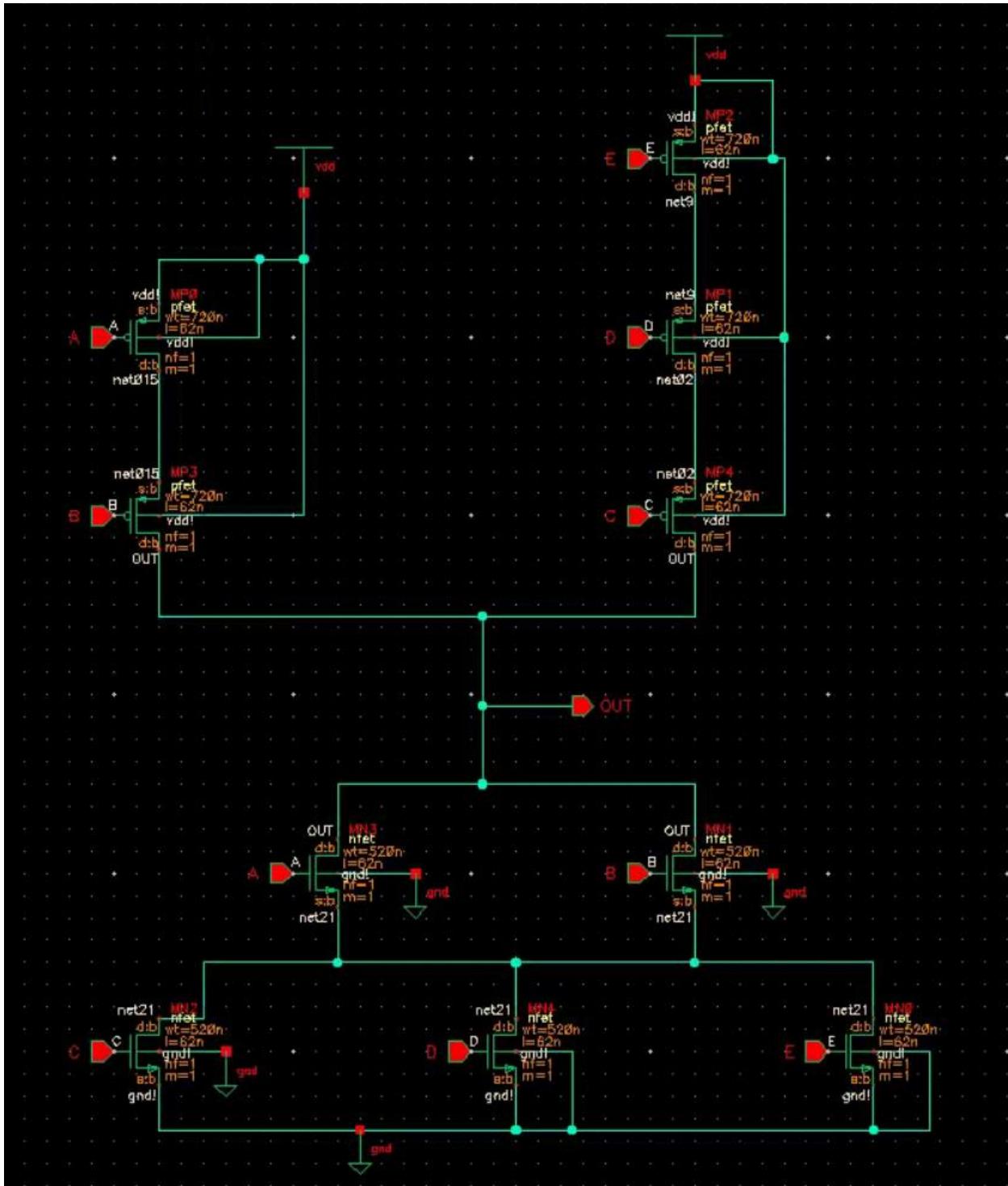


Hspice Simulation:

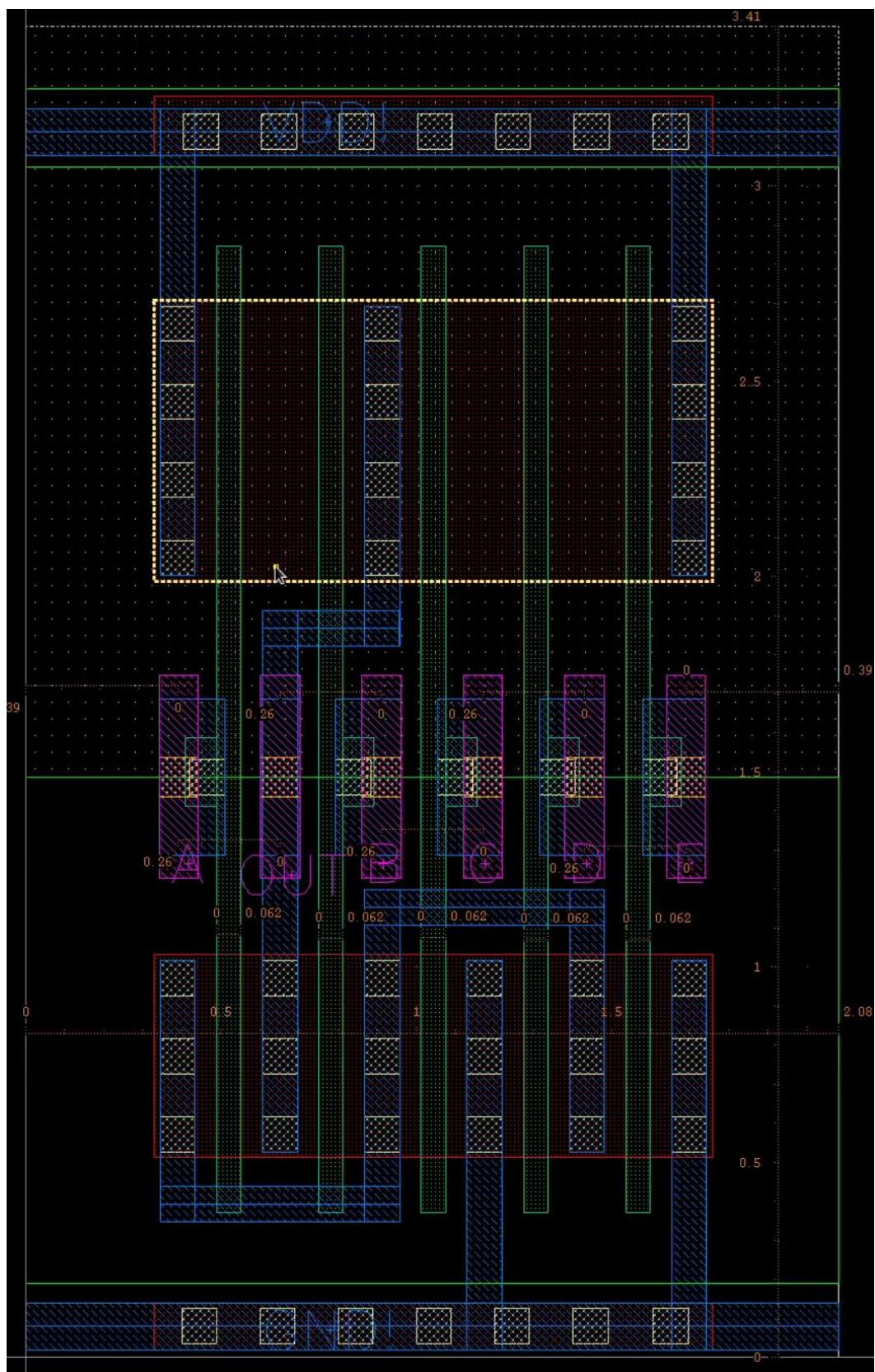


# OAI32

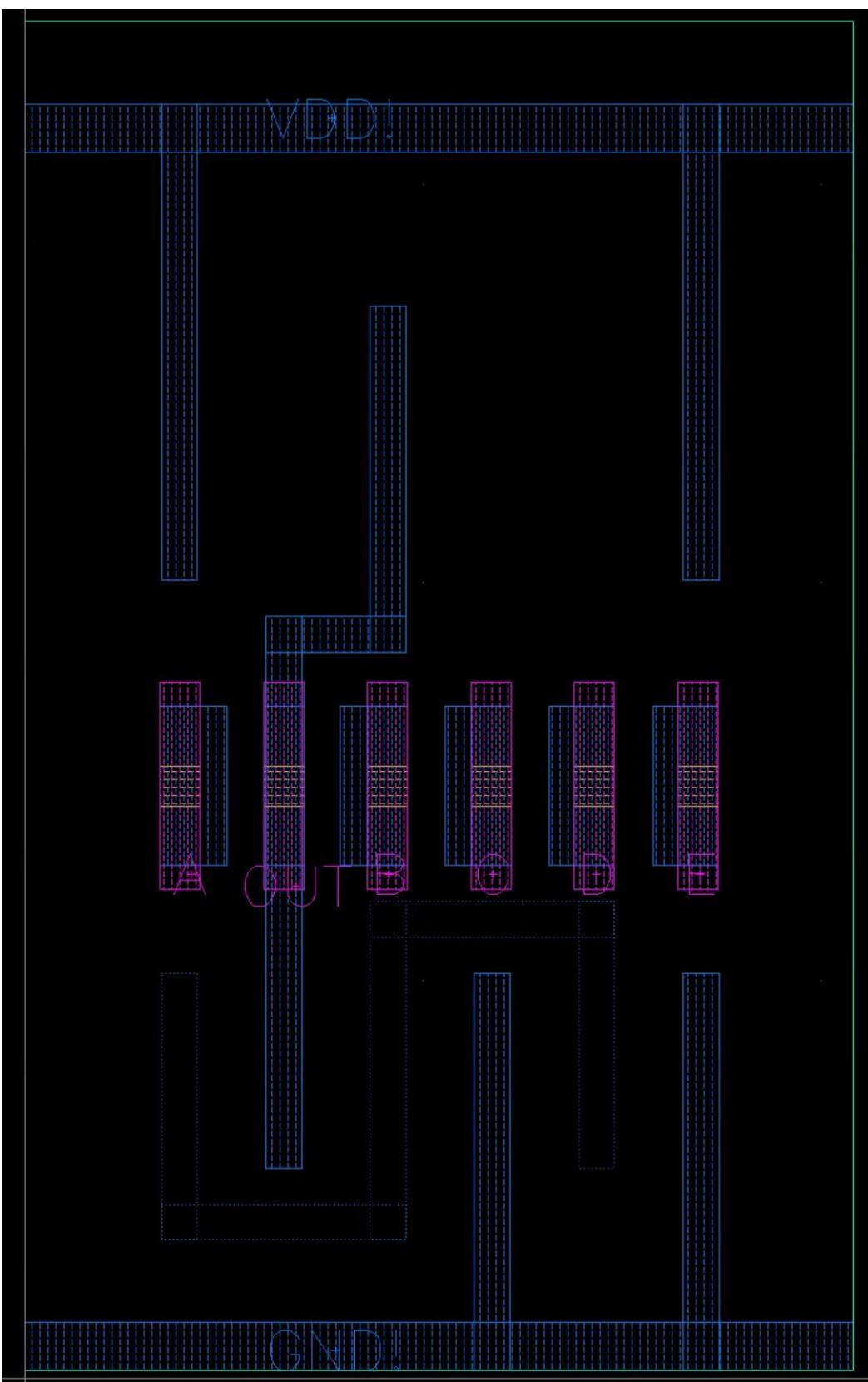
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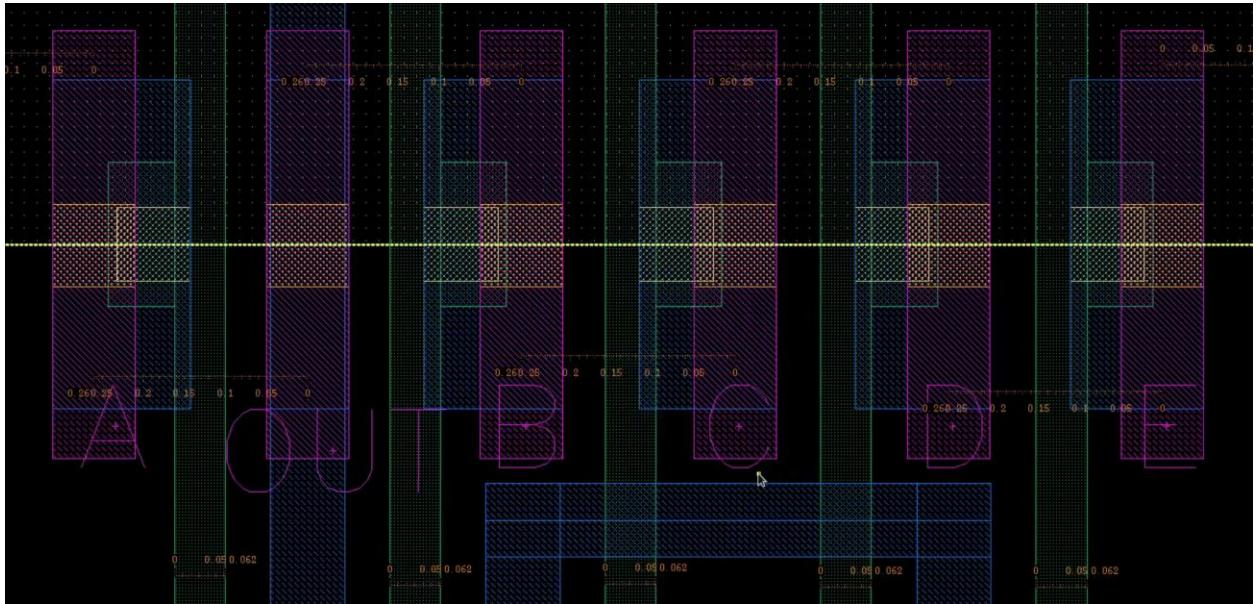
Layout:



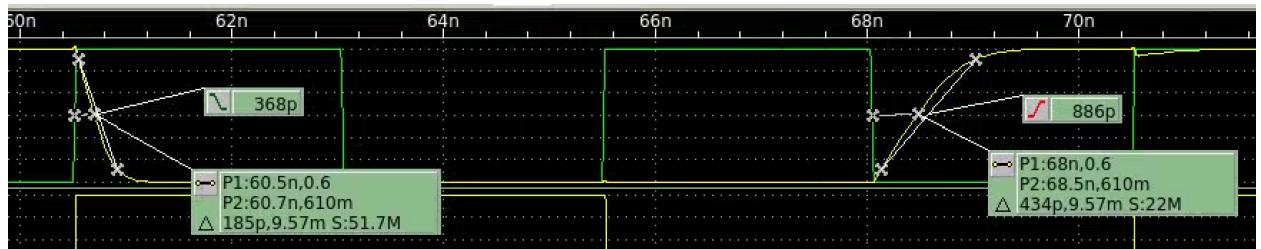
Abstract View:



Gate spacing:

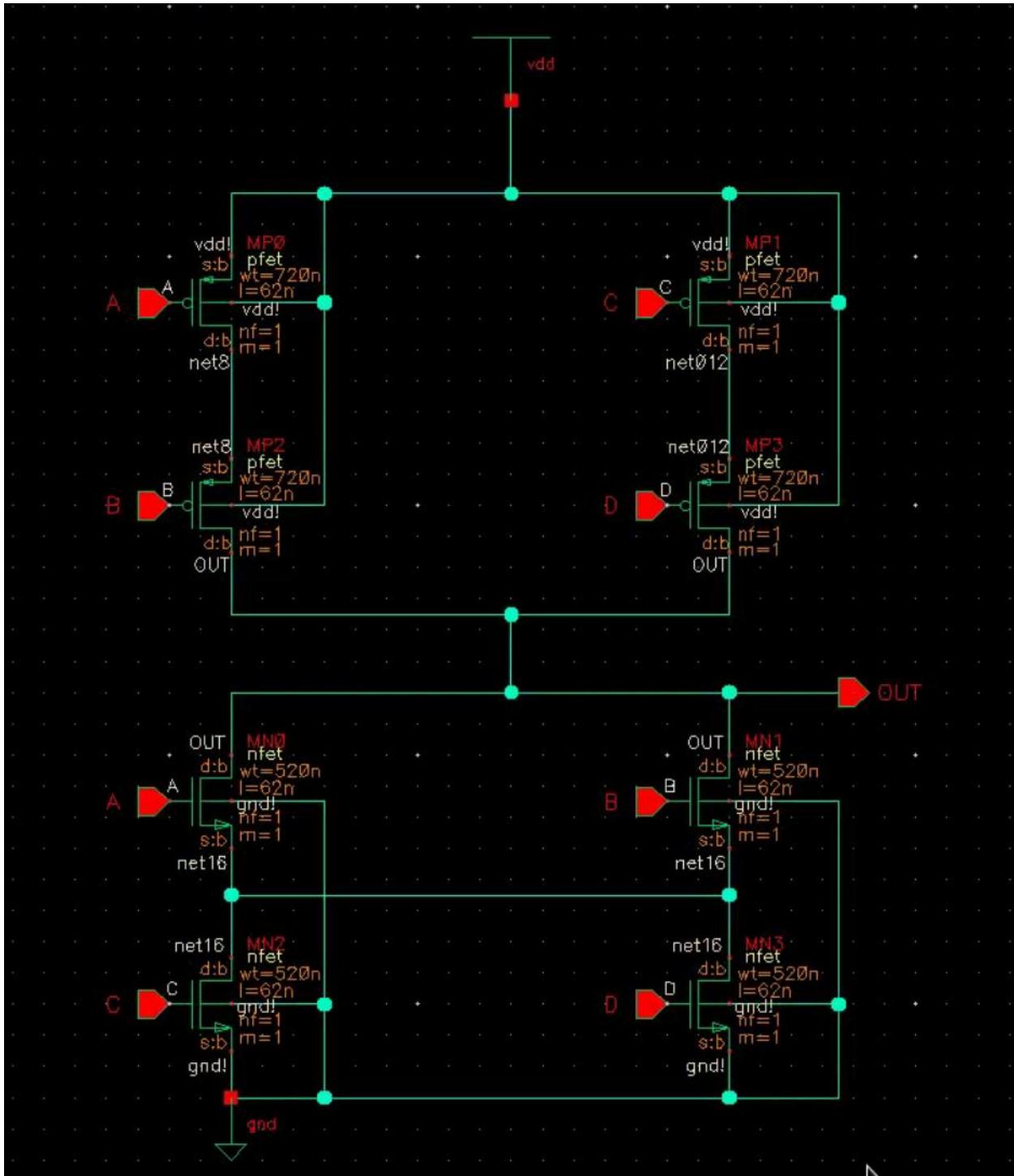


Hspice Simulation:

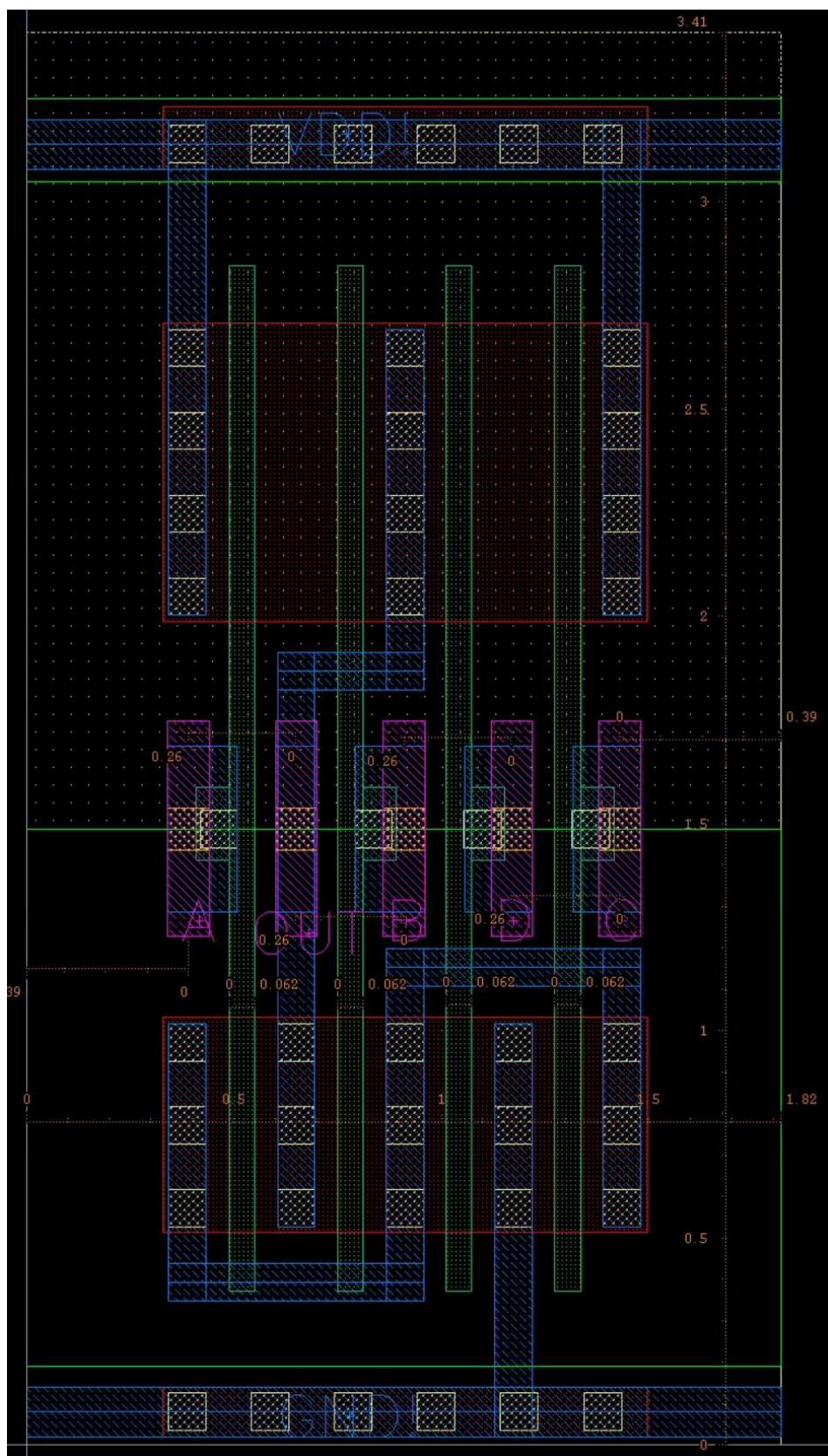


## OAI22

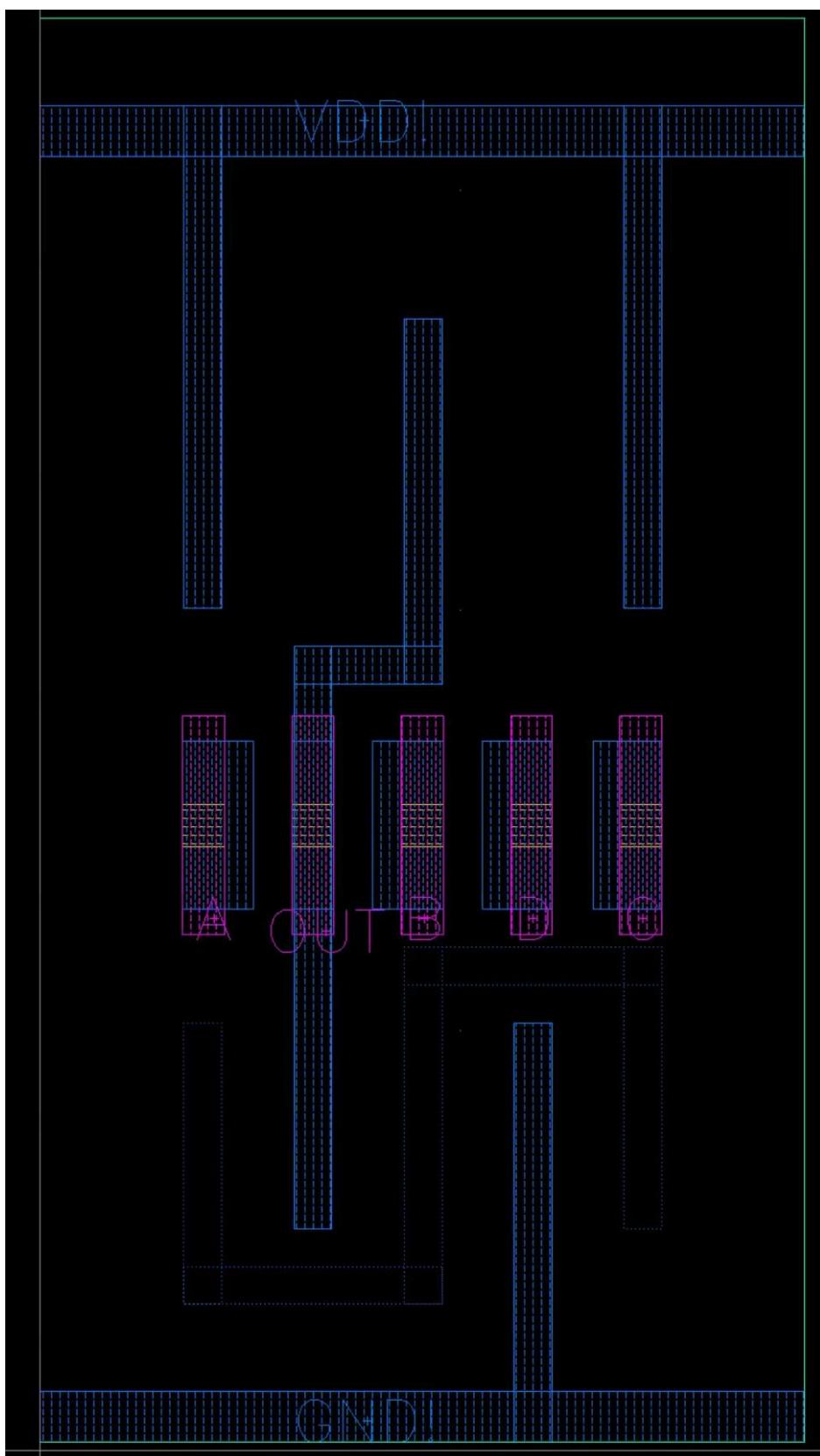
Schematic:



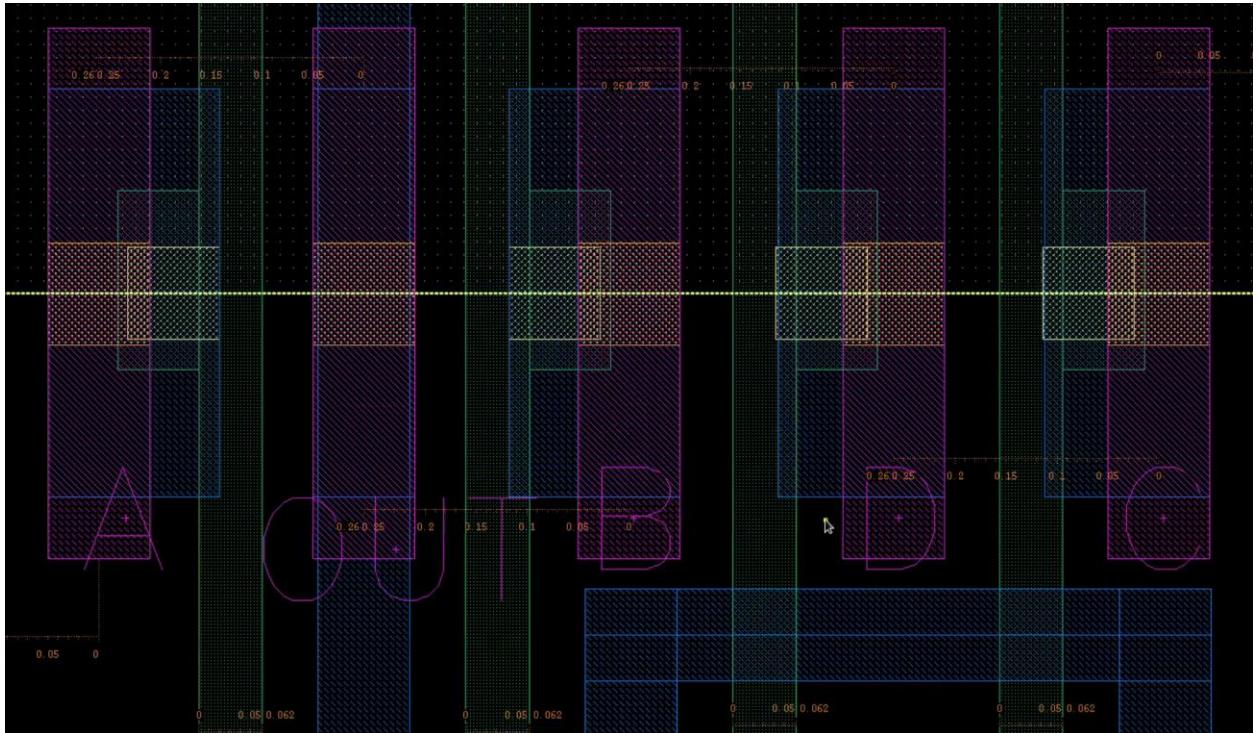
Layout:



Abstract View:



Gate spacing:

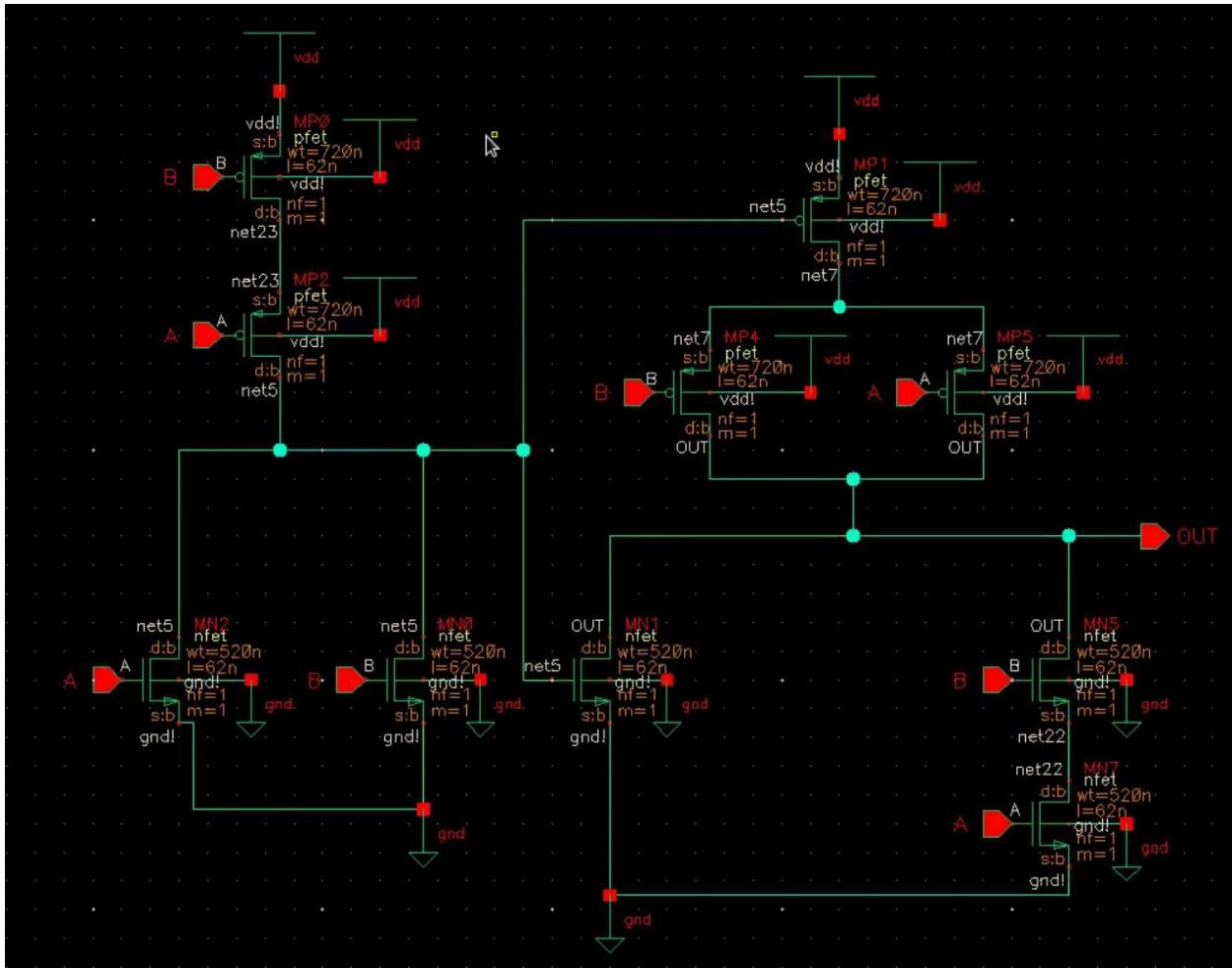


Hspice Simulation:

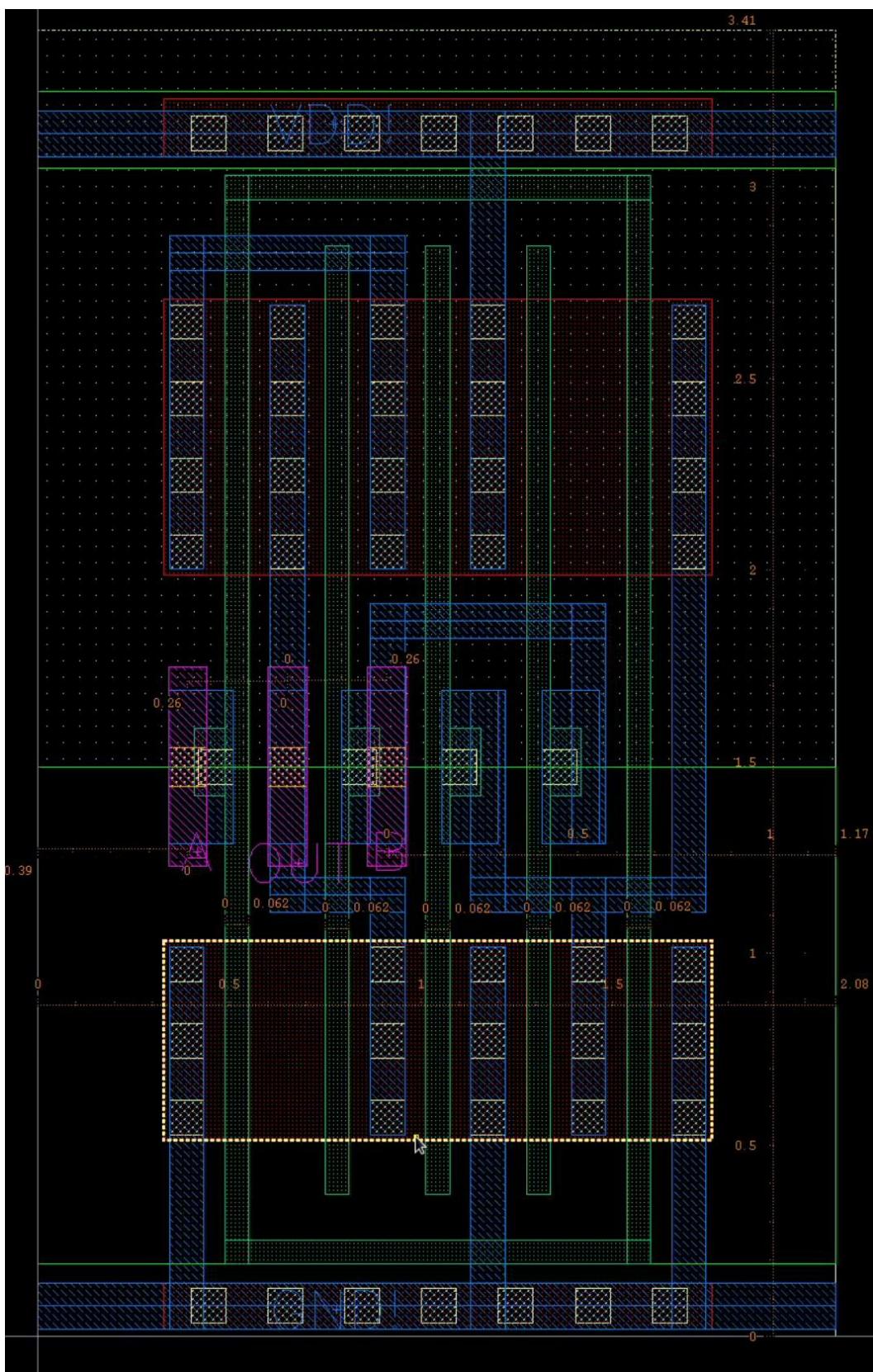


## XOR2

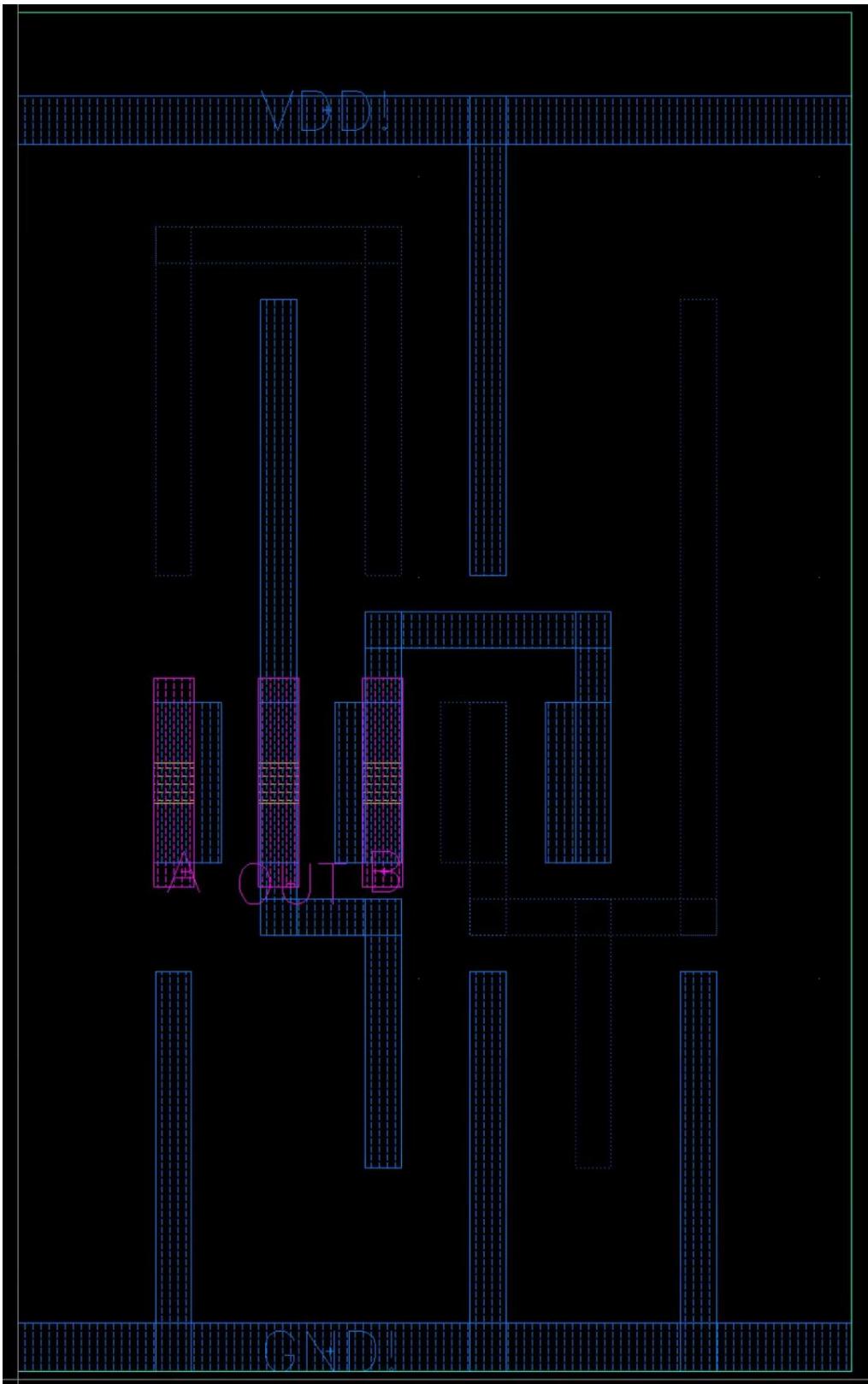
Schematic:



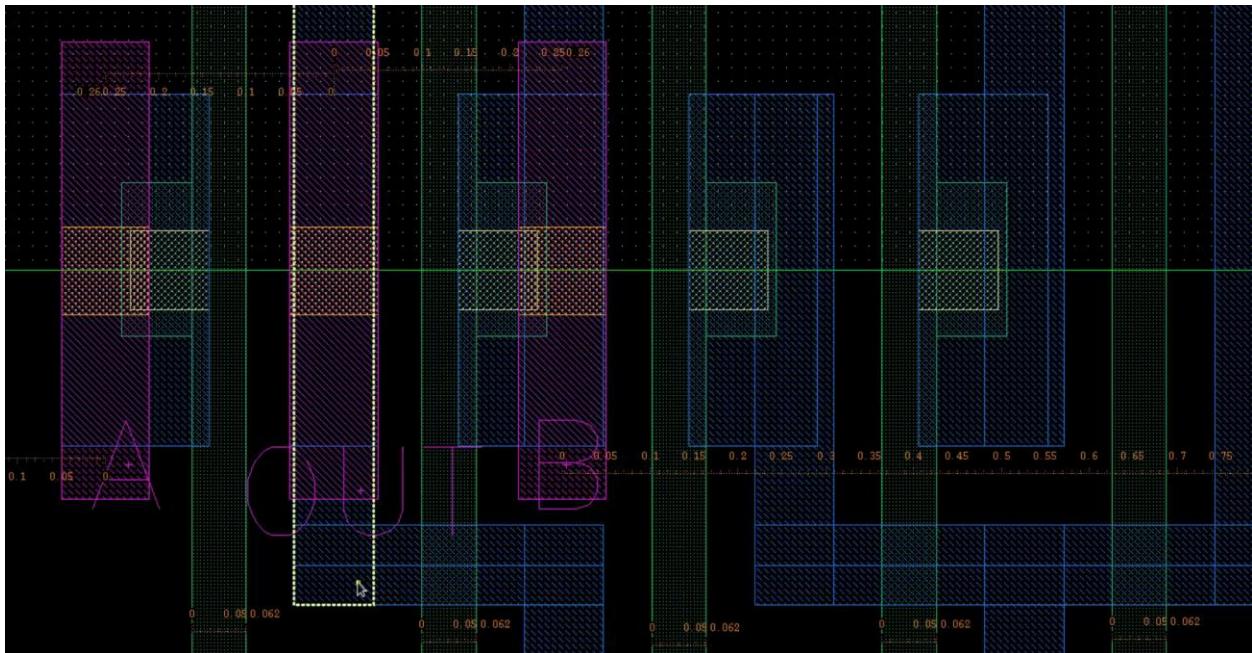
Layout:



Abstract View:



Gate spacing:



Hspice Simulation:

