Mark Ivey

mxi240020

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Project 5

Project 5: D Flip Flop

Times:

TSU\_DD\_ONE : -20ps (20 ps after clock edge)

TSU\_OPT\_ONE : 8ps (8 ps before clock edge)

THOLD\_ONE :~ 30ps

TSU\_DD\_ZERO : 39ps

TSU\_OPT\_ZERO : 45ps

THOLD\_ZERO : 65ps

TSU : 45 ps

THOLD : 65 ps

TD : 371ps (D low-to-high to Q)

TCLK->Q : 326ps

DFF Dimensions: 7.54 µm (width) x 3.735 µm (hight)

DFF Layout

A computer screen shot of a maze

Description automatically generated

Measurements and Contact Spacing

A computer screen shot of a maze

Description automatically generated

Figure 1: Abstract view

Methodology and Thought Process of the Layout

A diagram of a system

Description automatically generated with medium confidence

Figure 2: Euler Trail and Odd Nodes

In the annotated schematic above, it shows the thought process behind how I came up with two diffusion breaks and what gates I chose to connect. In the actual layout, I placed the clock in the center of the two mux/nor structures. Doing this allowed me to minimize the size of the gate; having the clock on the left or right would increase the width by 760 nm, as the metal 1 traces of CLK and would have to go around the input or output.

To get the TSU\_OPT, TSU\_DD, THOLD, TD and TCLK->Q, I did the following:

1. First, for the case of D going high to low, I used hspice to get a rough estimate, to the nearest 100 ps, for TSU\_DD
2. Then, using a script, 100-200 points were tested via a script in 1 ps increments.
3. The results were graphed and TSU\_OPT, TSU\_DD were determined.
4. Using TSU\_OPT, I then calculated THOLD
5. The process was repeated for D going low to high
6. For the final values of TD and TCLK->Q, I used the best worst case from TSU\_OPT, and THOLD. In my case, this turned out to be TSU\_OPT\_ZERO.

TSU\_DD\_ONE : -20ps (20 ps after clock edge)

TSU\_OPT\_ONE : 8ps (8 ps before clock edge)

THOLD\_ONE :~ 30ps

TSU\_DD\_ZERO : 39ps

TSU\_OPT\_ZERO : 45ps

THOLD\_ZERO : 65ps

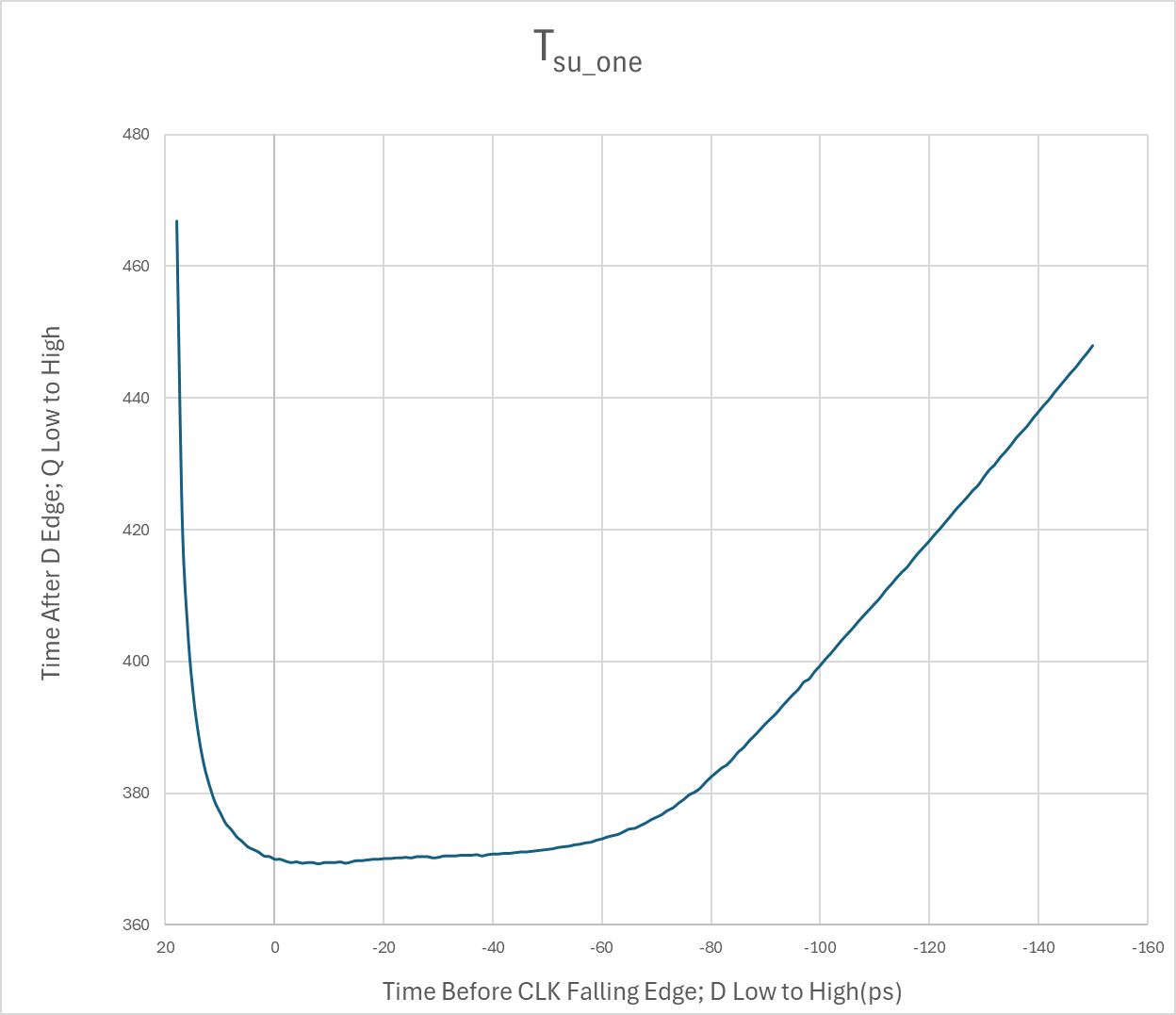
TSU : 45 ps

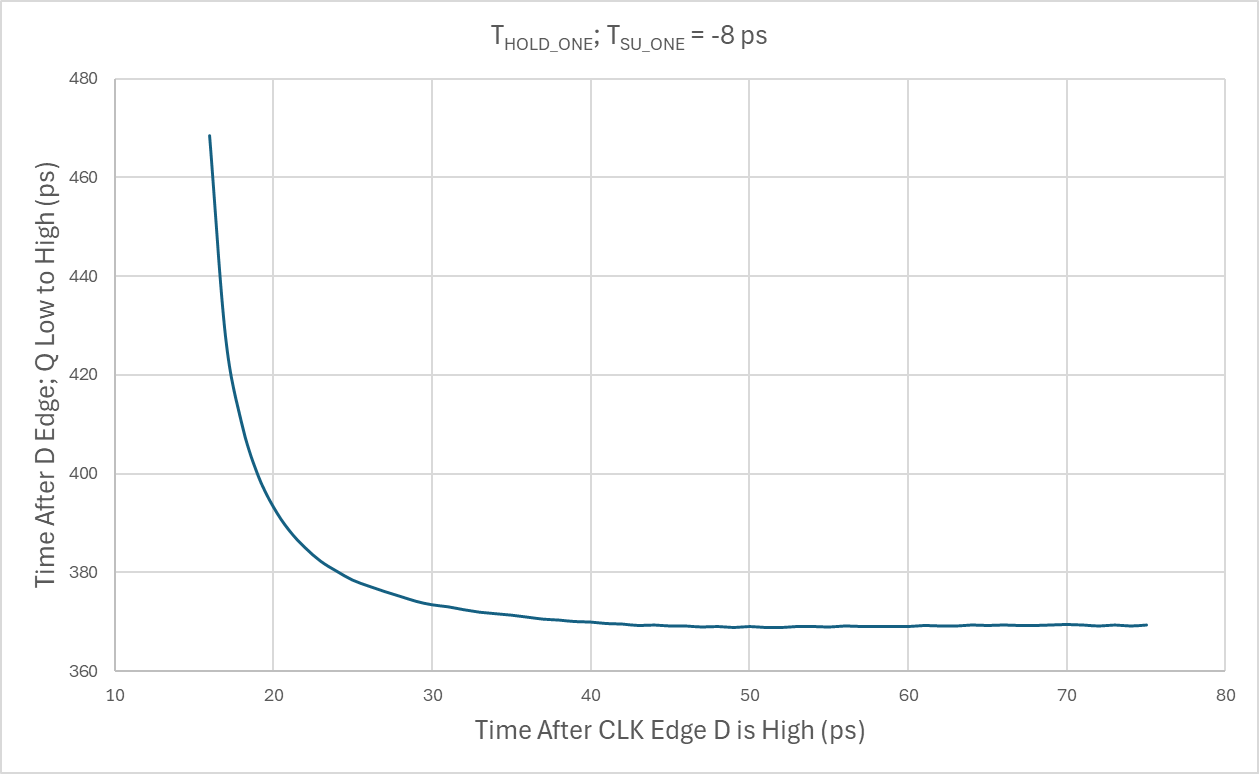
THOLD : 65 ps

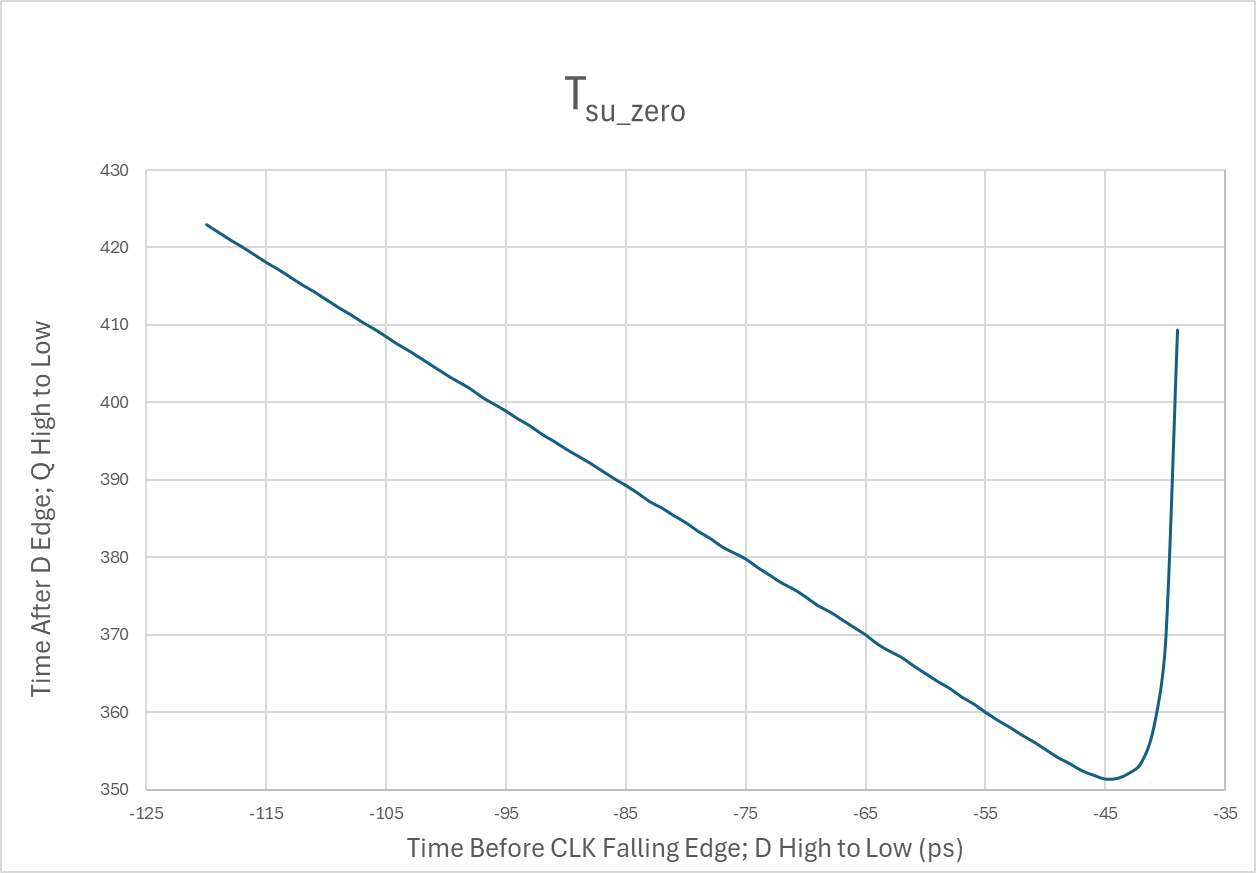
TD : 371ps (D low-to-high to Q)

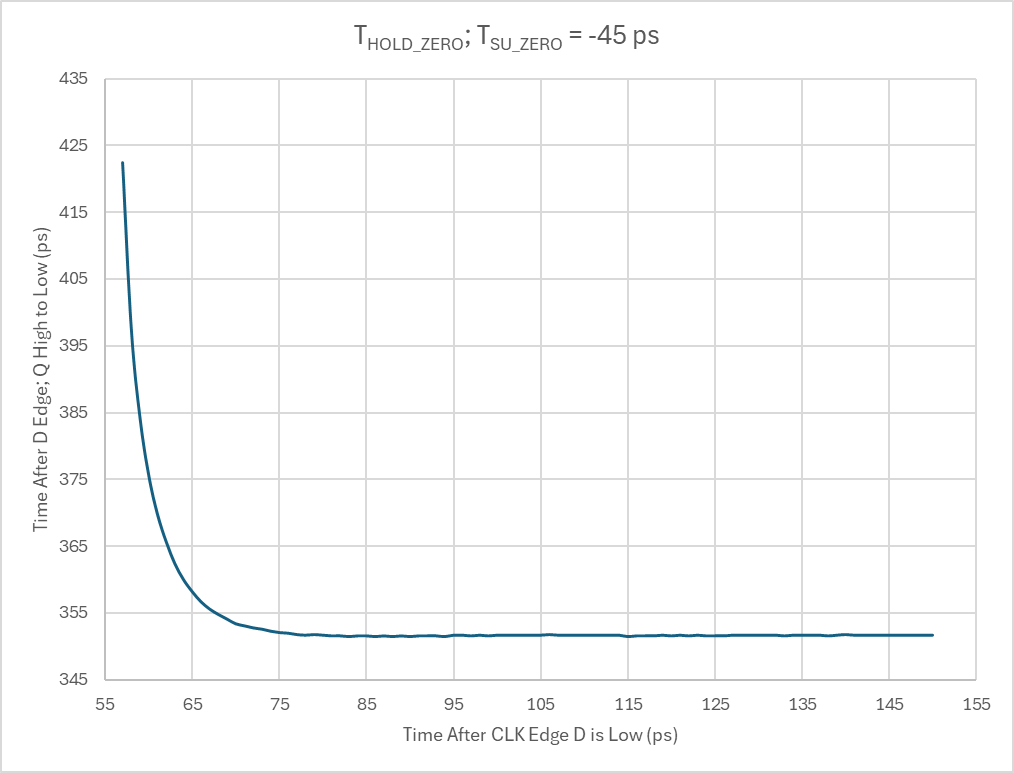
TCLK->Q : 326ps

These values were selected because the slew rate of Q from zero-to-one was lower than one-to-zero









A screen shot of a graph

Description automatically generated

Figure 3: CLK -> Q and delay of Rising and Falling Data