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Project 5

Project 5: D Flip Flop

Times:

$T_{SU\_DD\_ONE}$: -20ps (20 ps after clock edge)

$T_{SU\_OPT\_ONE}$: 8ps (8 ps before clock edge)

T_{HOLD_ONE} :~ 30ps

$T_{SU\_DD\_ZERO}$: 39ps

$T_{SU\_OPT\_ZERO}$: 45ps

T_{HOLD_ZERO} : 65ps

T_{SU} : 45 ps

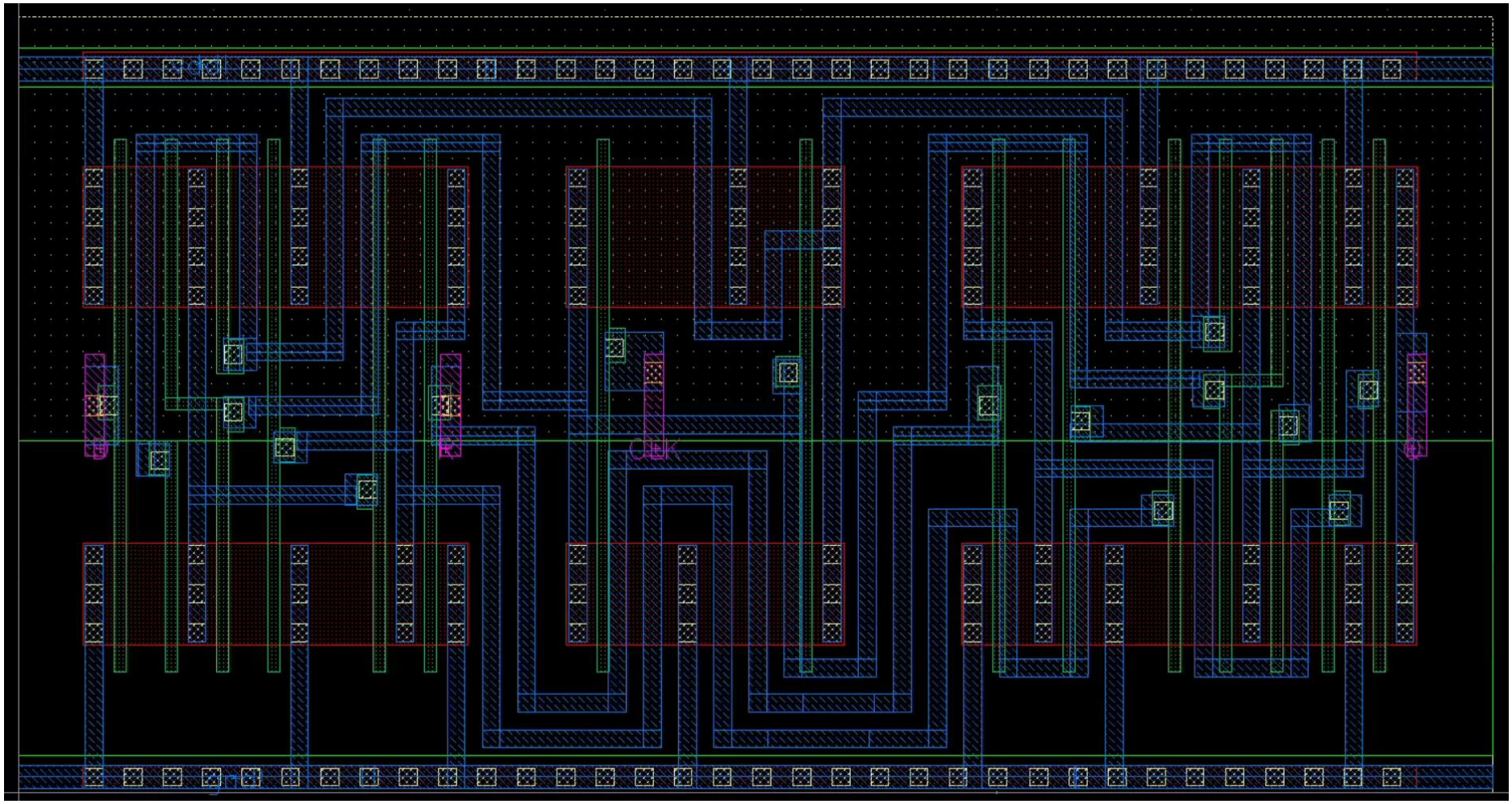
T_{HOLD} : 65 ps

T_{D} : 371ps (D low-to-high to Q)

$T_{CLK->Q}$: 326ps

DFF Dimensions: 7.54 µm (width) x 3.735 µm (hight)

DFF Layout



Measurements and Contact Spacing

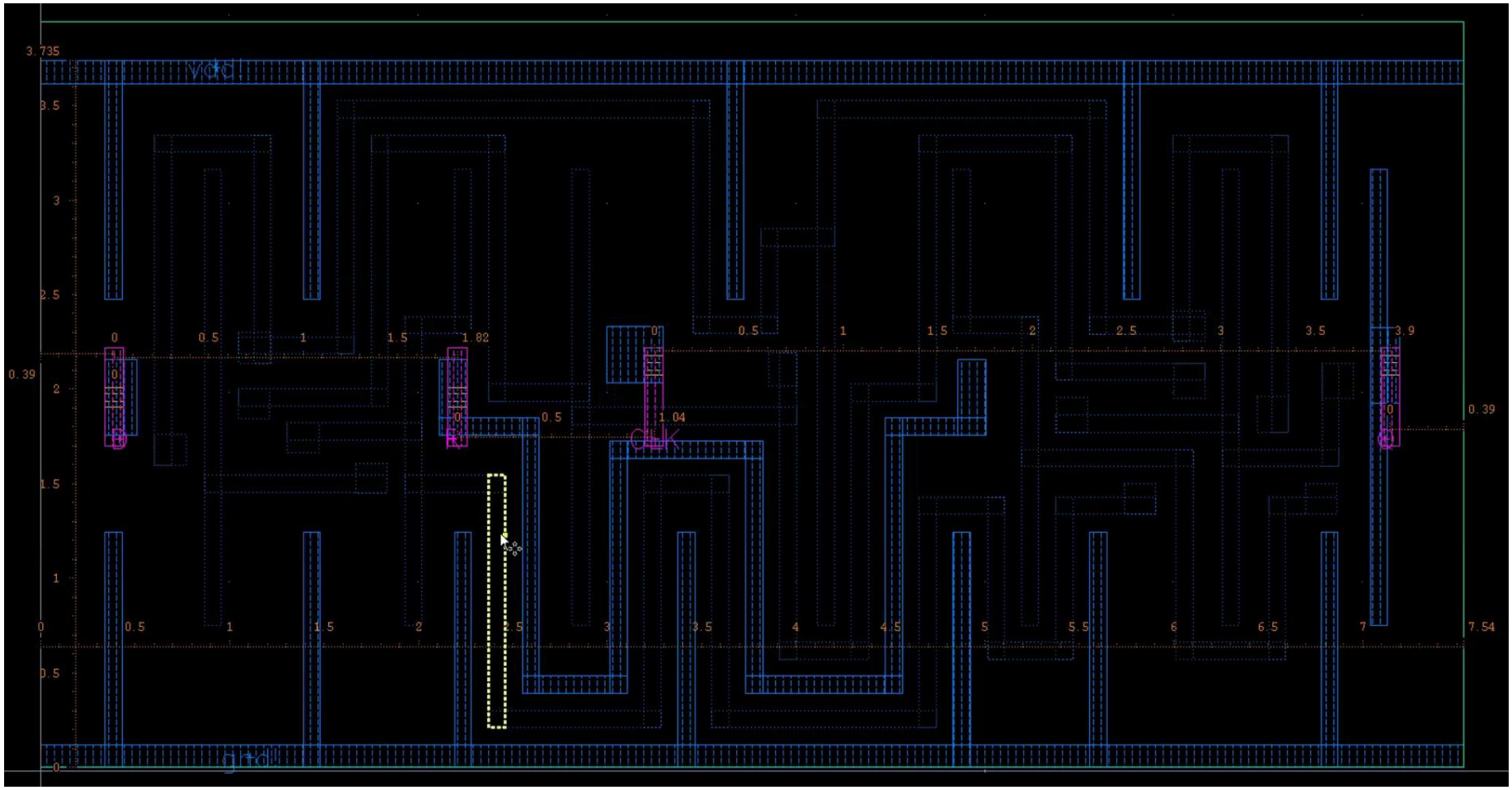


Figure 1: Abstract view

Methodology and Thought Process of the Layout

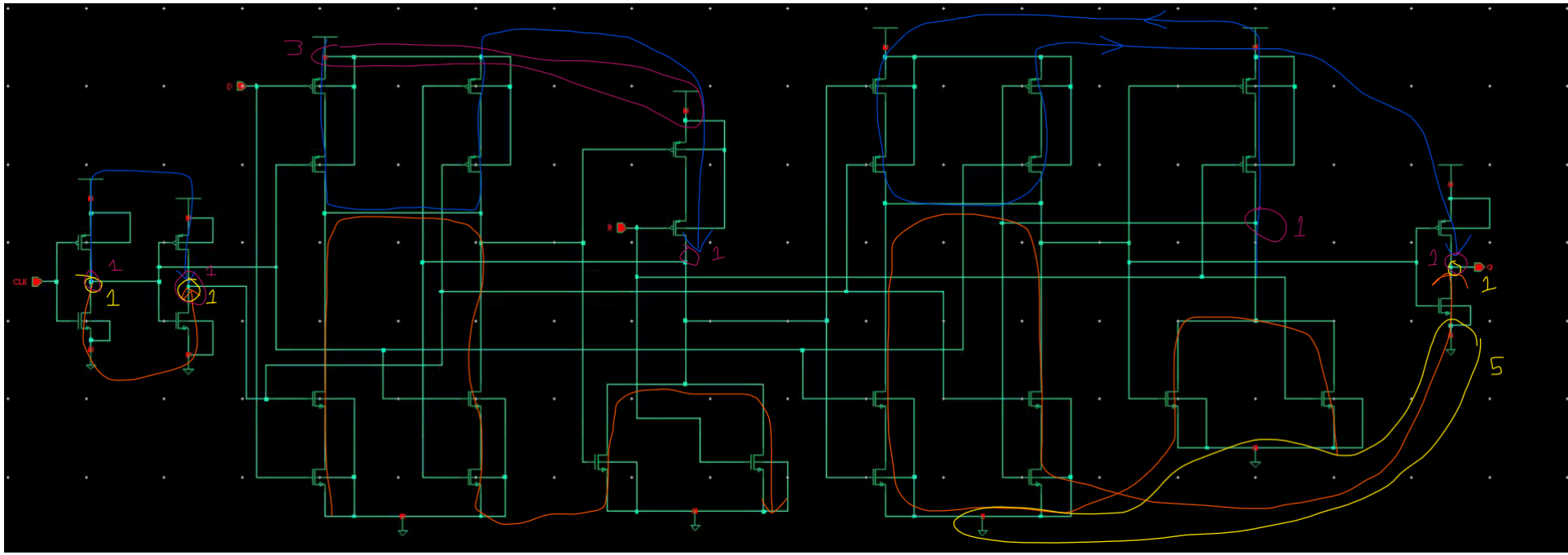


Figure 2: Euler Trail and Odd Nodes

In the annotated schematic above, it shows the thought process behind how I came up with two diffusion breaks and what gates I chose to connect. In the actual layout, I placed the clock in the center of the two mux/nor structures. Doing this allowed me to minimize the size of the gate; having the clock on the left or right would increase the width by 760 nm, as the metal 1 traces of CLK and $\overline{CLK}$ would have to go around the input or output.

To get the T_{SU_OPT}, T_{SU_DD}, T_{HOLD}, T_D and $T_{CLK->Q}$, I did the following:

1) First, for the case of D going high to low, I used hspice to get a rough estimate, to the nearest 100 ps, for T_{SU_DD}
2) Then, using a script, 100-200 points were tested via a script in 1 ps increments.
3) The results were graphed and T_{SU_OPT}, T_{SU_DD} were determined.
4) Using T_{SU_OPT}, I then calculated T_{HOLD}
5) The process was repeated for D going low to high
6) For the final values of T_D and $T_{CLK->Q}$, I used the best worst case from T_{SU_OPT}, and T_{HOLD}. In my case, this turned out to be $T_{SU\_OPT\_ZERO}$.

$T_{SU\_DD\_ONE}$: -20ps (20 ps after clock edge)

$T_{SU\_OPT\_ONE}$: 8ps (8 ps before clock edge)

T_{HOLD_ONE} :~ 30ps

$T_{SU\_DD\_ZERO}$: 39ps

$T_{SU\_OPT\_ZERO}$: 45ps

T_{HOLD_ZERO} : 65ps

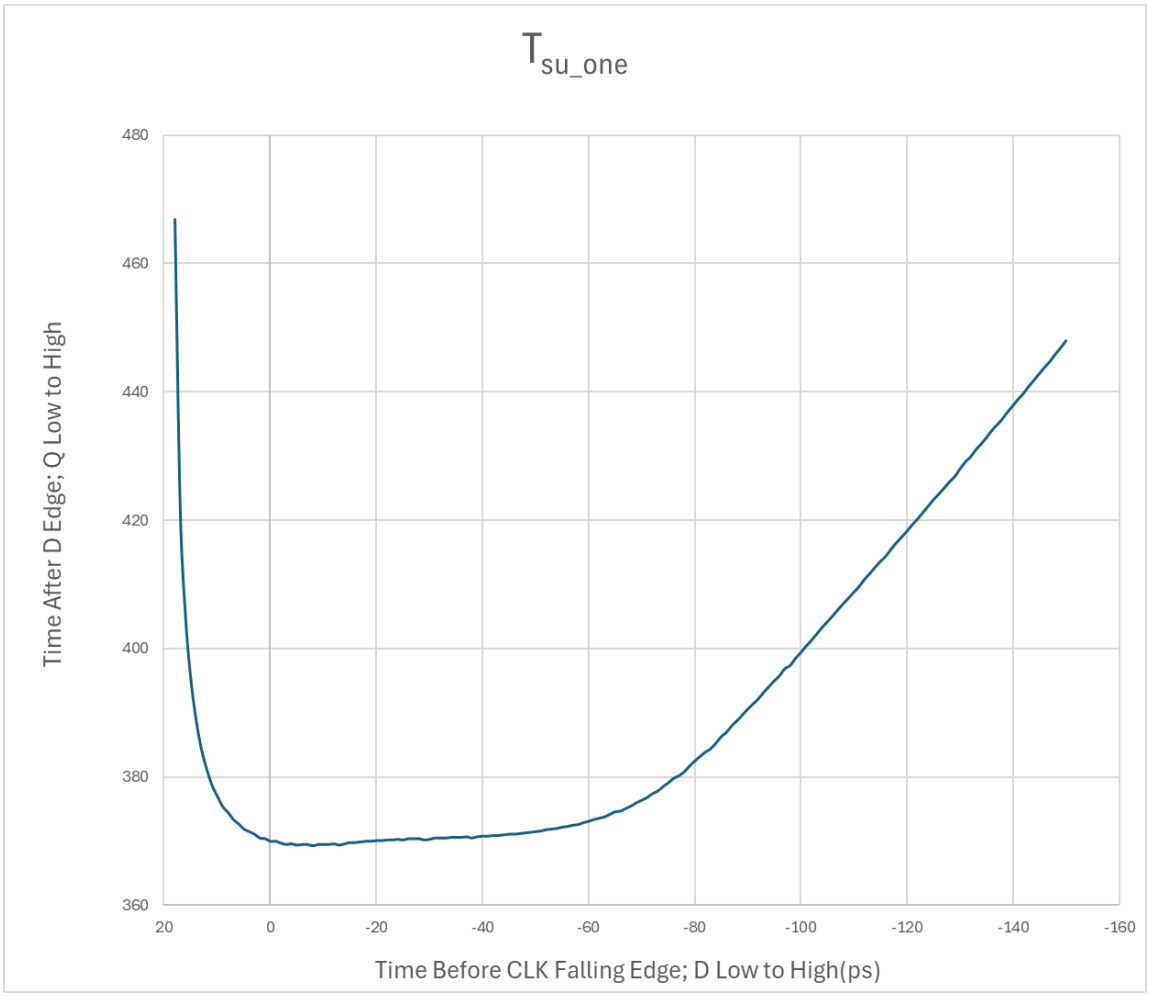
T_{SU} : 45 ps

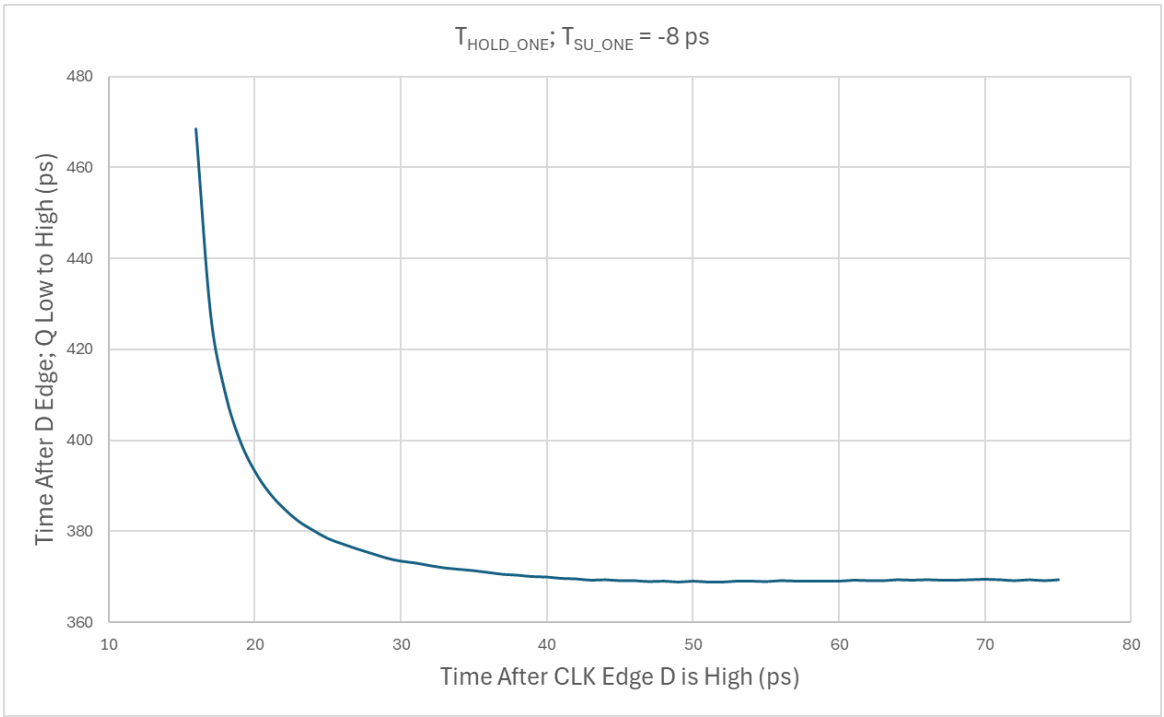
T_{HOLD} : 65 ps

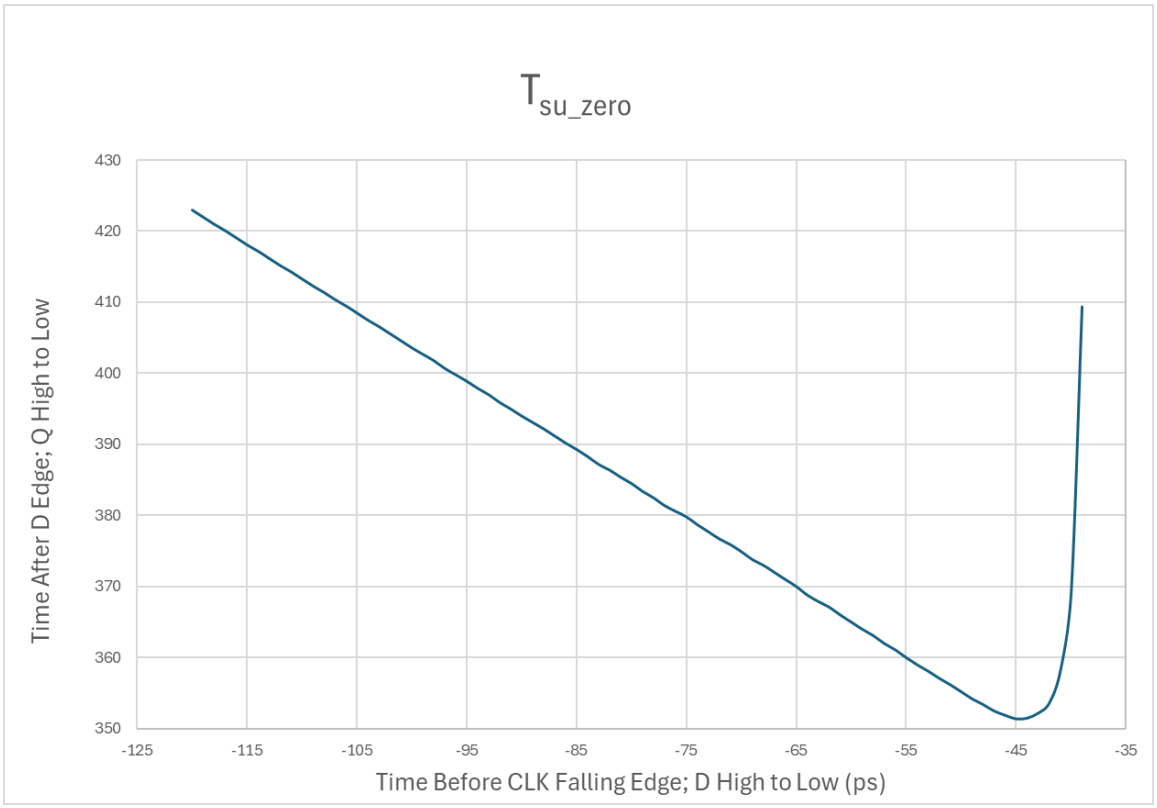
T_D : 371ps (D low-to-high to Q)

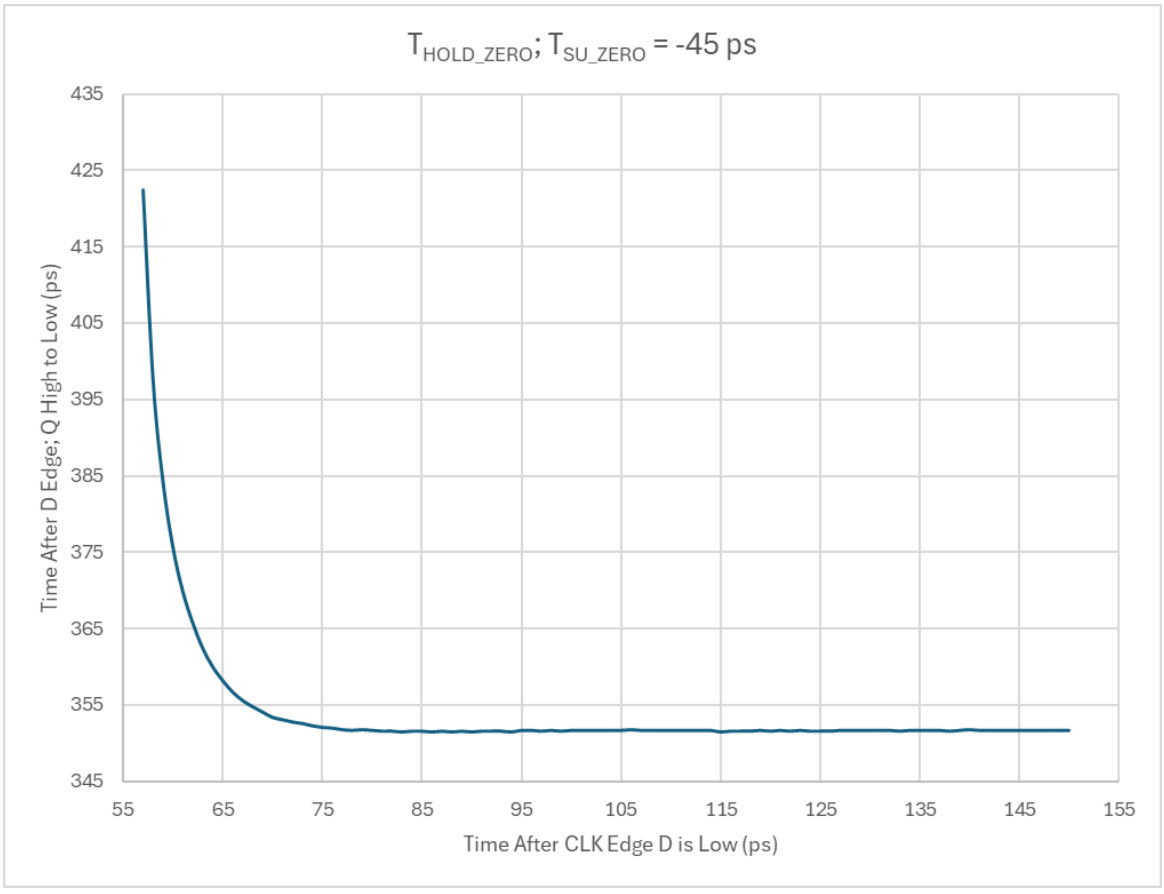
$T_{CLK->Q}$: 326ps

These values were selected because the slew rate of Q from zero-to-one was lower than one-to-zero


T_{su_one}
480
460
440
420
400
380
360
Time After D Edge; Q Low to High
20
0
-20
-40
-60
-80
-100
-120
-140
-160
Time Before CLK Falling Edge; D Low to High(ps)


T_{HOLD_ONE}; T_{SU_ONE} = -8 ps
480
460
440
420
400
380
360
Time After D Edge; Q Low to High (ps)
10
20
30
40
50
60
70
80
Time After CLK Edge D is High (ps)


T_{su_zero}
Time After D Edge; Q High to Low
430
420
410
400
390
380
370
360
350
-125
-115
-105
-95
-85
-75
-65
-55
-45
-35
Time Before CLK Falling Edge; D High to Low (ps)


T_{HOLD_ZERO}; T_{SU_ZERO} = -45 ps
Time After D Edge; Q High to Low (ps)
435
425
415
405
395
385
375
365
355
345
55
65
75
85
95
105
115
125
135
145
155
Time After CLK Edge D is Low (ps)

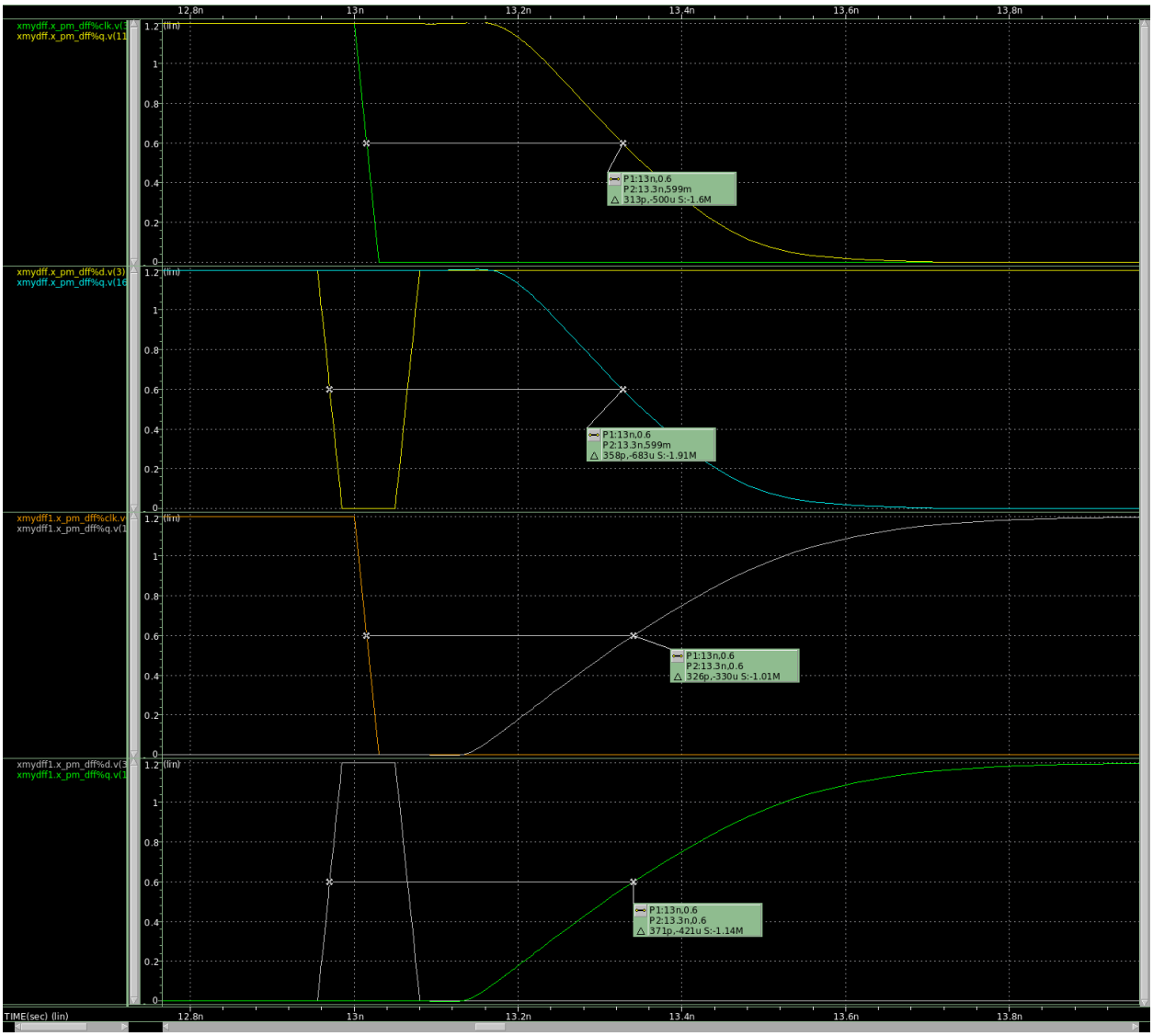


Figure 3: CLK -> Q and delay of Rising and Falling Data