DLTS Basics

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Chapter 1

Crystallographic Defects and Trap States

Imperfections in the crystal structure of solids are known as crystallographic defects. Such a defect may have an impact upon the electronic properties of a semiconductor, such as reduced carrier mobility by impurity scattering. When a defect introduces an electronic state in the forbidden energy region of the bandgap, that state may be considered a trap state. Doping is the well-known process of purposely introducing shallow-level traps that change the Fermi-level of the solid and can lead to the creation of n-type and p-type semiconductors. Deep-level traps lie closer in energy to mid-gap and are often undesirable as they lead to reduced conductivity and/or high rates of SRH recombination. The relationship between crystallographic defects, electronic trap states, and solid-state device performance are often complex and difficult to predict [1].

Crystalline defects can be categorized by their dimensionality. In increasing order, those categories are point, line, planar, and bulk defects [2].

Point defects include vacancies, anti-sites, intrinsic and extrinsic interstitials, and substitutions by impurities. These are difficult to detect physically due to their size, but they are always present and in sufficient concentration they may have a substantial effect upon the electronic properties of a semiconductor. Doping is an example of a substitution defect where a host atom is replaced by an impurity. Impurity concentration (substitutions, extrinsic interstitials) can be physically detected by SIMS, however, this measurement cannot detect intrinsic point defects (vacancies, anti-sites, intrinsic interstitials), where all atoms involved are part of the host crystal. To find these defects, electronic testing such as Hall effect or depletion-capacitance defect spectroscopy are typically used. Another point-defect measurement of note is Fourier-transform infrared spectroscopy, where a sample is exposed to infrared radiation and chemical bonds absorb light at certain frequencies.

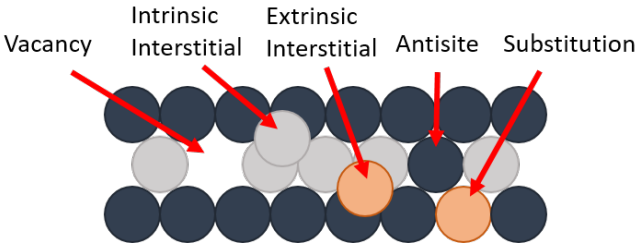

FIGURE 1.1: Simple depiction of crystallographic point defects.

Line defects include edge dislocations, screw dislocations, and dislocation loops. In III-V epitaxy, threading dislocations are of particular interest as their formation is due to strain relaxation when lattice-mismatched materials are grown, discussed in see Chapter **??**. For defects of this size and larger, TEM is frequently used to observe or count the defects [3]. EPD tests are also used to determine the cross-sectional density of threading dislocations [4].

Planar defects include anti-phase boundaries, grain boundaries, twins, and stacking faults. Boundaries between different phases of the material can result in dangling bonds and these defects may have been responsible for effects observed in InAlAsSb diodes in Chapter **??**.

Bulk or macroscopic defects include cracks, voids, and inclusions. Just a single of these types of defects can degrade solid-state device performance, as seen in Chapter **??**.

The effect of a point defect upon the electronic properties of a semiconductor depend on many factor besides its concentration. Not all impurities will have an apparent electronic impact, even in high concentration. In Czochralski-grown silicon wafers, it is well known that oxygen atoms contaminate the lattice upwards of 10^{18} atoms/cm^3 [5]. Some of these incorporate in the lattice as substitutions, which can be measured by an increase in the lattice constant using XRD. However, interstitial oxygen, measured by FTIR, is also present and has shown to be electrically inert or inactive. Annealing the wafer activates these interstitials and results in midgap states, where different states form at different annealing temperatures. Determining the exact physical reason behind phenomena such as this, or, in other words, the link between the atomic configuration and resulting electronic effects, is a difficult and complex problem to solve. The most proven approach is DFT with psuedopotentials [6, 7].

DFT is a quantum mechanical modeling technique where different defect configurations are modeled until one is found that best replicates the results from experiments such as defect spectroscopy. There a number of compounding complications which cannot be measured with accuracy, such as interaction of the defect with other surrounding defects or the defect charge state and its interaction with localized electric fields [1]. The DFT model combined with defect spectroscopy, therefore, is a potentially powerful tool and was used to understand the behavior of interstitial oxygen in silicon mentioned above [6]. DFT modeling is not covered in this work but awareness of it is important context to the study of defects in III-V crystals.

Higher dimensional defects may create defect bands in the bandgap and tend to efficiently facilitate nonradiative recombination for carriers less than a diffusion length away. These defect may also lead to shunting. There are techniques to mitigate or passivate them, such as

hydrogen passivation of dangling bonds in silicon [8]. The sidewalls of mesa-isolated devices represent a boundary defect which can dominate performance for devices with area in the 1 mm^2 range. There are a plethora of techniques developed to mitigate this boundary for a wide range of materials and device types, and sidewall passivation is an active area of research (see Chapter **??**).

The effect of trap-assisted recombination on III-V solar cell performance is decreased carrier lifetimes and an increase in the dark current. This reduces both the current and voltage. Current is lost if the MCDL of a generated carrier is lower than the distance the carrier must travel to the junction. The MCDL is related to the carrier lifetime by,

$$MCDL = \sqrt{D\tau}, \tag{1.1}$$

where D and τ are the minority carrier diffusion constant and the lifetime, respectively. The diffusion constant can be modeled using the Einstein relationship to be,

$$D = \mu \frac{k_B T}{q}, \tag{1.2}$$

where μ is the carrier mobility.

The inverse of the carrier lifetime in Equation 1.1 can be represented in terms of the various recombination mechanisms as,

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} \approx A + BN + CN^2, \tag{1.3}$$

where τ_{SRH}, τ_{rad}, and τ_{Auger} are the SRH, radiative, and Auger carrier lifetimes, respectively, and A, B, and C are the SRH, radiative, and Auger recombination coefficients, respectively.

From the right of Equation 1.3, it is seen that to the SRH lifetime normally does not depend on the majority carrier concentration, largely because the SRH lifetime is determined by the mid-gap trap density, N_t. The recombination coefficients B and C are material dependent, as they depend on the band structure, and can be found in databases. The SRH recombination rate or lifetime can be inferred from device performance by using the above equations when it is known that the carrier lifetimes are SRH-limited, and assuming low-injection and mid-gap traps is equal to,

$$\tau_{SRH} = \frac{1}{A} = \frac{1}{\sigma v_{th} N_t}. \tag{1.4}$$

The basic SRH-driven dark current under forward bias was explained previously in Equation ??, and is related to τ_{SRH} by,

$$J_{02} \approx \frac{qW_D n_i}{2\tau_{SRH}}. \tag{1.5}$$

The cell's voltage depends on the dark current, which from Equation 1.5 is roughly inversely proportional to the SRH lifetime assuming an abrupt junction, low-level injection, and a mid-gap trap.

Chapter 2

Deep-level Transient Spectroscopy

DLTS is a form of defect spectroscopy that is widely used to identify and characterize electrically active defects in a semiconductor. It was pioneered in 1974 by D. V. Lang at Bell Labs [9] and has since been used to electronically identify and characterize the common deep-levels or 'traps' caused by lattice defects in Si, GaAs, and many other semiconductor crystals. It is often used for point defects, but has been applied to boundary and threading defects, as well [10, 11]. Among some of the defects it has characterized are the gold donor and acceptor states in silicon [12], and the defect-donor (Dx) recombination center in AlGaAs [13].

Generally, DLTS has the following requirements material requirements: 1. Sufficient material quality and fabrication ability to create a Schottky or p-n junction diode. 2. The diode depletion region is well-behaved and understood and its width can be modulated by a change in magnitude of the reverse bias. 3. The particular defect concentration is high enough to cause a measurable change in the diode capacitance, typically 10^{-5} times the doping concentration is the minimum [1].

The experimental procedure of DLTS begins with fabrication of a p-n or Schottky diode. DLTS is a measurement of capacitance transients, and the capacitance that is measured is the junction

capacitance. The is the capacitance formed across the junction depletion region as a result of dipole formation across the junction from the ionized dopant atoms. The drift field that forms depletes the region of carriers leading to dielectric-like conductance. The steady-state junction capacitance can be modeled as a parallel plate capacitor,

$$C = \frac{\varepsilon A}{W_d}, \tag{2.1}$$

where C is the junction capacitance, ε is the semiconductor permittivity, and W_d is the depletion width, which for a p-n junction is,

$$W_d = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(V_{bi}-V_a)}. \tag{2.2}$$

In Equation 2.2, q is the elementary charge, N_a is the acceptor density in the p-type semiconductor, N_d is the donor density in the n-type semiconductor, V_bi is the built-in voltage of the junction, and V_a is the applied bias.

From Equations 2.1 and 2.2, it is apparent that the junction capacitance is a function of the applied bias. A change in the applied bias leads to a change in the voltage drop across the junction and a change in the depth of the drift field into the semiconductor on either side of the junction. In DLTS, the junction capacitance is perturbed from steady-state by applying a bias pulse. By switching between one applied bias to another the depletion region will expand or contract. However, the change in depletion width is not instantaneous because the carriers in the region require a finite amount of time to react to the applied potential. While free carriers react too quickly (picoseconds or less) to measure, thermal emission of carriers from deep-level trap states in the depletion region is a much slower process. This slow emission from traps in the depletion region leads to the capacitance transient that is measured by DLTS (see Figure 2.1).

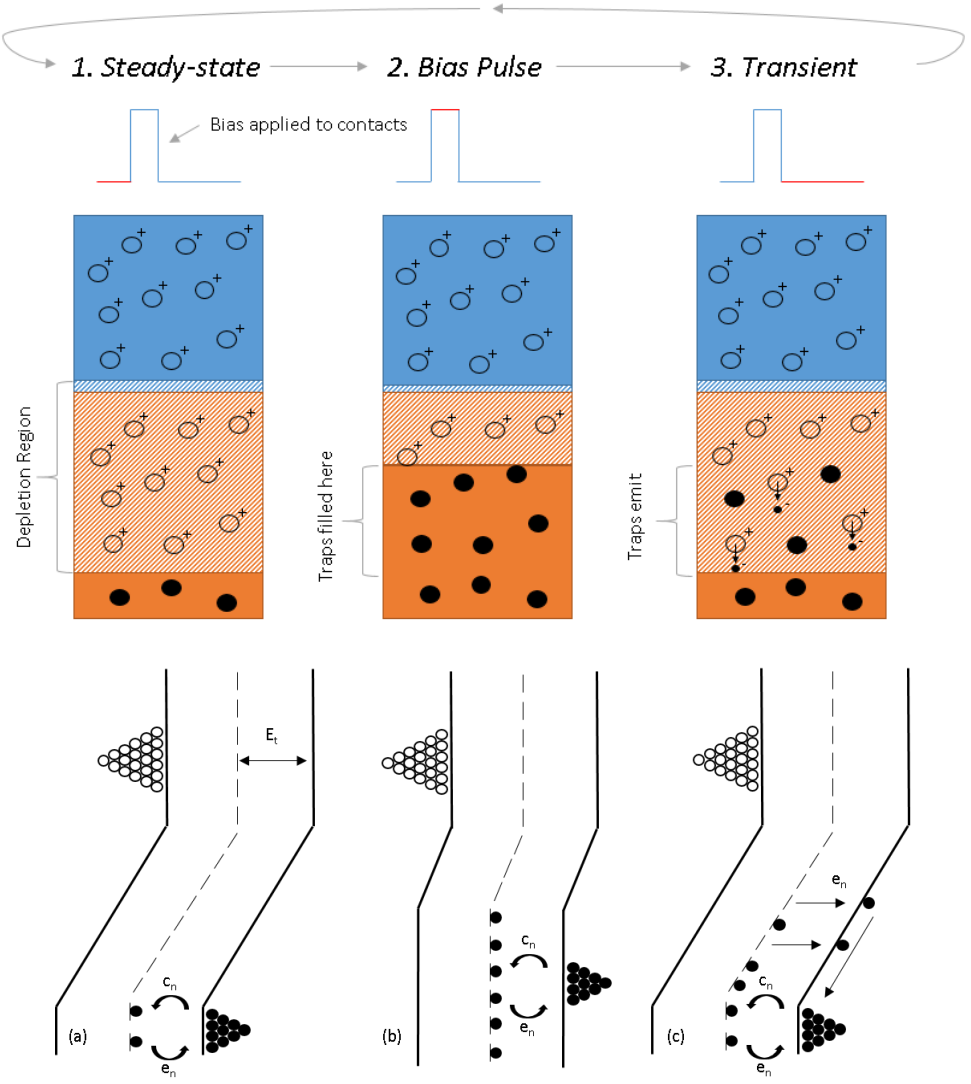

FIGURE 2.1: The three stages of the applied bias and the trap filling/emission behavior during each stage. From left to right: a) Behavior under steady-state reverse bias. b) Voltage pulse allows traps to be filled. c) Pulse ends and filled traps thermally emit carriers causing capacitance transient. From top to bottom: Shape of the voltage pulse applied to the contacts, spatial diagrams of the depletion region and trap behavior, and band diagram representation of the same depletion region and trap behavior.

A general DLTS procedure begins with a Schottky diode or a one-sided p-n diode from the material to be tested. The 'steady-state' reverse bias, V_r, is applied corresponding to the first diagram in Figure 2.1. Next, the voltage pulse is applied such that $V_p > V_r$. The width of the voltage pulse must be long enough in time to allow the deep-levels to trap carriers that have diffused into the previously-depleted region (second diagram of Figure 2.1). Once the traps are filled with carriers, the steady-state reverse bias is restored (the pulse ends) and carriers will

emit from the traps and the drift field will remove them from the depletion region, leading to the measurable transient (third diagram of Figure 2.1). In conventional DLTS, this process is repeated and the capacitance transient is processed as a function of temperature in order to extract the trap parameters of activation energy, capture cross-section, and trap density.

A simple capacitance transient from a single trap level can be modeled using exponential decay,

$$C(t) = C_\infty + \Delta C_0 \exp(-e_n t), \tag{2.3}$$

where C_∞ is the steady-state capacitance and ΔC_0 is the amplitude of the transient. The exponential decay rate here is the carrier emission rate, which for electrons (e_n) and holes (e_p) are,

$$e_n = \sigma_n v_{n,th} N_c \exp -\frac{E_c - E_t}{k_B T}, \tag{2.4a}$$

$$e_p = \sigma_p v_{p,th} N_v \exp -\frac{E_t - E_v}{k_B T}, \tag{2.4b}$$

where N_c and N_v are the density of states in the conduction and valence bands, respectively.

The emission rates in Equation 2.4b can be derived from Fermi statistics for trap occupancy as a function of temperature and the principle of detailed balance. They indicate that emission rate is a function of temperature, and this relationship is taken advantage of in conventional DLTS to extract trap parameters. Rearranging leads to $\ln(T^2/e_n)$ as a linear function of $1000/T$ with activation energy and cross-section determinable from slope and and intercept, respectively,

$$\log\left(\frac{T^2}{e_n}\right) = \frac{E_c - E_t}{1000 K_B}\left(\frac{1000}{T}\right) + \log\left(\frac{1}{\gamma_n \sigma_n}\right), \tag{2.5a}$$

$$\log\left(\frac{T^2}{e_p}\right) = \frac{E_t - E_v}{1000 K_B}\left(\frac{1000}{T}\right) + \log\left(\frac{1}{\gamma_p \sigma_p}\right), \tag{2.5b}$$

where γ is a collection of constants that depend on the effective mass of the carrier and properties of the bandgap. To obtain the slope and intercept, the emission rate at a number of temperatures must be determined. The capacitance meter will output time-series data that should roughly follow the form of Equation 2.3 for a given temperature. This data can be fitted to the model using standard curve fitting, however, if more than one defect is present the model will fail to represent the data accurately. A Laplace transform of the data is a more effective approach, but this is numerically a difficult problem and requires very high signal-to-noise (SNR) ratio. The proven technique, definitive of conventional DLTS, is to use a filter with a weighting function, W,

$$S_{out} = \frac{1}{t_c}\int_{t_d}^{t_d+t_c} W(t,e_n)S_{in}(t)dt \tag{2.6}$$

where t_d is the starting time of the filter and t_c is the duration. Typically, $t_c \approx 2/e_n$ with a fixed ratio of $t_d/t_c \approx 0.05$, though the optimal values change depending on the choice of weighting function [14].

Many DLTS weighting functions have been developed but the one used most in this work is the shifted exponential,

$$W(t,e_n) = \exp\left(\frac{2[t-t_d]}{t_c}\right) + [\exp(-2)-1]/2, \tag{2.7}$$

where W is a function of e_n through the choice of t_c. The main point is that the weighting function in Equation 2.7 is chosen by the experimentalist to have a pre-determined, semi-arbitrary emission rate. This exponential with a known emission rate constant (sometimes 'rate window' is used) is then multiplied by the measured transient data and integrated, as in Equation 2.6, and a maximum S_{out} occurs when the emission rate of the data matches the emission rate constant of the weighting function. To find this maximum, the temperature of the sample is swept to alter the thermal emission rate of the measured data. The DLTS spectra

itself is S_{out} as a function of temperature, where the peaks indicate a known emission rate at a known temperature, and these values are used to create a single data point in the Arrhenius plot of Equation 2.5b. To find more data points to create a line, the same measured data is filtered by more weighting functions of different pre-determined emission rate constants.

Equations in 2.5b assume that there is no temperature-dependence of the capture cross-section, when often this dependence will exist. If the cross-section changes with temperature, the capture cross-section should be determined by other methods, and the extracted activation energy will be a sum of the capture cross section activation energy, ΔE_σ, and the trap activation energy. Nevertheless, the sum is still valid for trap identification and this is the value that is typically reported, even if it may not represent the true trap energy level.

The final trap parameter, N_t, is not found by the Arrhenius plot but by the height of the peaks on the spectrum,

$$\frac{\Delta C_0}{C(\infty)} \approx \frac{N_t}{2N_d}. \tag{2.8}$$

The trap density can be found from the doping, the steady-state capacitance, and the total amplitude of the transient. An assumption made in the derivation of Equation 2.8 was that all traps in the depletion region are filled at $t = 0$ and emit their carriers to become empty at $t = \infty$. This is only valid for a large reverse bias where the depletion width is much larger than the transition region, λ. This region is due to the interaction between E_t, E_F, and band bending. During the bias pulse, there is still some band bending and the traps near the depletion edge are never filled. The never-filled traps are within $x_1 = x_0 - \lambda$ of the junction where x_0 is the depletion width during the pulse. After the pulse is over, the traps near the edge of the depletion layer remain filled as $E_t < E_F$ over the λ region. If W_d is the steady-state depletion width, then traps only emit carriers if they are within $x_2 = W_d - \lambda$ of the junction. Therefore, the trap density must be corrected to be a density over $x_1 < x < x_2$ rather than over W_d.

The corrected trap concentration can be found by introducing a position-dependent charge density to the derivation of Equation 2.8, resulting in,

$$\frac{\Delta C_0}{C(\infty)} = \frac{1}{2}\frac{x_1^2 - x_2^2}{W_d^2}\frac{N_t}{N_d}. \tag{2.9}$$

In summary, DLTS is a technique to detect the electronic properties of small yet numerous point-like defects in a semi-conductor crystal lattice. It requires fabrication of a diode and material quality sufficient to pulse a reverse bias without excessive dark current. The technique is capable of identifying or characterizing majority and minority deep-level states by their activation energy, carrier cross-section, and density.

Chapter 3

Development of MFIA-Based DLTS System

The system used in the previous chapter was an analog conventional DLTS system that was deemed inadequate for the experimental loads planned for this chapter. As an analog spectrometer, the legacy equipment could not digitize the direct capacitance vs. time transients (see Equation 2.3). To obtain spectra, the spectrometer processed transients in analog hardware with dedicated filtering circuits used to implement Equation 2.6. This is the same approach as Lang in the seminal DLTS paper [9]. The old system was equipped with only two of these filtering circuits, so only two emission rate constants could be measured for each sampled transient. To get enough points to fit a line on Arrhenius plot therefore required multiple temperature scans. Each temperature scan typically takes one to several hours, and these required repeat scans are not acceptable when performing *in situ* DLTS as the multiple-scan method can only work well when temperature cycling does not affect the behavior of the sample. The main point of *in situ* DLTS is to find effects that would be hidden by temperature cycling.

A custom DLTS system was developed to overcome these hurdles. The new implementation was designed to digitally capture the capacitance transients. Then, Equation 2.6 could be implemented in software, allowing for an arbitrary number of filters and freedom to design custom filters. This system would also allow other ways of processing the transients in software, such as performing a numerical Laplace transform. It was built around the Zurich Instruments MFIA, a dual-phase digital lock-in amplifier and LCR meter, and driven by software written in MathWorks MATLAB (available in Appendix **??**). The cryostat was an M22 model from Cryo Industries of America, capable of a temperature range of 10 K to over 400 K with cooling from a closed-loop helium recirculator. The system was designed to have have minimal physical switches so that scans could be started, monitored, and altered remotely via remote desktop. A similar system driven by LabVIEW was developed and described in work by Schifano *et al.* [15].

The MFIA lock-in unit has greater capabilities and flexibility when compared to common DLTS capacitance meters such as the popular Boonton models. While the Boontons and similar may only use 1 MHz, the MFIA can modulate a DC bias with frequencies from DC to 5 Mhz in order to measure sample capacitance. The amplitude of the AC wave can also be set arbitrarily on the MFIA versus the limited settings available on most meters. The MFIA can apply DC biases from -10 V to 10 V, which is adequate for DLTS measurements, and can apply the square wave DLTS pulse on its own without an external pulse generator. It can transfer digital samples via ethernet at 107 kHz continuously or higher in bursts, which is more than adequate for good SNR when processing spectra and does not require a separate analog-to-digital converter for data acquisition. Figure 3.1 is a block diagram of all the components in the DLTS setup, with the MFIA combining the three components: Pulse generator, capacitance meter, and data acquisition system.

The sample capacitance can be measured by using a dual-phase lock-in amplifier to analyze the

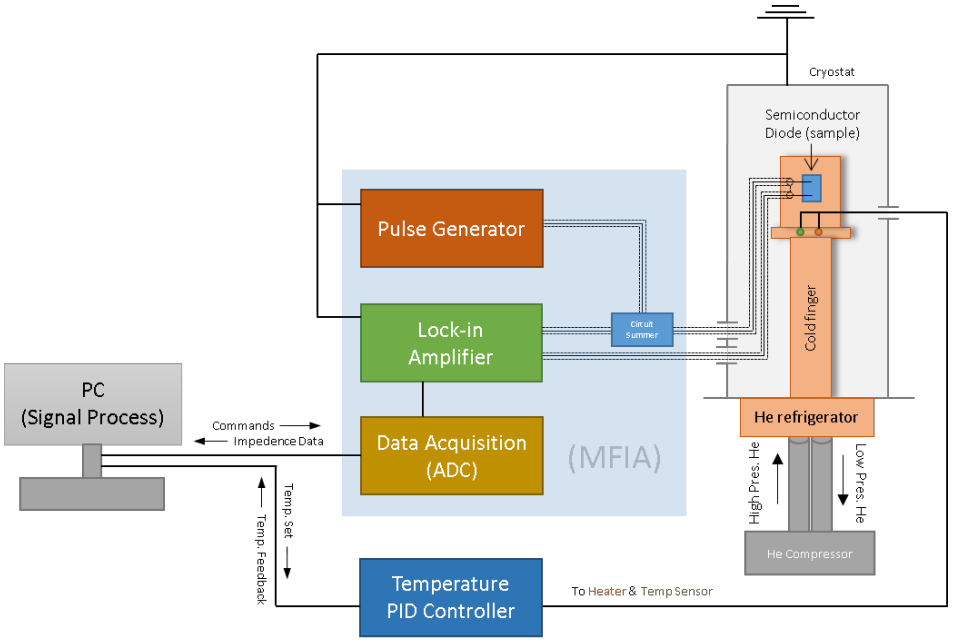

FIGURE 3.1: Block diagram of DLTS system. The use of MFIA simplified the setup without sacrificing features.

complex current response to a reference sinusoidal AC voltage. The sensible circuit representation for the depletion-region capacitor is a resistor in parallel with a capacitor as in Figure 3.2. The complex impedance of a parallel RC circuit is $1/Z = 1/R_p + j2\pi f_{ref} C_p$ and $I = V/Z$, thus,

$$C_p(t) = \frac{I_{\phi=\pi/2}(t)}{2\pi V_{ref} f_{ref}}, \tag{3.1}$$

where $I_{\phi=\pi/2}$ is the component of the current that is 90° out-of-phase with the applied reference AC voltage, and V_{ref} and f_{ref} are the amplitude and frequency of the reference voltage, respectively.

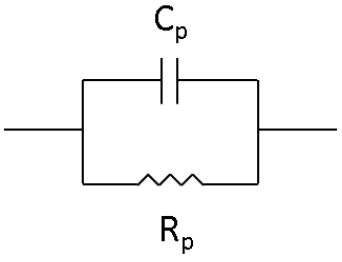

FIGURE 3.2: Parallel RC circuit diagram representative of a diode junction capacitance.

The lock-in can extract the 90°component of the current as it effectively multiplies the measured current signal by a cosine function over some time constant, T, which is at least as large as one period of the reference frequency,

$$I_{out,\phi=\pi/2}(t) = \frac{1}{T}\int_{t-T}^{t} \cos 2\pi f_{ref} s I_{in}(s) ds. \tag{3.2}$$

The principle of the lock-in amplifier is that, because sinusoidal functions are orthogonal, the only component that can be extracted from the filter in Equation 3.2 is the part of I_{in} that has the same frequency and is in-phase with the cosine function, which is 90° out-of-phase with the reference voltage.

The MFIA time constant found to have the best signal extraction without taking too long compared to the transient itself was 2.6 usec with a filter order of 8. The period of a 1 MHz AC signal is 1 usec and the fastest emission rate in DLTS is usually 5 kHz, which is 200 usec.

To test and calibrate the MFIA-based system, DLTS was performed on an irradiated QD GaAs sample. Results for this sample were previously published by collaborators [16], however, the prior results were obtained with a Bio-rad DL8000, which is a commercial DLTS unit. A comparison of the results obtained from the custom MFIA system and the DL8000 are shown in Table 3.1. The DLTS spectra were already shown in Figure **??**. The two DLTS systems were in close agreement for activation energy the cross-section for the two traps listed in the table, indicating that the MFIA-based system was operating as expected. Note that cross-section was found by y-intercept of a log plot and therefore same order of magnitude is an acceptable match.

TABLE 3.1: DLTS results for the irradiated QD GaAs calibration diode.

Defect Label	DLTS System	E_A (eV)	σ (cm^2)
QD-PR4"	Bio-Rad DL8000	$E_C - 0.30$	4×10^{-15}
	Custom MFIA-based	$E_C - 0.31$	8×10^{-15}
QD-PR2	Bio-Rad DL8000	$E_C - 0.67$	5×10^{-13}
	Custom MFIA-based	$E_C - 0.68$	7×10^{-13}

Glossary

DFT density functional theory. 3

DLTS deep-level transient spectroscopy. 5–7, 9–15

EPD etch pit density. 2

MCDL minority carrier diffusion length. 4

QD quantum dot. 15

SIMS secondary ion mass spectrometry. 2

SRH Shockley-Read-Hall. 1, 4, 5

TEM transmission electron microscopy. 2

XRD X-ray diffraction. 3

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