Course Code: ETE 203

Course Title: Electronics Device and Circuit – I

Lab Experiment No: 10

Experiment Name: Common Source JFET Characteristics

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Apparatus:

1. Dual Regulated DC Power supply (0–30 Volts)
2. JFET (BFW11 or equivalent)
3. Resistors (1k □)
4. DC Ammeters (0-100m A)
5. DC Voltmeters (0-30V)
6. Bread Board and connecting wires

Theory:

The full form of JFET is junction-gate field effect transistor. JEFTs are three terminal semiconductor devices named Drain, Gate and Source which are also known as voltage control devices. There are mostly 2 type of JFET one is n-channel JFET and another is p-channel JFET.A JFET is usually "on" when there is no voltage between its gate and source terminals.. By applying a reverse bias voltage to a gate terminal, the channel is "pinched", so that the electric current is impeded or switched off completely. If a potential difference of the proper polarity is applied between its gate and source terminals, the JFET will be more resistive to current flow.

Procedure:

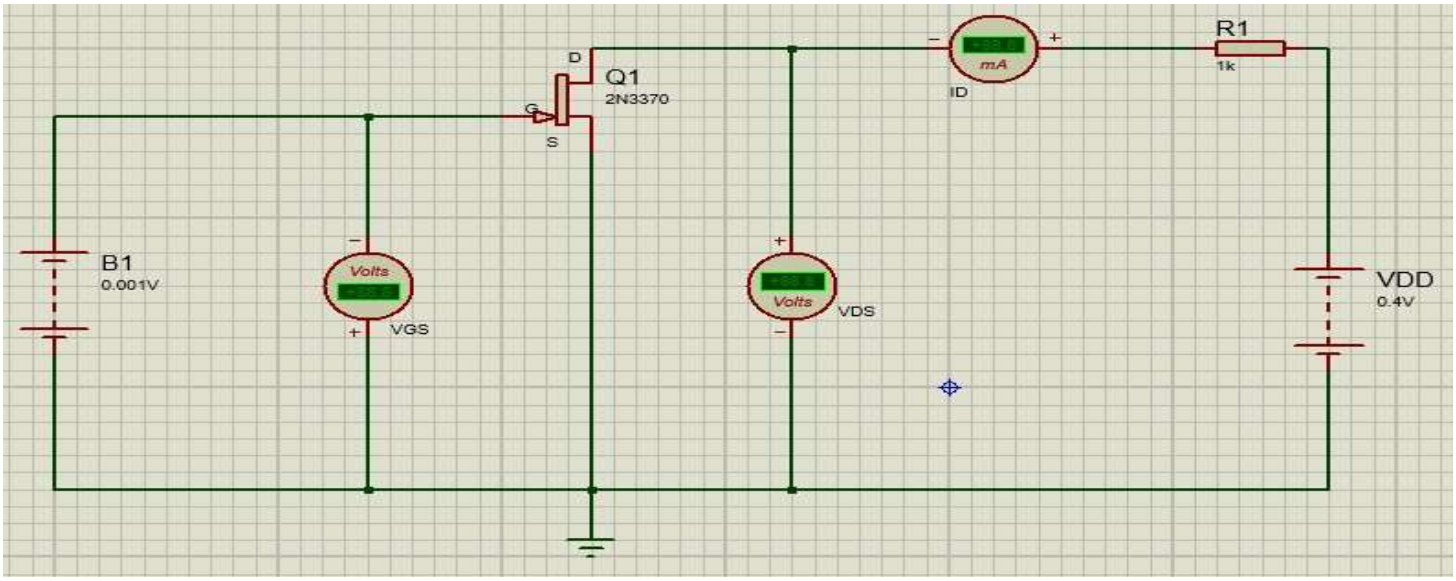
Drain characteristics:

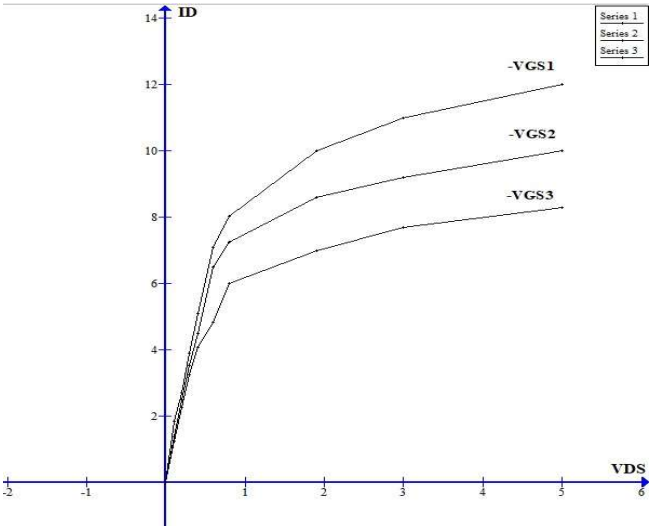
1. First we connect the circuit as shown in the Fig 1.
2. For the drain characteristics we keep VGS=0V by varying VGG.
3. Then varying VDD and recording the reading of VDS and D I in table 1.
4. Repeating the procedure for VGS= -1V and VGS= -2V and record reading in table 1.

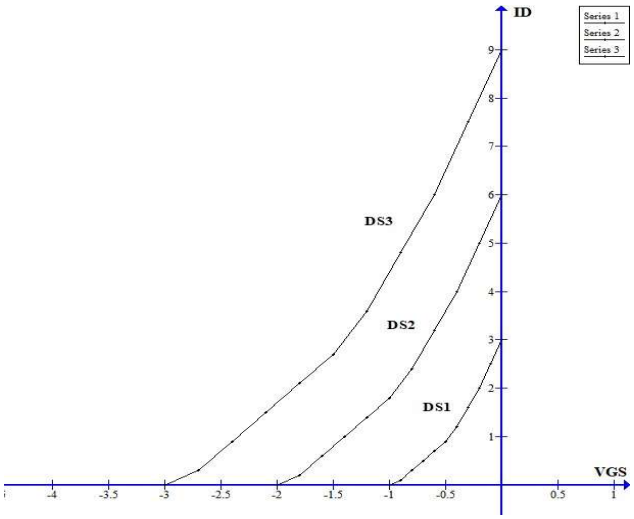
Transfer characteristics:

1. For transfer characteristics we keep VDS=1V.
2. Vary VGG and record reading of VGS and D I in table 2.
3. We repeat the procedure for VDS=1.5V and VDS=2V and record the reading from table 2.

Working Circuit Diagram and graph:







Calculation:

Drain Characteristics

Table: 1

NO.	V_{GS}=0V		V_{GS}=-1V		V_{GS}=-2V	
	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)
1.	0	0	0	0	0	0
2.	0.1	1.85	0.1	1.4	0.1	1.25
3.	0.2	2.7	0.2	2.5	0.2	2.27
4.	0.3	3.9	0.3	3.55	0.3	3.25
5.	0.4	5.09	0.4	4.5	0.4	4.08
6.	0.6	7.1	0.6	6.51	0.6	4.85
7.	0.8	8.03	0.8	7.45	0.8	6.35
8.	1.9	10	1.9	8.6	1.9	6.2
9.	3	11	3	9.2	3	6.8
10.	5	12	5	10	5	7.5

Transfer Characteristics:

Table: 2

NO.	V_{DS}=0.5V		V_{DS}=1V		V_{DS}=1.5V	
	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)
1.	0	6	0	3	0	9
2.	-0.2	5	-0.1	2.5	-0.3	7.5
3.	-0.4	4	-0.2	2	-0.6	6
4.	-0.6	3.2	-0.3	1.6	-0.9	4.8
5.	-0.8	2.4	-0.4	1.2	-1.2	3.6
6.	-1	1.8	-0.5	0.9	-1.5	2.7
7.	-1.2	1.4	-0.6	0.7	-1.8	2.1
8.	-1.4	1	-0.7	0.5	-2.1	1.5
9.	-1.6	0.6	-0.8	0.3	-2.4	0.9
10.	-1.8	0.2	-0.9	0.1	-2.7	0.3

Discussion:

In this experiment we are going to see the characteristics of a junction-gate field effect transistor in a circuit. When current is put through the circuit, variation of ID is seen with increase in VDS. ID increases linearly with increase in VDS till the VDS reaches a value where the saturation effect sets in. The value of VDS where the saturation effect sets in is referred to as the pinch off voltage (at VGS=0). For VDS > VP, JFET has characteristics of a constant current source. It can be further seen that the VGS is the control voltage for JFETs in the same way as the base current (IB) is for BJTs.