Project 1: Cache Simulator Design

Basic implemented features:

Cache Hierarchy:
- L1 Cache
- L2 Cache

Replacement policy implemented:
- LRU
- LFU

Insertion Policy:
- LIP
- MIP

Prefetcher supports:
- No prefetching
- +1 Prefetcher
- Strided Prefetcher

How to build:
- Just used make commands to build and validate my implementation.

Major bugs faced:

- Initially I used a single cache timestamp counter which was giving no errors for some debug outs and raising issues for others.