Md Mizanur Rahaman Nayan

Email: mizanur.rahaman@gatech.edu
Portfolio: mizanur.rahaman.com
Mobile: +1(404)7755668
Github: github.com/Mizanur4E

Education

- **Georgia Institute of Technology (Georgia Tech)** — Georgia, USA
  Ph.D. - Electrical and Computer Engineering — *August 2023 - Present*
- **Bangladesh University of Engineering and Technology (BUET)** — Dhaka, Bangladesh
  B.Sc - Electrical and Electronic Engineering — *February 2017 - May 2022*

Research Interests

Brain-inspired computation, In memory computation, Hardware-software co-design, Very large scale integration (VLSI) in Neural chip design, Non-conventional computing architecture, Applied machine learning, and IoT device design.

Publications

- **"Frequency Tunable CMOS Ring Oscillator Based Ising Machine", IEEE Transaction of Circuits and Systems: I (under review)**: Authors: M. M. R. Nayan and O. Hassan
- **"Parallel Training of TN and ITN Models Through CycleGAN for Improved Sequence to Sequence Learning Performance", APSIPA ASC, 2022**: Authors: M. M. R. Nayan and M. A. Haque
- **"A Deep Ensemble Model with an Efficient Feature for Multi-class Arrhythmia Classification Utilizing 12-Lead ECG Signal", IEEE ICECE, 2022**: Authors: $S.Mahmud^1, M.M.R.Nayan^1, S.Hasan^2, M.N.Taj^2$
- **"Bangla PDF Speaker : A Complete Computer Application to Convert Bangla PDF to Speech", IEEE ACMI, 2021**: Authors: M. M. R. Nayan and M. A. Haque
- **"An IoT Based Real-time Railway Fishplate Monitoring System for Early Warning", IEEE ICECE, 2020**: Authors: $M.M.R.Nayan^1, S.A.Sufi^2, A.K.Abedin^3, R.Ahamed^4$ *and M.F. Hossain*

Industry Experience

- **ACI Center** — MIS Department, ACI Limited, Dhaka, Bangladesh
  Machine Learning Engineer — *July 2022 - August 2023*
- **Cobalt Speech and Language Inc** — Remote
  Machine Learning Research Intern — *October 2021 - January 2022*

Expertise

- **Languages**: Python, Assembly, C, C++, MS SQL, HTML5, Bash
- **Scientific Computing and Mathematical Modeling**: MATLAB, SIMULINK, ANACONDA
- **Engineering Design**: Cadence, HSPICE, PSPICE, Proteus, Quartus, Arduino, MPLAB X IDE, AUTOCAD, VS
- **Machine Learning**: Supervised Learning, GAN Architecture, Natural Language Processing (NLP), Disease Classification
- **Frameworks**: TensorFlow, Keras, PyTorch, Scikit, NLTK, Django
- **Project Management**: Git, GitHub

Selected Academic Projects

- **Configurable Logic Block (CLB) Design**: A Unit block (CLB) of FPGA have been designed using 6T RAM cell, MUX and Buffer, Any expression of A, B, C is possible to implement using the block. The project was completed using Cadence Virtuoso and Cadence Virtuoso layout editor. (For details click here)
- **ASIC Design and Verification (Tic-Tac-Toe Game)**: Through this project complete design and verification (e.g. verilog design, RTL synthesis, verification process through testbench, layout and DRC) of an application specific integrated circuit (ASIC) have been learned. An ASIC is designed to perform Tic-Tac-Toe game using Cadence tools(e.g. Cadence Genus for RTL synthesis, NC SIM and SIM vision for testbench verification and Innovus for layout synthesis.) .(For details click here)
- **Digital Cricket Score Board in Proteus**: The designed device is able to keep track of run, over and wicket. 7490IC has been used as BCD counter for run, over and wicket. Unlike run, over and wicket it is required to develop a mod 6 counter to keep track number of ball. (For details click here)
- **MATLAB Chess Game**: Developed a chess game with GUI interface of MATLAB. Game engine is developed by scripting. Also a feature has been added to the engine to automatically detect check and checkmate in the game. (For details click here)
- **Signal Jammer**: This project aims to design an electronic device that can jam radio signal between a mobile and base station. It simply generates signal with same frequency range as base station does which cause interference and jam the original message signal.
- **4 Bit CPU Design**: Designed with System Verilog. It can perform 16 different instructions. (For details click here)

Honors and Awards

- Dean Listed in Level 1 and Level 4 at BUET
- General Scholarship, Higher Secondary, Rajshahi Board
- Ranked 2 in National Student to Startup, Chapter-1

Affiliation

- **IEEE Member** — BUET Student Branch
  Dhaka, Bangladesh