Md Mizanur Rahaman Nayan

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Education

- **Georgia Institute of Technology (Georgia Tech)** — Georgia, USA
  Ph.D.(Graduate Research Assistant - Electrical and Computer Engineering — *August 2023 - Present*
  - **Neuro Symbolic Macro**: Research on scalable energy-efficient hardware for explainable (Neuro Symbolic) AI
  - **Systolic Array-based HW Accelerator**: Research on exploiting systolic array-based architecture for AI workloads
  - **In Memory Search**: Research on parallel in memory search with emerging magnetic memory devices
- **Georgia Institute of Technology (Georgia Tech)** — Georgia, USA
  MS - Electrical and Computer Engineering — *August 2023 - May 2025*
- **Bangladesh University of Engineering and Technology (BUET)** — Dhaka, Bangladesh
  B.Sc - Electrical and Electronic Engineering — *February 2017 - May 2022*

Industry Experience

- **Nissan North America Inc** — Nissan Advanced Technology Center, Silicon Valley
  AI Hardware Accelerator Research Intern — *May 2025 - Aug 2025*
  - **Summary**: Workload characterization and benchmarking of AV perception model. Designed and FPGA-mapped RISC-V core-based accelerator for AV perception intended for in-car deployment; executed LiDAR/camera ONNX models and generated RISC-V instructions via LLVM; explored sparse convolution accelerator for LiDAR backbone.
- **ACI Limited** — MIS Department, ACI Limited, Dhaka, Bangladesh
  Machine Learning Engineer — *July 2022 - August 2023*
  - **Customer Recognition and Personalized Recommendation Module**: Contributed to the development of the module by enhancing image pre-processing, conducting basket analysis, and creating a recommendation model
  - **REST API with Django for Customer Recognition**: Developed the backend for the customer recognition module to facilitate on-site recommendations by interfacing with the central database
- **Cobalt Speech and Language Inc** — Remote
  Machine Learning Research Intern — *October 2021 - January 2022*
  - **Cycle GAN in Natural Language Processing**: Applied Cycle GAN for text normalization and inverse text normalization, and developed a data-driven framework for text formatting and normalization. Later published the work in APSIPA ASC 2022 Conference, Thailand.
  - **Speaker Diarization**: Contributed to a speaker diarization project by preprocessing voice data for training

Research Experience & Publications

- **"HyDra: SOT-CAM Based Vector Symbolic Macro for Hyperdimensional Computing", [Accepted] International Conference on Computer Aided Design, ICCAD 2025**: Authors: M. M. R. Nayan, C. K. Liu, Z. Wan, A. Raychowdhury, A. Naeemi
- **"Axon: A novel systolic array architecture for improved run time and energy efficient GeMM and Conv operation with on-chip im2col", Design, Automation & Test in Europe Conference, DATE 2025**: Authors: M. M. R. Nayan, R. Raj, G. B. Shaik, T. Krishna, A. Naeemi
- **"Frequency Tunable CMOS Ring Oscillator Based Ising Machine", International Journal of Circuit Theory and Applications, 2024**: Authors: M. M. R. Nayan and O. Hassan
- **"Parallel Training of TN and ITN Models Through CycleGAN for Improved Sequence to Sequence Learning Performance", APSIPA ASC, 2022**: Authors: M. M. R. Nayan and M. A. Haque
- **"A Deep Ensemble Model with an Efficient Feature for Multi-class Arrhythmia Classification Utilizing 12-Lead ECG Signal", IEEE ICECE, 2022**: Authors: $S.Mahmud^1, M.M.R.Nayan^1, S.Hasan^2, M.N.Taj^2$
- **"An IoT Based Real-time Railway Fishplate Monitoring System for Early Warning", IEEE ICECE, 2020**: Authors: $M.M.R.Nayan^1, S.A.Sufi^2, A.K.Abedin^3, R.Ahamed^4$ *and M.F. Hossain*
- **"Bangla PDF Speaker: A Complete Computer Application to Convert Bangla PDF to Speech", IEEE ACMI, 2021**: Authors: $M.M.R.Nayan, M.A.Haque$

Relevant Coursework

- ECE 6100: Advanced Computer Architecture
- CS 6122: Advanced Programming Technique
- ECE 6130: Advanced VLSI Systems
- CS 8803: Hardware Software Co Design for ML
- CS 7641: Machine Learning
- EEE 515: Microprocessors and Embedded Systems
- EEE 453: VLSI Circuits and Design I
- EEE 457: VLSI Circuits and Design II
- EEE 455: Compound Semiconductor Devices
- EEE 313: Solid State Devices

Research Interests

Compute in Memory, Emerging memory devices, Unconventional computing, Hardware-software co-design for ML, Very-large-scale integration (VLSI), Applied machine learning (ML), and IoT device design.

Honors and Awards

- Center for Research into Novel Compute Hierarchies(CRNCH) Ph.D. Fellowship, 2024
- Silicon Creations Grant for ISSCC 2024
- Georgia Tech ECE Fellowship, 2023
- Dean Listed in Level 1 and Level 4 at BUET
- Ranked 2 in National Student to Startup, Chapter-1

Expertise

- **Languages**: Python, C, C++, Verilog, Assembly, MS SQL, HTML5, Bash
- **Scientific Computing and Mathematical Modeling**: MATLAB, SIMULINK, ANACONDA
- **Engineering Design**: Cadence, HSPICE, Proteus, Quartus, Arduino, MPLAB X IDE
- **Machine Learning**: Supervised and Unsupervised Learning, Generative Learning, Natural Language Processing (NLP)
- **Frameworks**: TensorFlow, PyTorch, Scikit, NLTK, Django
- **Project Management**: Git, GitHub

Affiliation

- **Research scholar**
  Semiconductor Research Corporation *August 2023 - Present*
- **IEEE Member**
  Atlanta Section *November 2023 - Present*

Relevant Academic Projects

- **Superscalar Processor Design**: Implemented branch predictor and out-of-order processor according to Tomasulo algorithm. We developed always taken, smith counter, Yeh-Patt, Gshare methods for branch predictor.
- **Cache and Cache Coherence Simulator**: Built a simulator with a write-back, write-allocate L1 cache, and a write through, write-no-allocate L2 cache. Implemented a prefetcher in the L2 cache. For cache coherence, implemented the agent and directory controllers for some cache coherence protocols on a multiprocessor.
- **Convolution accelerator with on-the-fly im2col v2 in Verilog HDL**: We have reproduced a paper where they have implemented two solutions to address challenges during mapping convolution operation in hardware accelerator. Firstly, using an on-the-fly im2col to convert the convolution data into matrices for GeMM. Secondly, using a data-feeder that supports dilated convolutions to save memory as well as area.
- **6T SRAM Cell Design and Write-ability Test**: We looked at the "write-ability" of 6T SRAM cell using 14nm PTM model of MOSFET. We used the Cadence tool for conducting the analysis.
- **Configurable Logic Block (CLB) Design**: A Unit block (CLB) of FPGA have been designed using 6T SRAM cell, MUX and Buffer, Any expression of A, B, C is possible to implement using the block. The project was completed using Cadence Virtuoso and Cadence Virtuoso layout editor. (For details click here)
- **ASIC Design and Verification (Tic-Tac-Toe Game)**: Through this project complete design and verification (e.g. verilog design, RTL synthesis, verification process through testbench, layout and DRC) of an application specific integrated circuit (ASIC) have been learned. An ASIC is designed to perform Tic-Tac-Toe game using Cadence tools(e.g. Cadence Genus for RTL synthesis, NC SIM and SIM vision for testbench verification and Innovus for layout synthesis.) .(For details click here)
- **3D Animated Scene**: Developed a C++ application using custom classes, OpenGL, and ASSIMP to load and animate 3D objects. Objects remain stationary until activated, then move and rotate randomly, with separate threads handling each object's motion. They collide, bounce, and stay within a central space, with support for custom 3D objects.
- **TCP Server and Client**: Implemented a TCP server and TCP client application that can be used to receive and send messages from multiple clients
- **Digital Cricket Score Board in Proteus**: The designed device is able to keep track of run, over and wicket. 7490IC has been used as BCD counter for run, over and wicket. Unlike run, over and wicket it is required to develop a mod 6 counter to keep track number of ball. (For details click here)
- **MATLAB Chess Game**: Developed a chess game with GUI interface of MATLAB. Game engine is developed by scripting. Also a feature has been added to the engine to automatically detect check and checkmate in the game. (For details click here)
- **Signal Jammer**: This project aims to design an electronic device that can jam radio signal between a mobile and base station. It simply generates signal with same frequency range as base station does which cause interference and jam the original message signal.
- **4 Bit CPU Design**: Designed with System Verilog. It can perform 16 different instructions. (For details click here)