Team Name: Reggit

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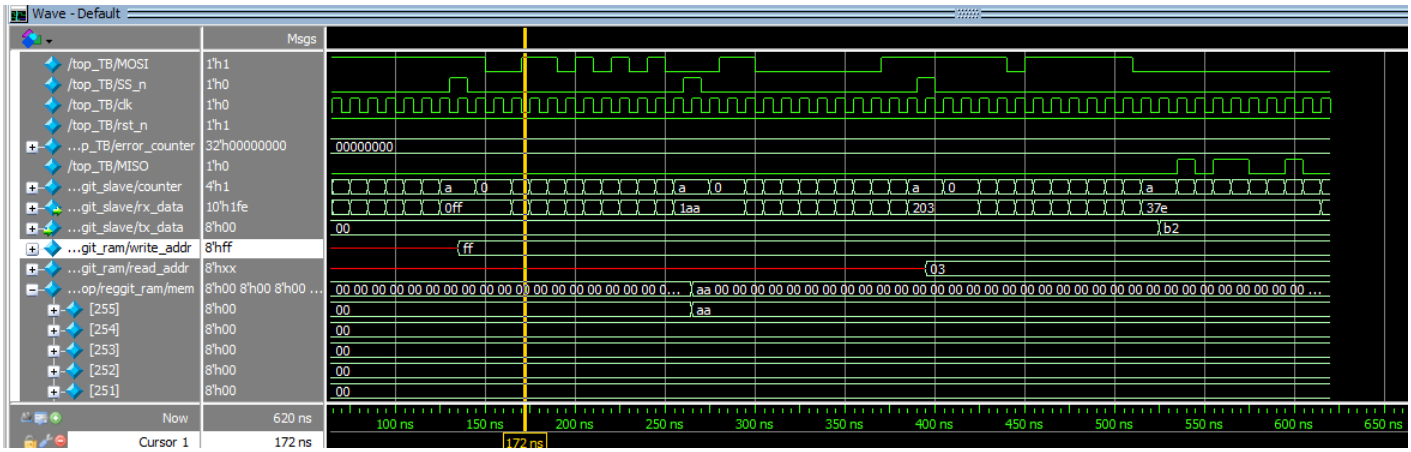
1) Snippets from the waveforms captured from QuestaSim for the design with inputs assigned values and output values visible:



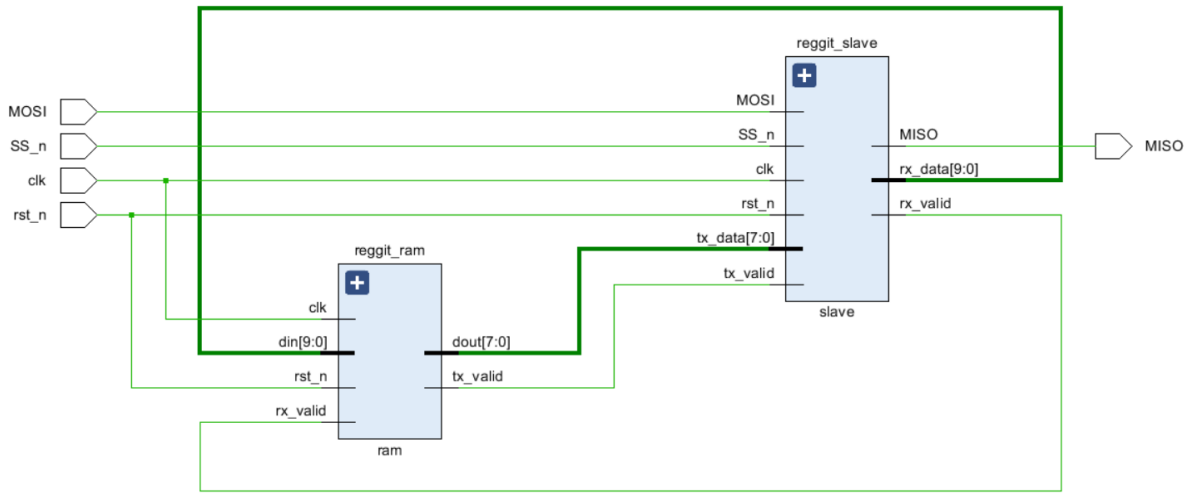

```
VSIM 37> run -all
# Congrates every thing worked as expected
# ** Note: $stop    : top_TB.v(97)
#    Time: 620 ns  Iteration: 1  Instance: /top_TB
# Break in Module top_TB at top_TB.v line 97
```

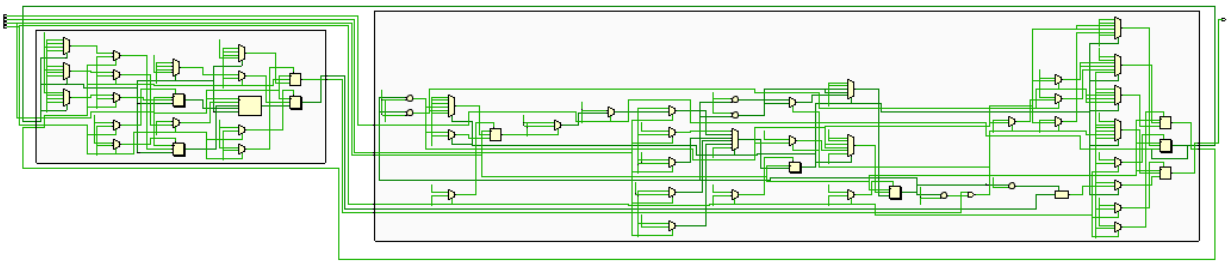
2) Synthesis snippets for each encoding

-Gray encoding.

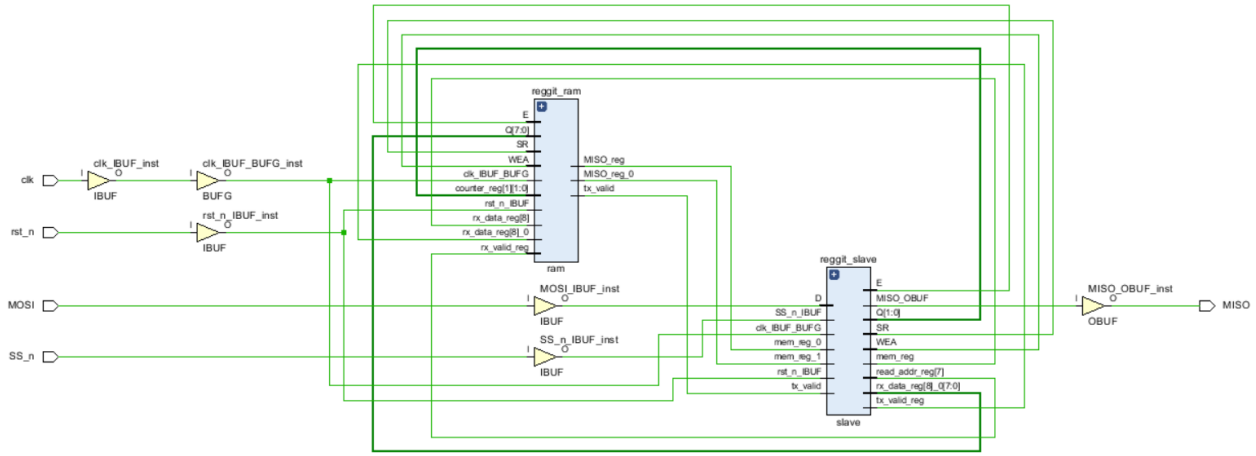
• Schematic after the elaboration & synthesis

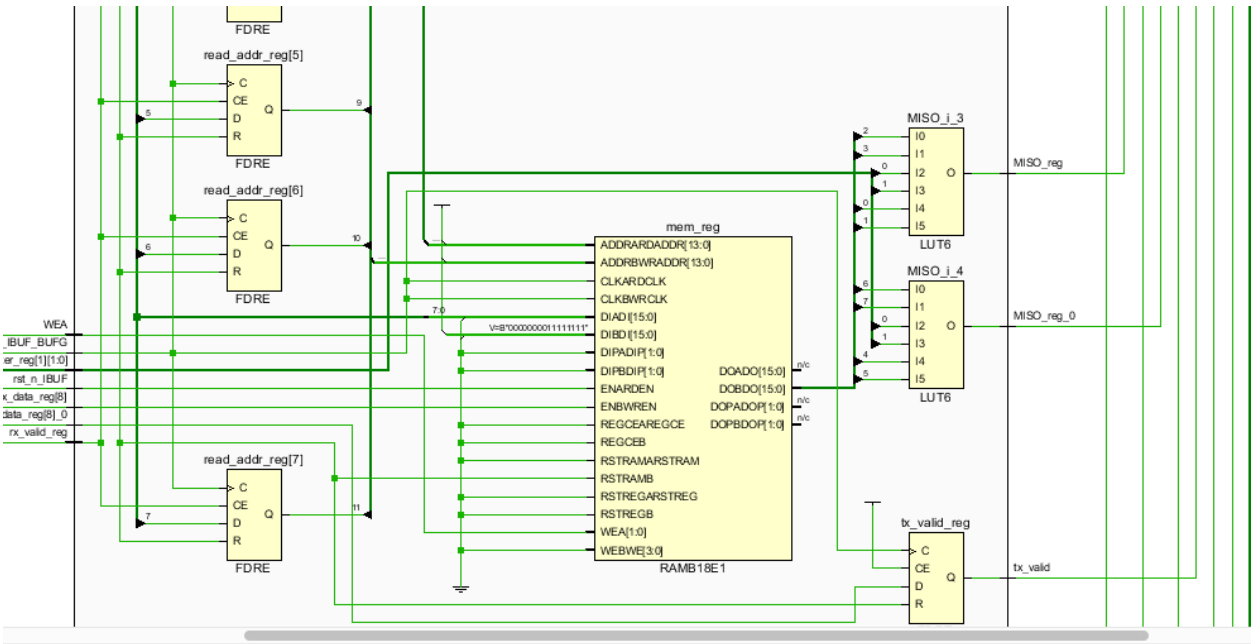
-Elaboration:

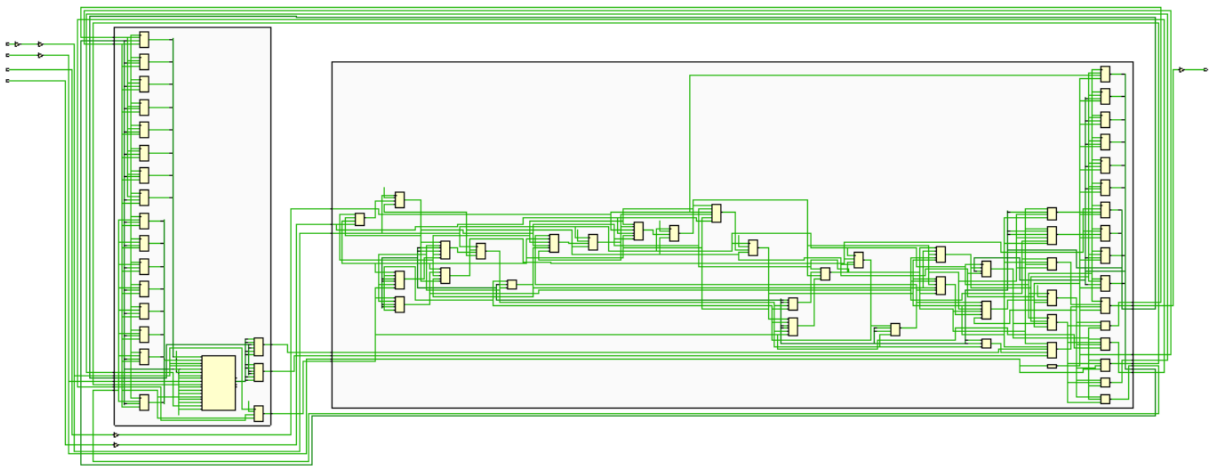




-Synthesis:


reggit_ram
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
rst_n
rst_n_IBUF_inst
IBUF
MOSI
MOSI_IBUF_inst
IBUF
SS_n
SS_n_IBUF_inst
IBUF
E
Q[7:0]
SR
WEA
clk_IBUF_BUFG
counter_reg[1][1:0]
rst_n_IBUF
rx_data_reg[8]
rx_data_reg[8]_0
rx_valid_reg
MISO_reg
MISO_reg_0
tx_valid
ram
reggit_slave
D
SS_n_IBUF
clk_IBUF_BUFG
mem_reg_0
mem_reg_1
rst_n_IBUF
tx_valid
E
MISO_OBUF
Q[1:0]
SR
WEA
mem_reg
read_addr_reg[7]
rx_data_reg[8]_0[7:0]
tx_valid_reg
slave
MISO_OBUF_inst
OBUF
MISO


FDRE
read_addr_reg[5]
FDRE
read_addr_reg[6]
FDRE
read_addr_reg[7]
FDRE
WEA
IBUF_BUFG
er_reg[1][1:0]
rst_n_IBUF
k_data_reg[8]
data_reg[8]_0
rx_valid_reg
mem_reg
ADDRARDADDR[13:0]
ADDRBWRADDR[13:0]
CLKARDCLK
CLKBWRCLK
DIADI[15:0]
DIBDI[15:0]
DIPADIP[1:0]
DIPBDIP[1:0]
ENARDEN
ENBWREN
REGCEAREGCE
REGCEB
RSTRAMARSTRAM
RSTRAMB
RSTREGARSTREG
RSTREGB
WEA[1:0]
WEBWE[3:0]
DOADO[15:0]
DOBDO[15:0]
DOPADOP[1:0]
DOPBDOP[1:0]
RAMB18E1
MISO_i_3
LUT6
MISO_i_4
LUT6
MISO_reg
MISO_reg_0
tx_valid_reg
tx_valid

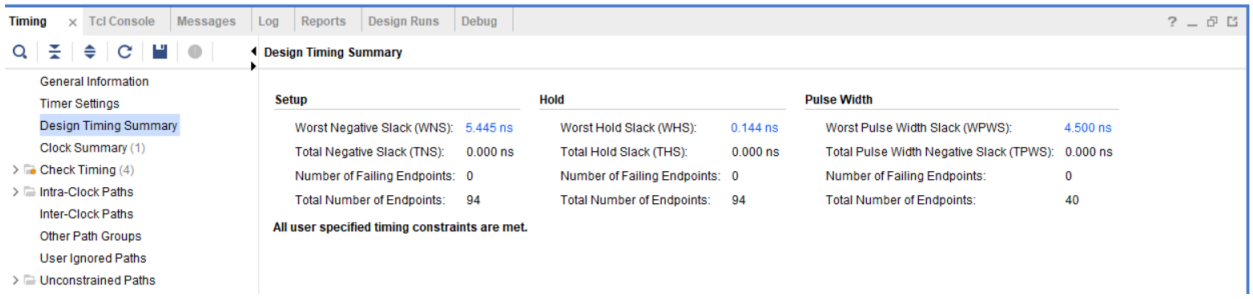


• Synthesis report showing the encoding used (gray):

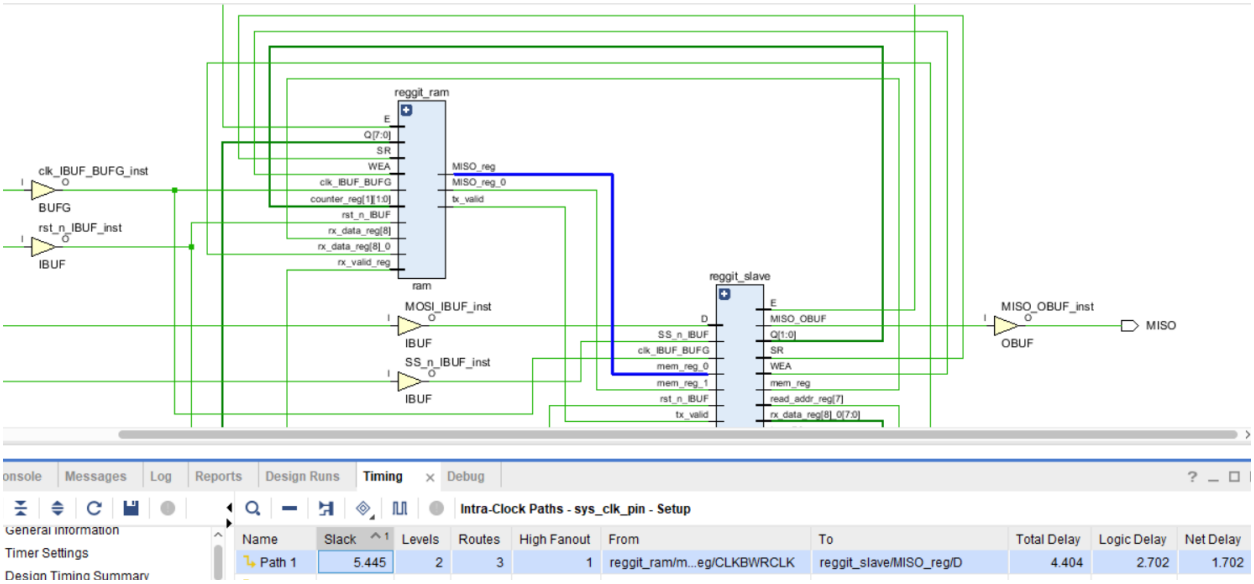
State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	100
READ_DATA	111	011

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'slave'

• Timing report snippet (gray):



• Snippet of the critical path highlighted in the schematic: (gray)



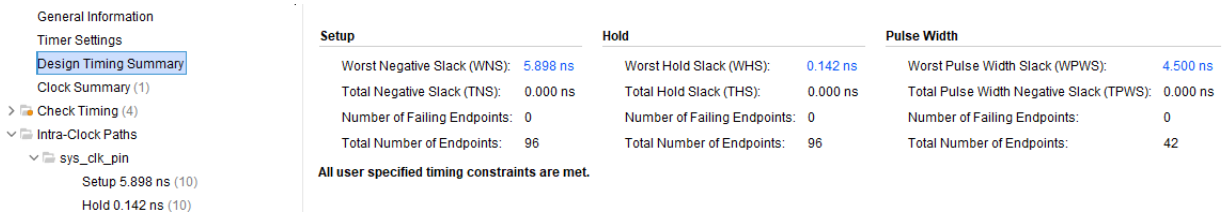
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	5.445	2	3	1	reggit_ram/m...eg/CLKBWRCLK	reggit_slave/MISO_reg/D	4.404	2.702	1.702

Synthesis report showing the encoding used (one_hot):

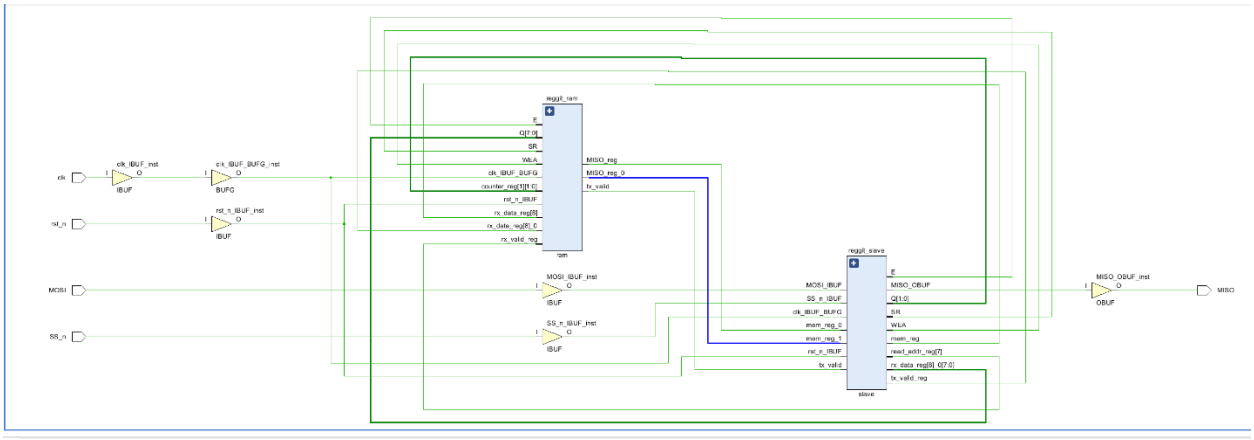
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	100
READ_DATA	10000	011

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'slave'
```

Timing report snippet (one_hot):



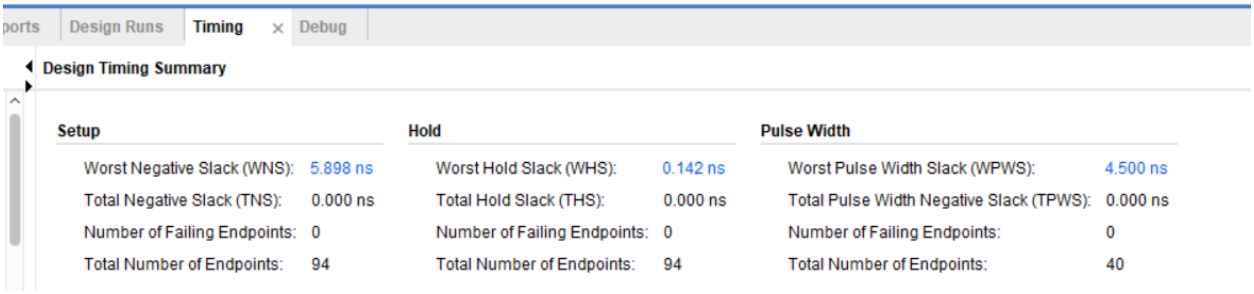
Snippet of the critical path highlighted in the schematic (one_hot):



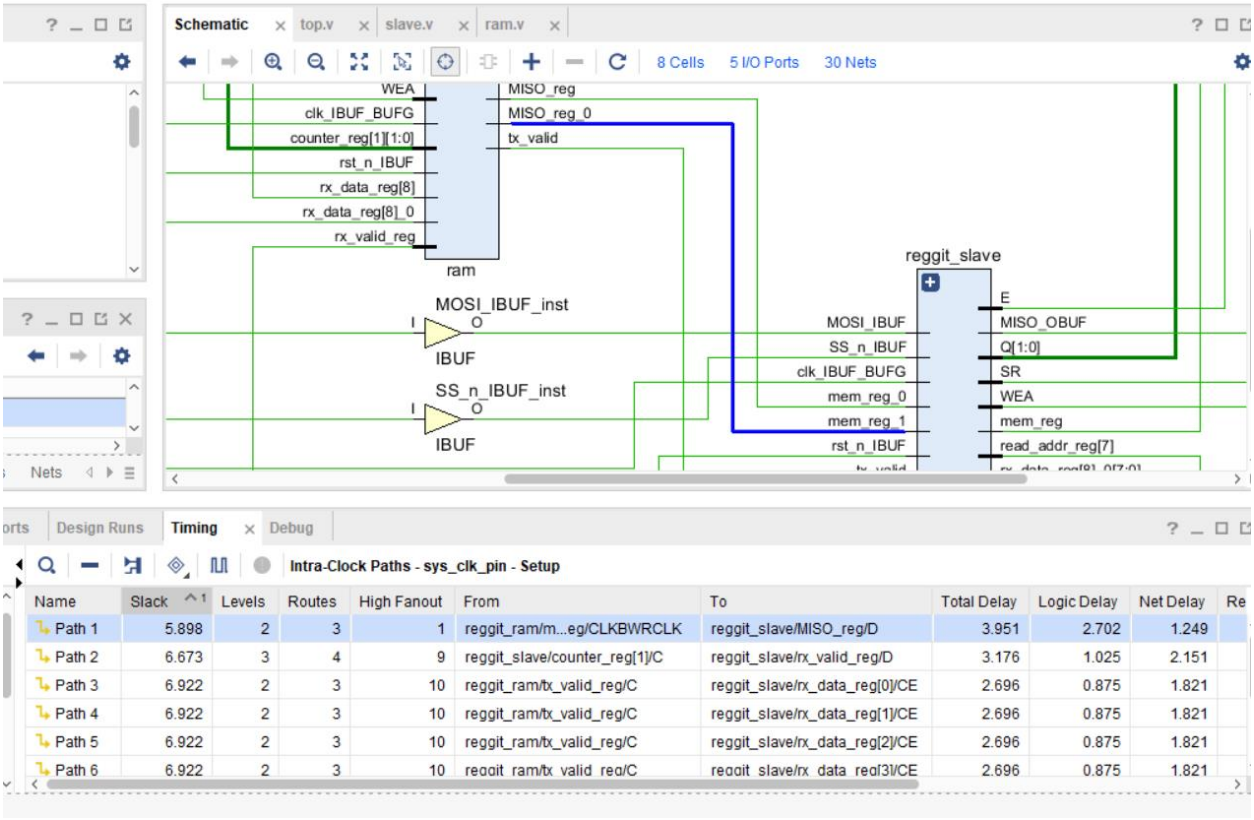
Synthesis report showing the encoding used (sequential):

```
-----------------------------------------------------------------------------------------------------
                State |                     New Encoding |                Previous Encoding
-----------------------------------------------------------------------------------------------------
                 IDLE |                              000 |                             000
              CHK_CMD |                              001 |                             001
                WRITE |                              010 |                             010
             READ_ADD |                              011 |                             100
            READ_DATA |                              100 |                             011
-----------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'slave'
-----------------------------------------------------------------------------
```

Timing report snippet (sequential):



Snippet of the critical path highlighted in the schematic (sequential):



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Re
Path 1	5.898	2	3	1	reggit_ram/m...eg/CLKBWRCLK	reggit_slave/MISO_reg/D	3.951	2.702	1.249	
Path 2	6.673	3	4	9	reggit_slave/counter_reg[1]/C	reggit_slave/rx_valid_reg/D	3.176	1.025	2.151	
Path 3	6.922	2	3	10	reggit_ram/tx_valid_reg/C	reggit_slave/rx_data_reg[0]/CE	2.696	0.875	1.821	
Path 4	6.922	2	3	10	reggit_ram/tx_valid_reg/C	reggit_slave/rx_data_reg[1]/CE	2.696	0.875	1.821	
Path 5	6.922	2	3	10	reggit_ram/tx_valid_reg/C	reggit_slave/rx_data_reg[2]/CE	2.696	0.875	1.821	
Path 6	6.922	2	3	10	reggit_ram/tx_valid_reg/C	reggit_slave/rx_data_reg[3]/CE	2.696	0.875	1.821	

3) Implementation snippets for each encoding

1)gray encoding

- Utilization report:

Reports | Design Runs | Power | Methodology | Timing | **Utilization**

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
top	27	37	15	27	11	0.5	5	1
reggit_ram (ram)	3	17	5	3	0	0.5	0	0
reggit_slave (slave)	24	20	11	24	10	0	0	0

- Timing report snippet:

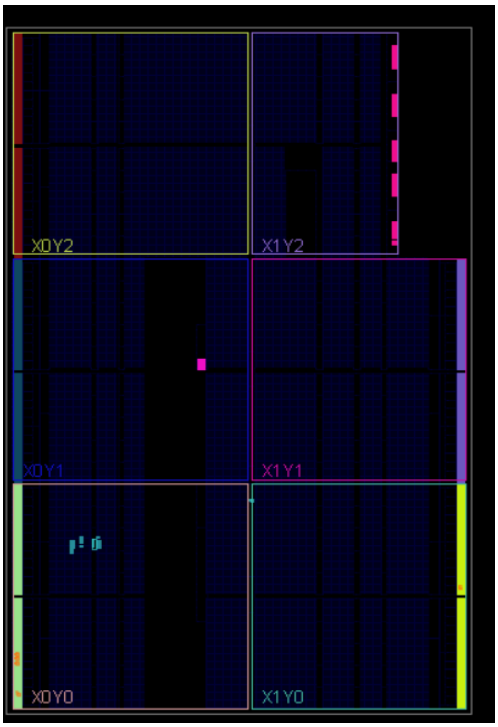
rts | Design Runs | Power | Methodology | **Timing** | Utilization

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.327 ns	Worst Hold Slack (WHS):	0.042 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	40

All user specified timing constraints are met.

- FPGA device snippet:



3) Implementation snippets for each encoding

1) one hot encoding

- Utilization report:

Reports | Design Runs | Power | Methodology | Timing | **Utilization** ×

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N top	28	39	13	28	14	0.5	5	1
reggit_ram (ram)	3	17	5	3	0	0.5	0	0
reggit_slave (slave)	25	22	10	25	13	0	0	0

- Timing report snippet:

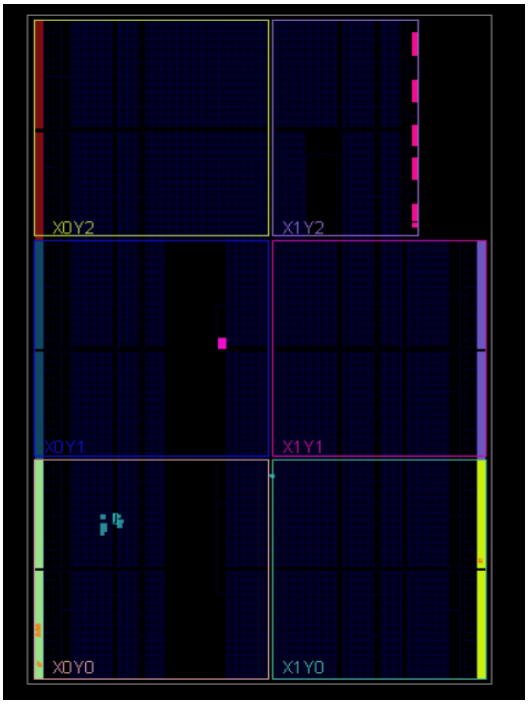
ports | Design Runs | Power | Methodology | **Timing** × | Utilization

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.675 ns	Worst Hold Slack (WHS):	0.054 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	97	Total Number of Endpoints:	97	Total Number of Endpoints:	42

All user specified timing constraints are met.

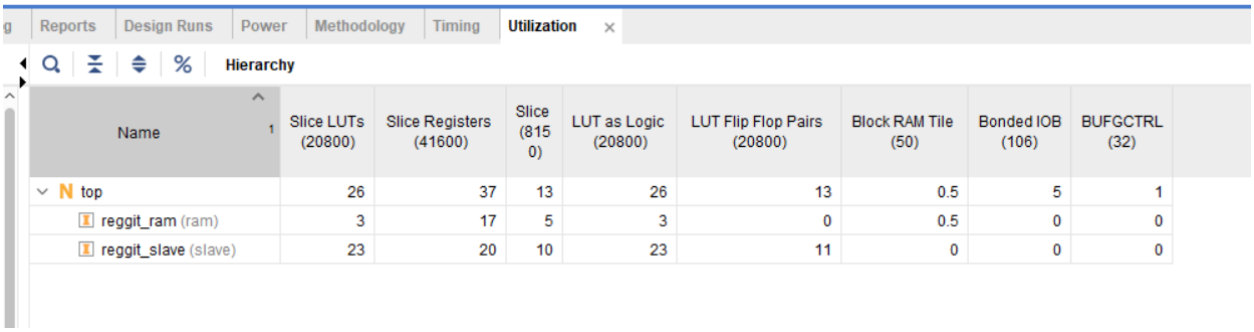
- FPGA device snippet:



3) Implementation snippets for each encoding

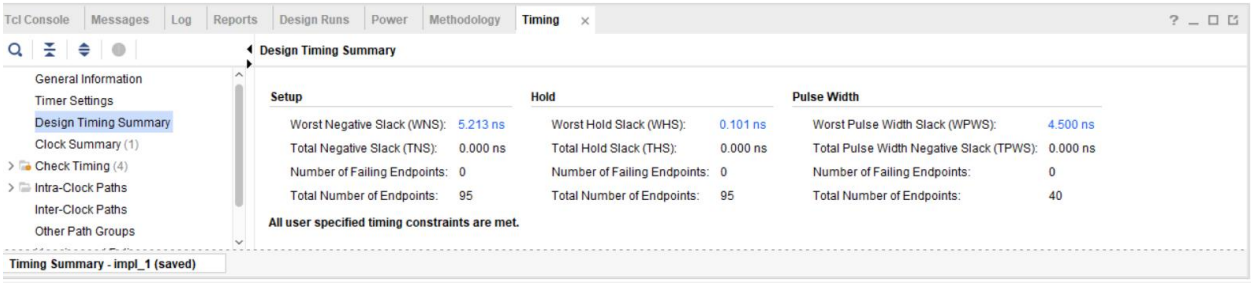
1) seq encoding

• Utilization report:

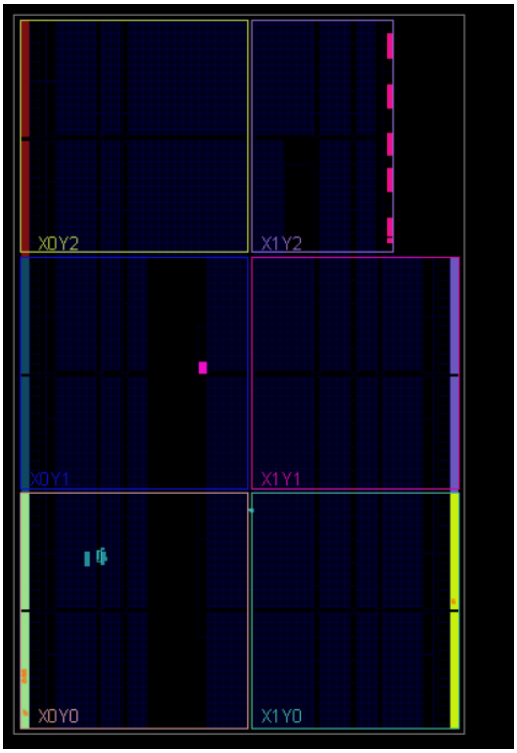


Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N top	26	37	13	26	13	0.5	5	1
reggit_ram (ram)	3	17	5	3	0	0.5	0	0
reggit_slave (slave)	23	20	10	23	11	0	0	0

• Timing report snippet:



• FPGA device snippet:



❖ Conclusion:

- The best encoding is one hot.

4) Snippet of the “Messages” tab showing no critical warnings or errors after running elaboration, synthesis, implementation and a successful bitstream generation.