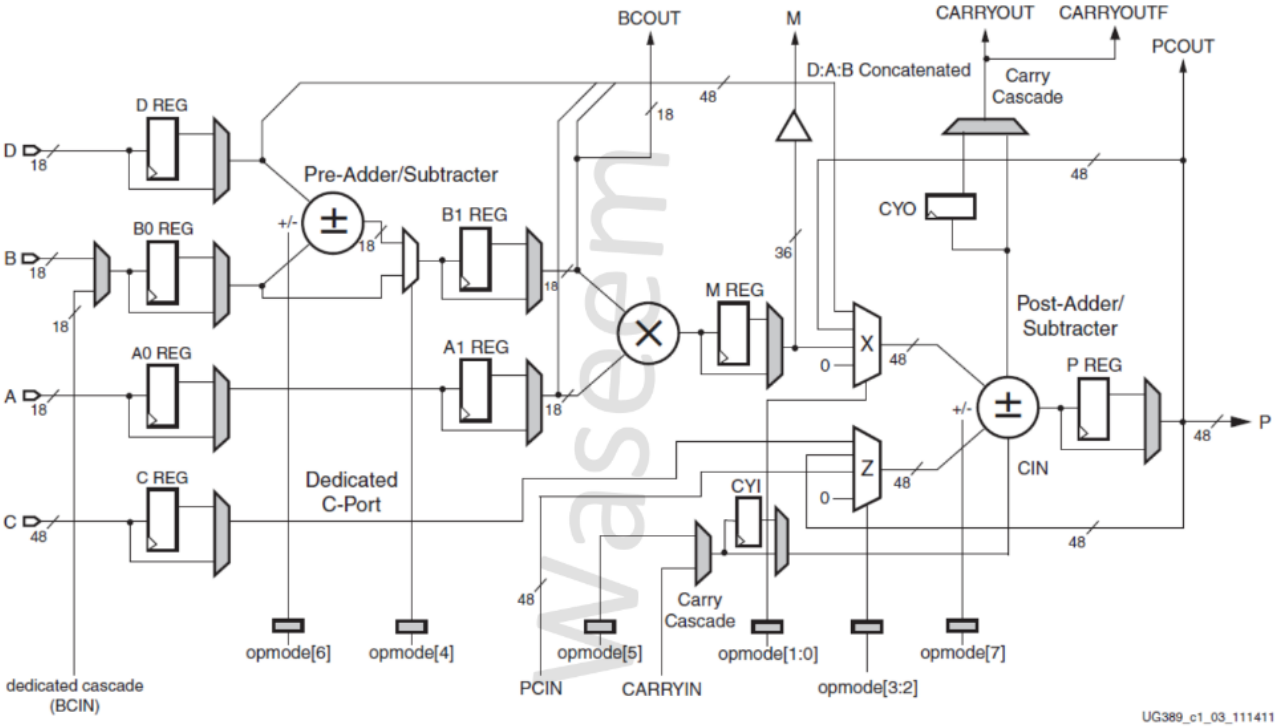
Project 1: DSP

REGGIT



Waseem

DIGITAL DESIGN ENGINEER:
Mohamed Khaled Ahmed

RTL Code:

```
module sel_reg(D,clk,E,rst,out);
parameter size=18;
parameter z=1;
parameter RSTTYPE="SYNC";
input [size-1:0] D;
input clk,rst,E;
output [size-1:0]out;
reg [size-1:0]temp;
generate
    if (z) begin
        if(RSTTYPE=="SYNC")begin
            always @(posedge clk ) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        else begin
            always @(posedge clk or posedge rst) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        assign out = temp;
    end
    else assign out=D;
endgenerate
endmodule
```

```
module DSP48A1(A,B,Bcin,C,D,carryin,M,P,carryout,
carryoutF,clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode
,ceP,rstA,rstB,rstC,rstcarryin,rstD,rstM,rstopmode,rstP,Bcout,Pcin,Pcout);
```

```
//parameters
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL ="OPMODE5";
parameter B_INPUT ="DIRECT";
parameter RSTTYPE ="SYNC";
```

```
//inputs
input [17:0]A,B,D;
input [47:0]C,Pcin;
input [17:0]Bcin;
input clk,carryin;
input [7:0]opmode;
input rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
input ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;
```

```
//outputs
output [17:0]Bcout;
output [47:0]Pcout,P;
output [35:0]M;
output carryout,carryoutF;
```

```
//wires
wire [17:0]Bmux_out;
wire [17:0]A0REG_out,B0REG_out,DREG_out,A1REG_out,adder1,adder1_mux_out,B1REG_out;
wire [47:0]CREG_out,PREG_out;
wire [35:0]multiply_out,MREG_out,M_buff;
wire carryin_MUX_out,CIN;
wire [7:0] opmode_reg_out;
wire [47:0]DAB_conc;
wire [47:0]Xmux_out,Zmux_out,adder2_out;
```

```
//reg
reg [47:0]reg_X_temp,reg_Z_temp;

//_____________________________________________________________
// verilog design
//_____________________________________________________________

assign Bmux_out=(B_INPUT =="DIRECT")? B :(B_INPUT =="CASCADE")? Bcin:0;

sel_reg #(18,A0REG,RSTTYPE) _A0REG(A,clk,ceA,rstA,A0REG_out);//A0REG
sel_reg #(18,A1REG,RSTTYPE) _A1REG(A0REG_out,clk,ceA,rstA,A1REG_out);//A1REG
sel_reg #(18,B0REG,RSTTYPE) _B0REG(Bmux_out,clk,ceB,rstB,B0REG_out);//B0REG
sel_reg #(48,CREG,RSTTYPE) _CREG (C,clk,ceC,rstC,CREG_out);//CREG
sel_reg #(18,DREG,RSTTYPE) _DREG (D,clk,ceD,rstD,DREG_out);//DREG
sel_reg #(8,OPMODEREG,RSTTYPE) _OPMODEREG(opmode,clk,ceopmode,rstopmode,opmode_reg_out);//opcodereg

assign adder1=(opmode_reg_out[6])? (DREG_out-B0REG_out) : (DREG_out+B0REG_out);//first adder
assign adder1_mux_out=(opmode_reg_out[4])? adder1 : B0REG_out;

sel_reg #(18,B1REG,RSTTYPE) _B1REG(adder1_mux_out,clk,ceB,rstB,B1REG_out); //B1REG

assign Bcout=B1REG_out;

assign multiply_out=A1REG_out*B1REG_out;

sel_reg #(36,MREG,RSTTYPE) _MREG (multiply_out,clk,ceM,rstM,MREG_out);//MREG
assign M_buff=MREG_out;
assign M=M_buff;
assign carryin_MUX_out=(CARRYINSEL =="OPMODE5")? opmode_reg_out[5]:(CARRYINSEL =="CARRYIN")? carryin : 0;

sel_reg #(1,CARRYINREG,RSTTYPE) _CYI(carryin_MUX_out,clk,cecarryin,rstcarryin,CIN);
//                                                          Xmux
```

```
//_____________________________________________________________Xmux
always @(*) begin
    case (opmode_reg_out[1:0])
        0:reg_X_temp=0;
        1:reg_X_temp={12'b0,MREG_out};
        2:reg_X_temp=Pcout;
        3:reg_X_temp=DAB_conc;
    endcase
end
assign DAB_conc={DREG_out[11:0],A1REG_out,B1REG_out};
assign Xmux_out=reg_X_temp;
//_____________________________________________________________Zmux
always @(*) begin
    case (opmode_reg_out[3:2])
        0:reg_Z_temp=0;
        1:reg_Z_temp=Pcin;
        2:reg_Z_temp=Pcout;
        3:reg_Z_temp=CREG_out;
    endcase
end
assign Zmux_out=reg_Z_temp;
assign {carry,adder2_out}=(opmode_reg_out[7])?(Zmux_out-(Xmux_out+carryin)):(Zmux_out+Xmux_out+carryin);

sel_reg #(48,PREG,RSTTYPE) _PREG (adder2_out,clk,ceP,rstP,P);

assign Pcout=P;

sel_reg #(1,CARRYOUTREG,RSTTYPE) _CARRYOUTREG (carry,clk,cecarryin,rstcarryin,carryout);
assign carryoutF=carryout;
assign Pcout=P;
endmodule
```

Testbench Code:

```
module DSP_TB();
reg [17:0]A,B,D;
reg [47:0]C,Pcin;
reg [17:0]Bcin;
reg clk,carryin;
reg [7:0]opmode;
reg rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
reg ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;



wire [17:0]Bcout_dut;
wire [47:0]Pcout_dut,P_dut;
wire [35:0]M_dut;
wire carryout_dut,carryoutF_dut;


DSP48A1 dut(A,B,Bcin,C,D,carryin,M_dut,P_dut,carryout_dut,carryoutF_dut,
            clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode,ceP,rstA,
            rstB,rstC,rstcarryin,rstD,rstM,rstopmode
            ,rstP,Bcout_dut,Pcin,Pcout_dut);

initial begin
    clk=0;
    forever begin
        #5;
        clk=~clk;
    end
end
```

```
initial begin
    rstA=1;
    rstB=1;
    rstM=1;
    rstP=1;
    rstC=1;
    rstD=1;
    rstcarryin=1;
    rstopmode=1;
    repeat(50)begin
        ceA=$random;
        ceB=$random;
        ceM=$random;
        ceP=$random;
        ceC=$random;
        ceD=$random;
        cecarryin=$random;
        ceopmode=$random;
        A=$random;
        B=$random;
        D=$random;
        C=$random;
        Pcin=$random;
        Bcin=$random;
        carryin=$random;
        opmode=$random;
        @(negedge clk);
        if(M_dut!=0 || P_dut!=0 || Bcout_dut!=0 || carryout_dut!=0 || carryoutF_dut!=0 || P_dut!=0)begin
            $display("Error");
            $stop;
        end
    end
```

```
    rstA=0;
    rstB=0;
    rstM=0;
    rstP=0;
    rstC=0;
    rstD=0;
    rstcarryin=0;
    rstopmode=0;
    ceA=1;
    ceB=1;
    ceM=1;
    ceP=1;
    ceC=1;
    ceD=1;
    cecarryin=1;
    ceopmode=1;
    A=2;
    C=0;
    D=1;
    B=1;
    opmode[6] = 0; //adder1 = D+B
    opmode[4] =1 ; //adder1_mux_out
    opmode[1:0] =1;
    opmode[3:2] = 0;
    opmode[7]= 0;
    carryin =0;
    @(negedge clk);
    //output Bcout =2 , p=2 ,M =2 ,PCout =2
    repeat(100) begin
        A=$random;
        B=$random;
        D=$random;
        C=$random;
        Pcin=$random;
        Bcin=$random;
        carryin=$random;
        opmode=$random;
        @(negedge clk);
    end
    $stop;
end
```

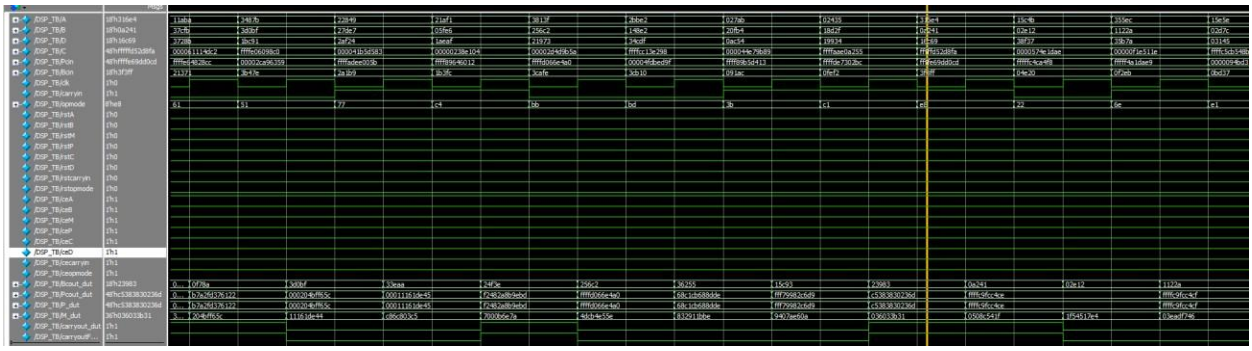
```
initial begin
    $monitor("intput: A = %d\t B = %d\t C = %d\t D = %d\t PCin = %d\t carryin = %d\t opmode =%d\t \n output: Bcout = %d\t PCout =%d\t P = %d\t M =%d\t Carry_Out = %d\t Carry_OutF = %d",
    A,B,C,D,Pcin,carryin,opmode,Bcout_dut,Pcout_dut,P_dut,M_dut,carryout_dut,carryoutF_dut);
end
endmodule
```

Do file:

run_dsp_tb.do

```
vlib work
vlog DSP48A1.v sel_reg.v DSP_TB.v
vsim -voptargs=+acc work.DSP_TB
add wave *
run -all
```

QuestaSim Snippets:

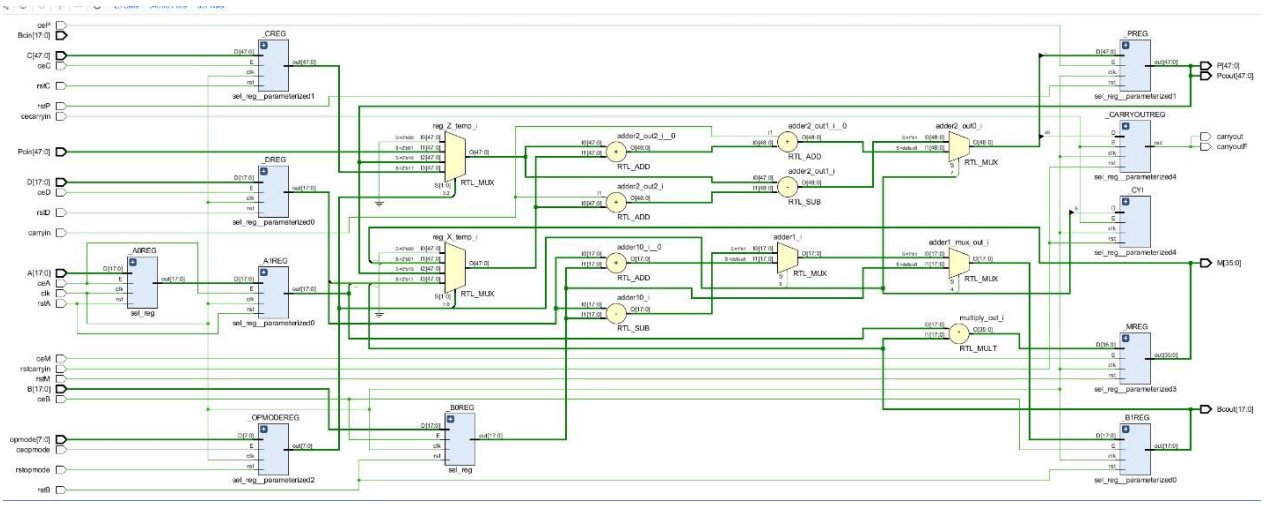


```
# intput: A = 178975  B = 112491  C =      1263109014  D = 196221  PCin = 281472921665547  carryin = 1  opmode = 63
#  output: Bcout =  92077  PCout =281474706953440  P = 281474706953440  M =17205382324  Carry_Out = 0  Carry_OutF = 0
# intput: A = 178975  B = 112491  C =      1263109014  D = 196221  PCin = 281472921665547  carryin = 1  opmode = 63
#  output: Bcout =  83987  PCout =281474706953441  P = 281474706953441  M =11727018797  Carry_Out = 0  Carry_OutF = 0
# intput: A = 120586  B = 146043  C = 281474488630981  D = 243245  PCin = 281474970659583  carryin = 0  opmode =215
#  output: Bcout =  83987  PCout =281474706953441  P = 281474706953441  M =11727018797  Carry_Out = 0  Carry_OutF = 0
# intput: A = 120586  B = 146043  C = 281474488630981  D = 243245  PCin = 281474970659583  carryin = 0  opmode =215
#  output: Bcout =  80120  PCout =254928719629225  P = 254928719629225  M =15031573325  Carry_Out = 0  Carry_OutF = 0
# intput: A = 239421  B = 202205  C = 281474802871019  D =  72474  PCin =      1766210002  carryin = 1  opmode = 38
#  output: Bcout =  80120  PCout =254928719629225  P = 254928719629225  M =15031573325  Carry_Out = 0  Carry_OutF = 0
# intput: A = 239421  B = 202205  C = 281474802871019  D =  72474  PCin =      1766210002  carryin = 1  opmode = 38
#  output: Bcout =  41040  PCout =172799639224537  P = 172799639224537  M = 9661350320  Carry_Out = 1  Carry_OutF = 1
# intput: A =  35357  B =  75990  C = 281474026841742  D = 166898  PCin = 281474061863058  carryin = 0  opmode = 69
#  output: Bcout =  41040  PCout =172799639224537  P = 172799639224537  M = 9661350320  Carry_Out = 1  Carry_OutF = 1
# intput: A =  35357  B =  75990  C = 281474026841742  D = 166898  PCin = 281474061863058  carryin = 0  opmode = 69
#  output: Bcout =  75990  PCout =172798724376939  P = 172798724376939  M = 9825837840  Carry_Out = 1  Carry_OutF = 1
# intput: A =  57854  B =  86125  C = 281472867536900  D = 222375  PCin = 281473120009250  carryin = 0  opmode =141
#  output: Bcout =  75990  PCout =172798724376939  P = 172798724376939  M = 9825837840  Carry_Out = 1  Carry_OutF = 1
# intput: A =  57854  B =  86125  C = 281472867536900  D = 222375  PCin = 281473120009250  carryin = 0  opmode =141
#  output: Bcout =  86125  PCout =     7969136434  P =      7969136434  M = 2686778430  Carry_Out = 1  Carry_OutF = 1
# intput: A =  67845  B =  28987  C = 281473470335052  D = 199119  PCin =      1703015371  carryin = 0  opmode =227
#  output: Bcout =  86125  PCout =     7969136434  P =      7969136434  M = 2686778430  Carry_Out = 1  Carry_OutF = 1
# intput: A =  67845  B =  28987  C = 281473470335052  D = 199119  PCin =      1703015371  carryin = 0  opmode =227
#  output: Bcout =  28987  PCout =281470180758470  P = 281470180758470  M = 4982675750  Carry_Out = 0  Carry_OutF = 0
# intput: A =  92012  B = 223247  C =      1749545424  D =  55643  PCin =       397528367  carryin = 0  opmode =238
#  output: Bcout =  28987  PCout =281470180758470  P = 281470180758470  M = 4982675750  Carry_Out = 0  Carry_OutF = 0
# intput: A =  92012  B = 223247  C =      1749545424  D =  55643  PCin =       397528367  carryin = 0  opmode =238
#  output: Bcout = 223247  PCout =108902585437893  P = 108902585437893  M = 1966623015  Carry_Out = 1  Carry_OutF = 1
# intput: A = 152613  B = 202610  C =        39102212  D =  12980  PCin = 281474173692064  carryin = 1  opmode = 31
#  output: Bcout = 223247  PCout =108902585437893  P = 108902585437893  M = 1966623015  Carry_Out = 1  Carry_OutF = 1
# intput: A = 152613  B = 202610  C =        39102212  D =  12980  PCin = 281474173692064  carryin = 1  opmode = 31
#  output: Bcout = 202610  PCout =172574140818186  P = 172574140818186  M =20541402964  Carry_Out = 1  Carry_OutF = 1
# intput: A =  14300  B =  23572  C = 281474749205732  D =  30773  PCin =      1730128334  carryin = 1  opmode =164
#  output: Bcout = 202610  PCout =172574140818186  P = 172574140818186  M =20541402964  Carry_Out = 1  Carry_OutF = 1
# intput: A =  14300  B =  23572  C = 281474749205732  D =  30773  PCin =      1730128334  carryin = 1  opmode =164
#  output: Bcout =  36552  PCout = 47593923788407  P =  47593923788407  M =30920919930  Carry_Out = 0  Carry_OutF = 0
# intput: A = 224346  B =   6157  C =       711689044  D =  68102  PCin = 281474683005660  carryin = 0  opmode = 55
#  output: Bcout =  36552  PCout = 47593923788407  P =  47593923788407  M =30920919930  Carry_Out = 0  Carry_OutF = 0
# intput: A = 224346  B =   6157  C =       711689044  D =  68102  PCin = 281474683005660  carryin = 0  opmode = 55
#  output: Bcout =   6157  PCout =281474683005660  P = 281474683005660  M =  522693600  Carry_Out = 0  Carry_OutF = 0
# intput: A =  21579  B = 207623  C =       793864030  D =  83545  PCin =      1797362134  carryin = 1  opmode =202
#  output: Bcout =   6157  PCout =281474683005660  P = 281474683005660  M =  522693600  Carry_Out = 0  Carry_OutF = 0
# intput: A =  21579  B = 207623  C =       793864030  D =  83545  PCin =      1797362134  carryin = 1  opmode =202
#  output: Bcout =  13581  PCout =176394785630692  P = 176394785630692  M = 1381298322  Carry_Out = 0  Carry_OutF = 0
# intput: A = 216923  B = 161096  C =       686430545  D =  36096  PCin = 281473877244540  carryin = 1  opmode = 25
#  output: Bcout =  13581  PCout =176394785630692  P = 176394785630692  M = 1381298322  Carry_Out = 0  Carry_OutF = 0
# intput: A = 216923  B = 161096  C =       686430545  D =  36096  PCin = 281473877244540  carryin = 1  opmode = 25
#  output: Bcout = 161096  PCout =281474976710655  P = 281474976710655  M =  293064399  Carry_Out = 1  Carry_OutF = 1
# intput: A =  48319  B = 186257  C = 281474460383938  D = 147055  PCin = 281473902609535  carryin = 1  opmode = 24
#  output: Bcout = 161096  PCout =281474976710655  P = 281474976710655  M =  293064399  Carry_Out = 1  Carry_OutF = 1
# intput: A =  48319  B = 186257  C = 281474460383938  D = 147055  PCin = 281473902609535  carryin = 1  opmode = 24
#  output: Bcout = 222353  PCout =      293064399  P =       293064399  M =34945427608  Carry_Out = 1  Carry_OutF = 1
# intput: A =  65047  B =  77806  C = 281473701604455  D = 113169  PCin = 281472941495309  carryin = 1  opmode = 66
#  output: Bcout = 222353  PCout =      293064399  P =       293064399  M =34945427608  Carry_Out = 1  Carry_OutF = 1
# intput: A =  65047  B =  77806  C = 281473701604455  D = 113169  PCin = 281472941495309  carryin = 1  opmode = 66
#  output: Bcout = 224861  PCout =      293064400  P =       293064400  M =10743874607  Carry_Out = 0  Carry_OutF = 0
# ** Note: $stop    : DSP_TB.v(102)
#    Time: 1510 ns  Iteration: 1  Instance: /DSP_TB
# Break in Module DSP_TB at DSP_TB.v line 102
```

Constraint File:

```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
```

Elaboration (“Messages” tab & Schematic snippets):



Synthesis (“Messages” tab, Utilization report, timing report & Schematic snippets):

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Timing

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<1%)
- Memory
- DSP
  - DSPs (<1%)
    - DSP48E1 only
- IO and GT Specific
  - Bonded IOB (65%)
    - IOB Master Pads
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes

Hierarchy

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	229	158	1	327	1
_A1REG (sel_reg__pa...	0	18	0	0	0
_B1REG (sel_reg__pa...	0	18	0	0	0
_CARRYOUTREG (sel...	0	1	0	0	0
_CREG (sel_reg__par...	0	48	0	0	0
_DREG (sel_reg__par...	0	18	0	0	0
_MREG (sel_reg__par...	0	0	1	0	0
_OPMODEREG (sel_r...	228	7	0	0	0
_PREG (sel_reg__par...	0	48	0	0	0

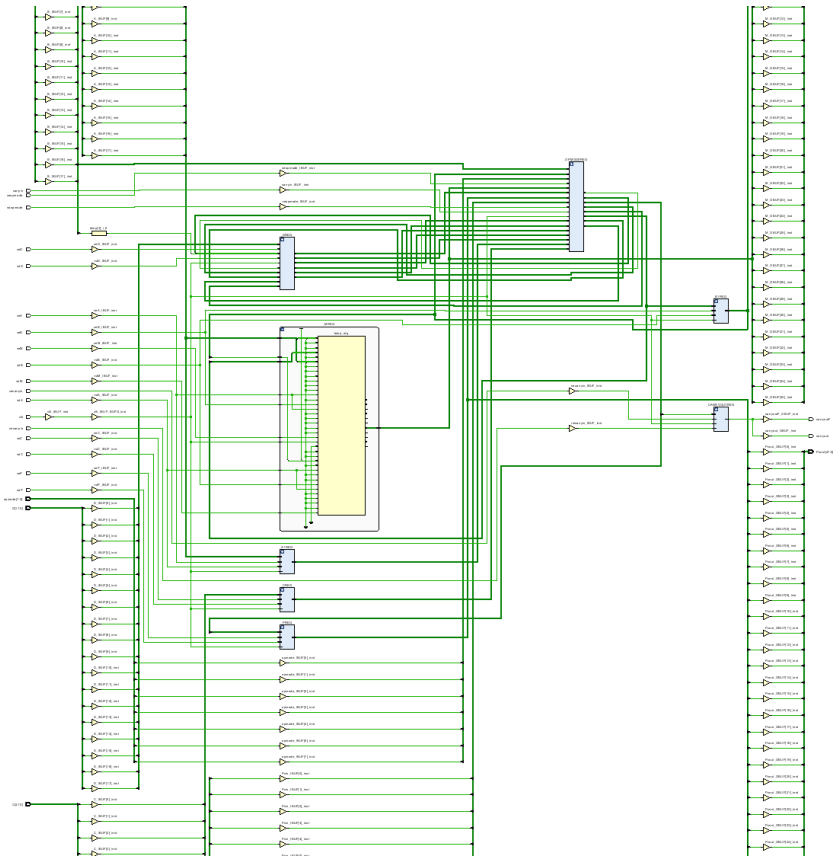
Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Timing

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (326)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

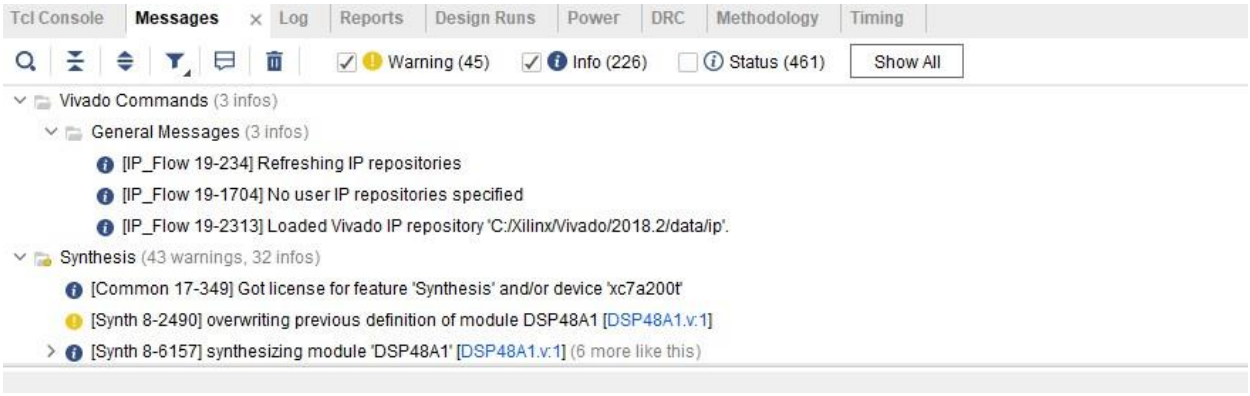
Design Timing Summary

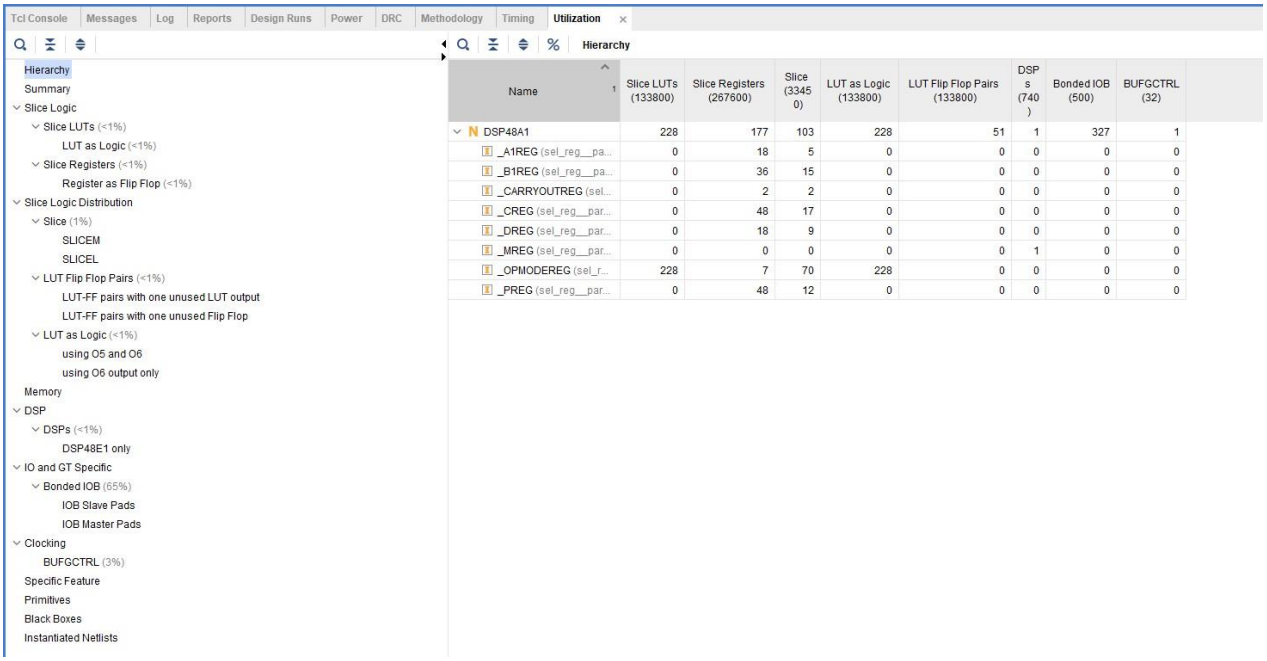
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.168 ns	Worst Hold Slack (WHS):	0.339 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	86	Total Number of Endpoints:	86	Total Number of Endpoints:	160

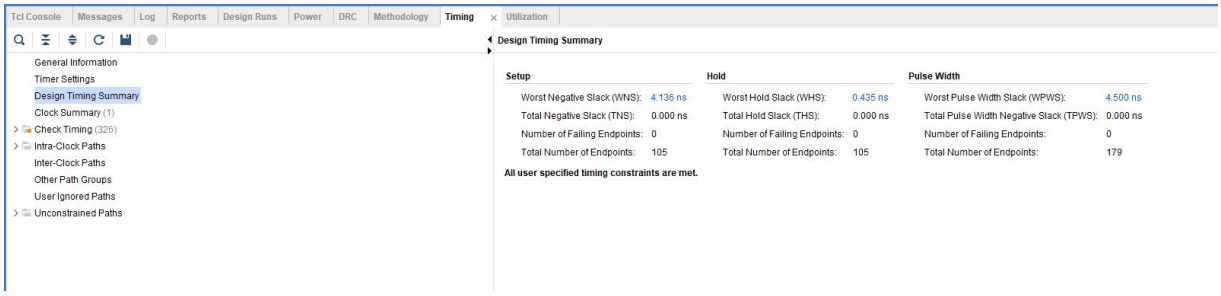
All user specified timing constraints are met.

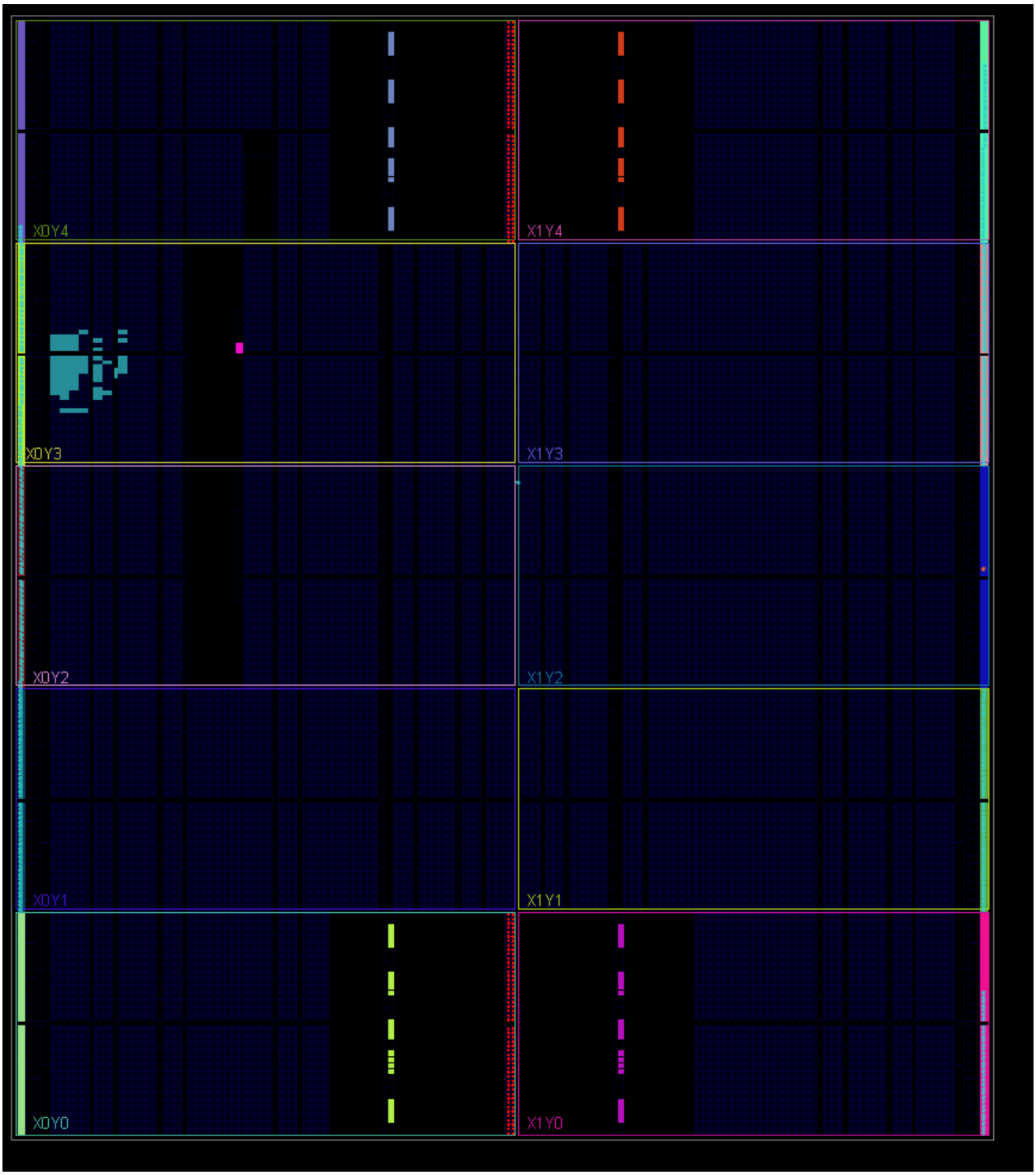


Implementation (“Messages” tab, Utilization report, timing report & device snippets):





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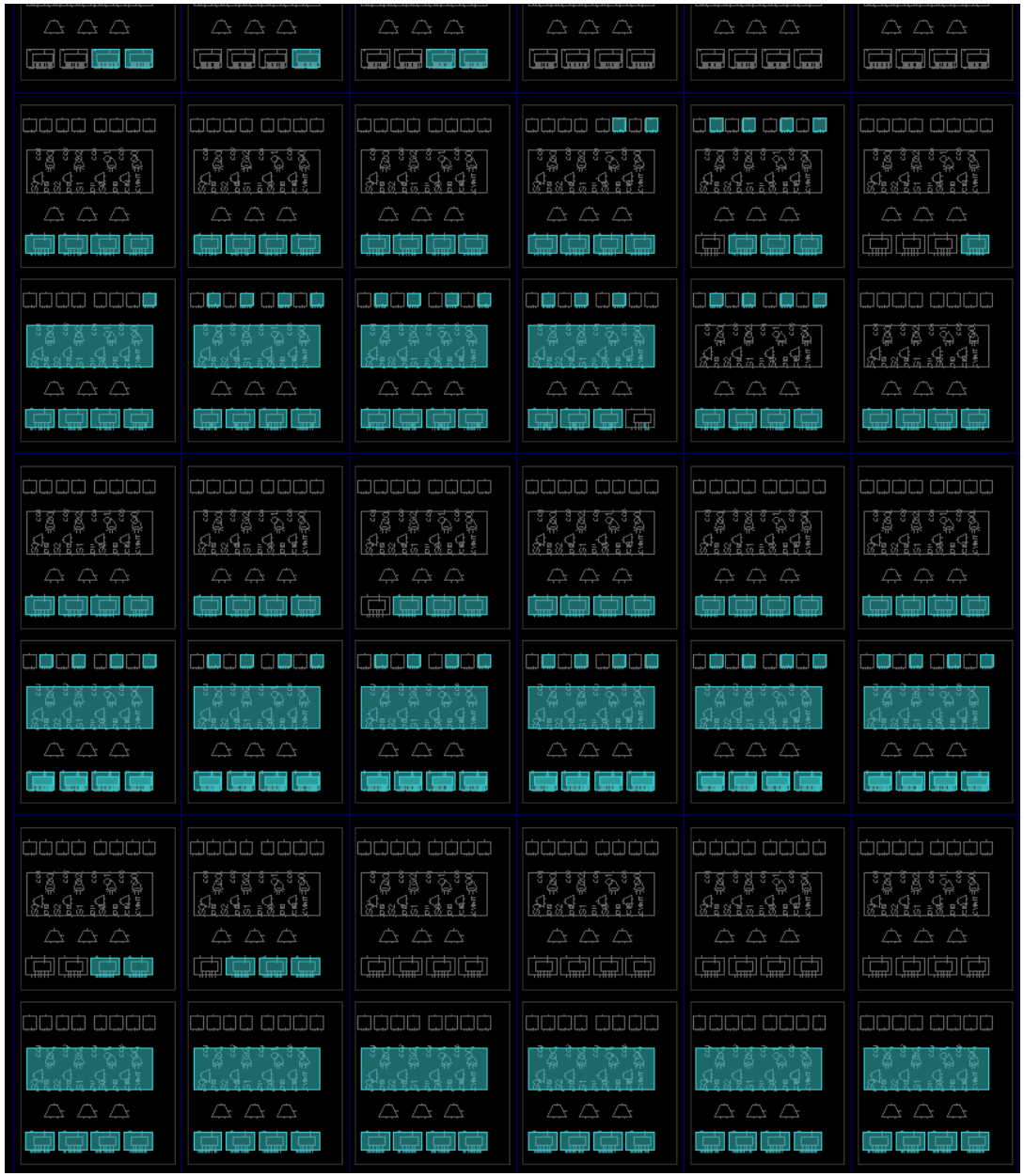

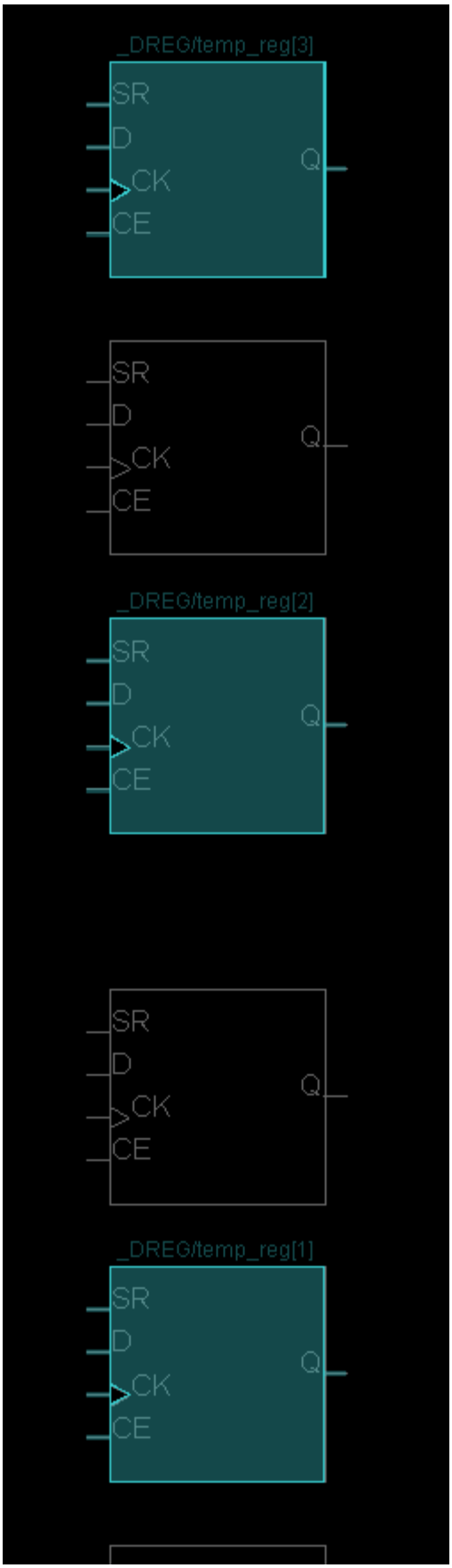
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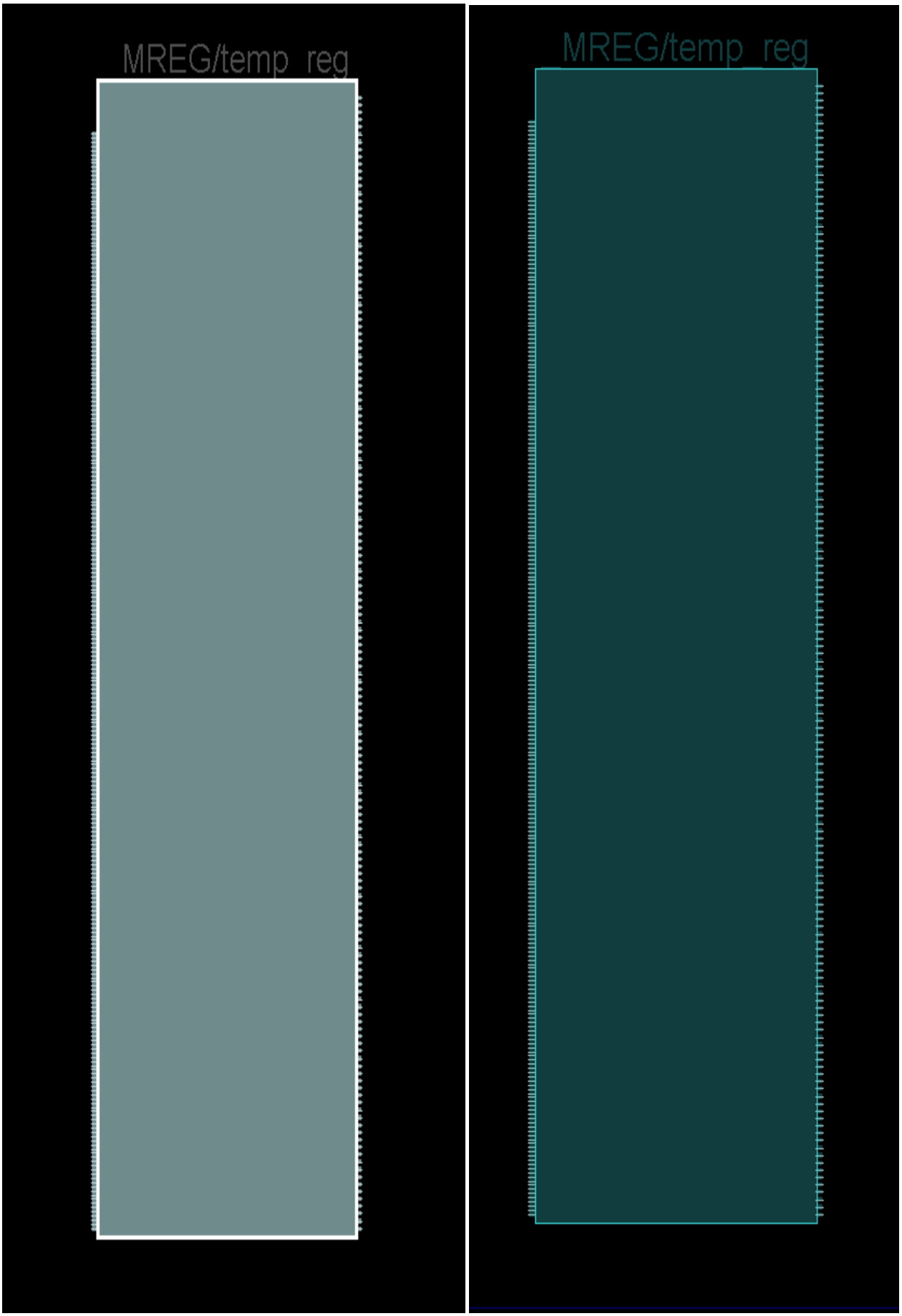
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