



# MT5932 Datasheet

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## Document Revision History

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Revision	Date	Description
1.0	5 May 2017	Initial draft
1.1	16 May 2017	Modified performance values

## Features

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### Wi-Fi

- IEEE 802.11 b/g/n (2.4GHz, 1x1)
- Supports 20MHz, 40MHz bandwidth in 2.4GHz band
- Wi-Fi security WEP/WPA2/WPS
- Wi-Fi direct
- SoftAP, sniffer
- MediaTek Smart Connection
- Single-cloud connectivity
- Receiver antenna diversity
- Integrated Balun, PA/LNA
- Optional external LNA and PA support

### Microcontroller subsystem

- 192MHz ARM® Cortex®-M4 with FPU
- 14 DMA channels
- 1 RTC timer, 1 64-bit and 5 32-bit general purpose timers
- Hardware DFS from 3MHz to 192MHz
- Development support: Serial wire debug (SWD), JTAG
- Crypto engine
- AES 128/192/256 bits
- DES, 3DES
- MD5, SHA-1/224/256/384/512
- True random number generator
- JTAG password protection

### Memory

- Up to 384KB SRAM, with zero-wait state and 96MHz maximum frequency
- Up to 32KB L1 cache, with high hit rate, zero-wait state and 192MHz maximum frequency

### Communication interfaces

- A set of SDIO 2.0 master and SDIO 2.0 slave
- An I2C (3.4Mbps) interface
- Three UARTs (3Mbps, with hardware flow control)
- A set of SPI master and 1 SPI slave (both SCKs are up to 48MHz, quad mode)
- SPI master for external serial flash (48MHz maximum SCK frequency, quad mode)
- Two I2S interfaces
  - 1 16/24-bit, master/slave mode;
  - 1 16-bit, master/slave mode with TDM

- Two TX/RX channels with 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz frequencies.

- Five PWM channels
- 14 GPIOs (fast IOs, 5V-tolerant)
- Three channel 12-bit AUXADC

### Power management

- Integrated DC-DC
- Power input
  - $V_{RTC}$ : from 1.62V to 3.63V
  - $V_{PMU} / V_{RF}$ : 3.3V (+/-10%)
  - $V_{IO\_0}$ : 1.8, 2.8, 3.3V
  - $V_{IO\_1}$ : 1.8, 2.8, 3.3V
- Off mode: <0.5μA
- Retention mode (with RTC)
  - <2.7μA (RTC only)
  - ~4.7μA with 8KB RAM sleep mode
- Deep sleep mode (with external 32kHz clock, SDIO off)
  - 85μA with 0KB RAM sleep mode
  - 113μA with 384KB RAM sleep mode
- G-band RX power: 42mA
- G-band TX power
  - FPA: 248mA at 19dBm CCK
  - FPA: 220mA at 16.5dBm OFDM
- DTIM interval with 32kHz external clock source and 384KB SRAM
  - DTIM=1: 0.63mA
  - DTIM=3: 0.30mA
- Ambient temperature from -30°C to 85°C

### Clock source

- 26MHz or 40MHz crystal oscillator
- 32kHz crystal oscillator or internal 32kHz RC for RTC

### Package type

- 3.223mm x 3.223mm x 0.53mm 56-ball WLCSP with 0.4mm ball pitch

### Note:

The power consumption data is measured at 25°C

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## 1. Introduction

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### 1.1. Overview

MediaTek MT5932 is a highly integrated chipset featuring an application processor, a low power 1x1 11n single-band Wi-Fi subsystem and a power management unit (PMU).

MT5932 is based on ARM® Cortex®-M4 with floating point microcontroller unit (MCU) and supports interfaces including UART, I2C, SPI, I2S, PWM, SDIO and ADC.

The Wi-Fi subsystem contains 802.11b/g/n radio, baseband and MAC designed to meet low-power and high throughput application design requirements. It also contains a 32-bit RISC CPU to fully offload the application processor.

### 1.2. Platform features

#### 1.2.1. Micro-controller subsystem

- ARM® Cortex®-M4 with FPU as application processor with maximum frequency at 192MHz
- 32KB L1 cache with high hit rate and zero wait state, with maximum frequency at 192MHz
- 384KB SYSRAM with zero wait state, with maximum frequency at 96MHz.
- Crypto engine supporting AES, DES/3DES, MD5, SHA1/SHA2
- True random number generator
- Single RTC timer, one 64-bit and five 32-bit general purpose timers (GPTs).
- 14 DMA channels
- eXecute In Place (XIP) on flash
- Dedicated SPI master to an external serial flash with source clock update of up to 80MHz, quad mode.
- Up to 14 GPIO interfaces with 5V-tolerant fast IOs, each IO can be configured as an external interrupt source.

#### 1.2.2. Interfaces

The following interfaces are multiplexed with GPIO.

- SPI master interface, 1, 2 or 4-bit mode, up to 48MHz.
- An SPI slave interface, 1, 2 or 4-bit mode, up to 48MHz.
- An SDIO host interface (v2.0).
- An SDIO device interface (v2.0).
- An I2S interface supporting 16 or 24-bit, master or slave mode (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit or receive, two channels).
- An I2S interface supporting 16-bit, master/slave mode (supports TDM mode) (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit or receive, two channels).
- An I2C master interface (3.4Mbps).

- Up to three UART interfaces with hardware flow control (~3Mbps).
- Up to three channels of 12-bit ADC
- Up to five PWM channels

### 1.3. Wi-Fi subsystem features

#### 1.3.1. Wi-Fi MAC

- Supports all data rates of 802.11g including 6, 9, 12, 18, 24, 36, 48 and 54Mbps.
- Supports short GI and all data rates of 802.11n including MCS0 to MCS7.
- Wi-Fi security WEP, WPA2 and WPS
- Supports Wi-Fi direct, SoftAP and sniffer modes.
- Supports MediaTek Smart Connection.
- Supports single-cloud connectivity.

#### 1.3.2. WLAN baseband

- 20 and 40MHz channels
- MCS0-7 (BPSK,  $r=1/2$  through 64QAM,  $r=5/6$ )
- Supports greenfield, mixed mode and legacy modes.
- Short guard interval
- Supports digital pre-distortion to enhance PA performance.
- Supports RX antenna diversity.

#### 1.3.3. WLAN RF

- Integrated 2.4GHz PA and LNA and T/R switch
- Supports frequency band from 2402 to 2494MHz.
- Single-ended RFIO with an integrated balun
- Supports an optional external LNA and PA.

#### 1.3.4. Core processor

- Dedicated high-performance 32-bit RISC CPU N9 with up to 160MHz clock speed.
- Feasibility Wi-Fi host subsystem in Cortex-M4 MCU to support custom applications.

## 1.4. System block diagram

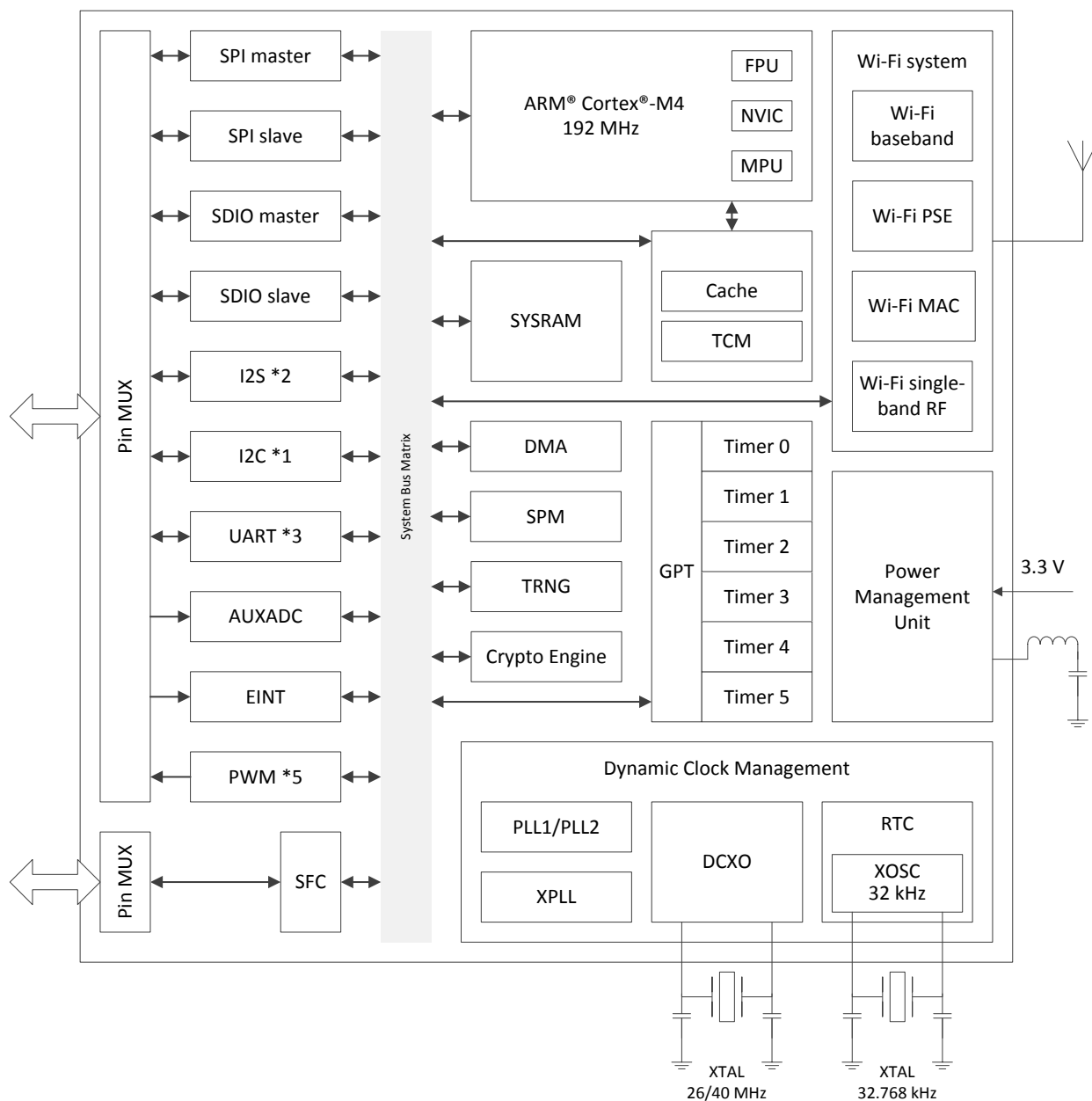


Figure 1.4-1. MT5932 system block diagram



## 2. Functional Overview

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### 2.1. Host processor subsystem

#### 2.1.1. ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has reduced pin count and low power consumption and delivers very high performance efficiency and low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.

MT5932 has further enhanced the Cortex-M4 with FPU to reduce the power by another 11% (in Dhrystone) compared to the original Cortex-M4. Low power consumption is a significant feature for IoT and Wearables application development.

#### 2.1.2. Cache controller

A configurable 32KB cache is implemented to improve the code fetch performance when CPU accesses a non-zero wait-state memory such as EMI, external flash or boot ROM through the on-chip bus.

The core cache is a small block of memory containing a copy of a small portion of cacheable data in the external memory. If CPU reads a cacheable datum, the datum will be copied to the core cache. Once CPU requests the same datum again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory to achieve zero wait-state latency.

The cache can be disabled and this block of memory can be turned into tightly coupled memory (TCM), a high-speed memory for normal data storage. The sizes of TCM and cache can be set to one of the following four configurations:

- 32KB cache, 64KB TCM
- 16KB cache, 80KB TCM
- 8KB cache, 88KB TCM
- 0KB cache, 96KB TCM

#### 2.1.3. Memory management

Three types of memories are implemented for use:

- On-die memories (SRAMs) with up to 96KB at CPU clock speed with zero wait state.

The SRAMs are composed of TCMs and L1 caches. The L1 cache (up to 32KB) is implemented to improve processor access performance of the long latency memories (external flash).

TCMs are designed for high speed, low latency and low power demanding applications. Each TCM has its own power state; active, retention or power-down. TCM must be in active state for normal read and write access. Retention state saves the SRAM content and consumes the minimum leakage current with no access. Power-down loses the content and consumes almost zero power.

The TCMs can also be accessed by other internal AHB masters like DMA or multimedia subsystem for low power applications. These applications can run on TCM without powering on the external flash to save more power.

Boot ROM is also implemented for processor boot-up and its content is unchangeable.

## 2.1.4. Memory protection unit (MPU)

The MPU is an optional component to manage the CPU access to memory. The MPU provides full support for:

- Protection regions (up to 8 regions and can be further divided up into 8 sub-regions).
- Overlapping protection regions, with region priority.
- Access permissions.
- Exporting memory attributes to the system.

The MPU is useful for applications where a critical code has to be protected against the misbehavior of other tasks. It can be used to define access rules, enforce privilege rules and separate processes.

## 2.1.5. Nested Vectored Interrupt Controller (NVIC)

The NVIC supports up to 32 maskable interrupts and 16 interrupt lines of Cortex-M4 with 32 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

## 2.1.6. External Interrupt Controller

The external interrupt controller consists of up to 32 edge detectors for generating event/interrupt requests. Each input line can be independently configured to select the type (interrupt or event) and the corresponding trigger event (rising edge or falling edge or both or level). Each line can also be masked independently. A pending register maintains the status line of the interrupt requests. Up to 21 GPIOs can be connected to 21 external interrupt lines.

## 2.1.7. Bus architecture

To better support various IoT applications, MT5932 adopts 32-bit multi-AHB matrix to provide low-power, fast and flexible data operation.

Table 2.1-1 shows the interconnections between bus masters and slaves.

- The bus masters include Cortex-M4, SPM, SPI master, SPI slave, SDIO master, SDIO slave, Crypto engine, Wi-Fi connectivity system and DMA.
- The bus slaves include the Always On (AO) domain APB peripherals, Power Down (PD) domain APB peripherals, TCM, SFC, EMI, SYSRAM, RTC SRAM and Wi-Fi connectivity system.

**Table 2.1-1. MT5932 bus connection**

Master Slave	ARM Cortex- M4	PD DMA	SPM	SPI Master	SPI Slave	SDIO Master	SDIO Slave	Crypto Engine	CONNSYS Master
AO APB Peripherals	•	•	•					•	
PD APB Peripherals	•	•	•					•	
TCM	•	•	•					•	
EMI	•	•	•	•	•	•	•	•	•
SFC	•	•	•					•	
SYSRAM	•	•	•	•	•	•	•	•	•
RTC SRAM	•	•	•	•	•	•	•	•	•
CONNSYS	•	•	•					•	

### 2.1.8. Direct Memory Access (DMA) controller

MT5932 chipset features three DMA controllers, containing 16 channels in power down domain. They manage data transfer between the peripheral devices and memory.

There are three types of DMA channels in the DMA controller – full-size DMA channel, half-size DMA channel and virtual FIFO DMA for different peripheral devices. DMA controllers support ring-buffer and double-buffer memory data transactions.

To improve the bus efficiency, the DMA controllers provide an unaligned-word access function. When this function is enabled, it can automatically convert the address format from the unaligned type to aligned type, ensuring compliance with the AHB/APB protocol.

Each peripheral device is connected to a dedicated DMA channel that can configure transfer data sizes, source address and destination address by software. The DMA controllers can be used with the following peripherals:

- Two I2C interfaces
- A single HIF (Wi-Fi AHB interface signal)
- Two I2S interfaces
- Three UART interfaces

## 2.2. Boot source

There are three boot source options:

- Serial flash
- SPI slave (to load binary from host)
- SDIO slave (to load binary from host)

The host may transmit a binary through SPI slave or SDIO slave to internal SRAM. The MCU (Cortex-M4) can execute on internal SRAM after transmission is complete. The boot source in boot ROM is determined according to the flowchart shown in Figure 2.2-1. HIF\_EN and HIF\_SEL can be configured at power up using GPIO\_4 and GPIO\_13, respectively.

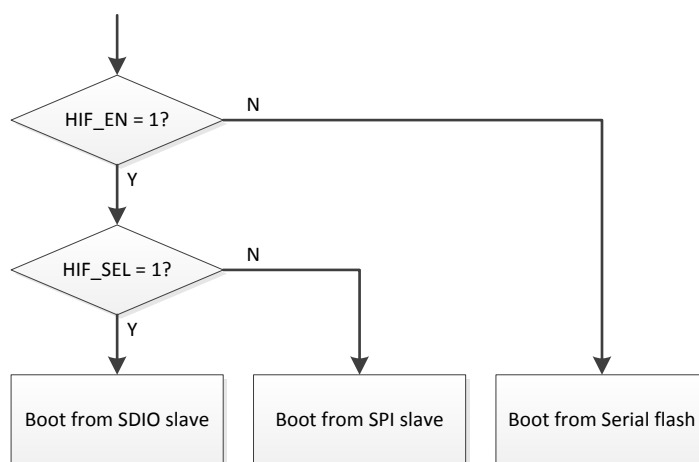


Figure 2.2-1. Boot source flow

## 2.3. Clock architecture

The clock controller (see Figure 2.3-1) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler.** To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching.** The clock sources can be changed safely at runtime through a configuration register.
- **Clock management.** To reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory. The AHB and APB clock supports Dynamic Clock Management (DCM) with a dynamic clock slow down or gating when the bus fabric is idle.
- **System clock source.** Two different clock sources can be used to drive the master clock ( $F_{CPU}$  and  $F_{BUS}$ ):
  - 26MHz/40MHz Crystal Oscillator (XO), that can supply reference clock for PLLs.
  - Baseband PLL1 (BBPLL1) with XO as a reference clock and a maximum frequency at 1040MHz.
  - Baseband PLL2 (BBPLL2) with XO as a reference clock or divided from BBPLL1 and a fixed frequency at 960MHz.
- **Auxiliary clock source.** Three ultralow-power clock sources that can be used to drive the real-time clock  $F_{FRTC\_CK}$ .

- Embedded EOSC32K is the default F\_FRTC\_CK clock source:
  - 32 kHz low-speed internal RC (EOSC32K) with  $\pm 5\%$  variation
- The fifth bit (nm\_trap\_slow\_src\_sel) of SYSTEM\_INFO is 1, users can switch to low-speed internal clock divided from Crystal Oscillator (XO) (XO\_DIV\_32K\_CK) to get more accurate clock source:
  - If XO is 40MHz, XO\_DIV\_32K\_CK is 32.760 kHz (0.024%).
  - If XO is 26MHz, XO\_DIV\_32K\_CK is 32.745 kHz (0.07%).
- The fifth bit (nm\_trap\_slow\_src\_sel) of SYSTEM\_INFO is 0, users can switch to XOSC32K:
  - 32.768kHz low-speed external crystal (XOSC32K)
- **Peripheral clock sources.** Three types of peripheral clock source options are used. Each peripheral has its own gating register:
  - Several peripherals (SDIOMST (MSDC), SPIMST and SFC) have their own clock independent from the system clock. BBPLL1 and BBPLL2, each having independent outputs allowing the highest flexibility, can generate independent clocks for the SDIOMST (MSDC), SPIMST and SFC.
  - Clock of several peripherals including three I2Cs, a crypto engine, DMA and more is the same as fast AHB/APB bus clock ( $F_{BUS}$ ).
  - Clock of several low speed peripherals (SEJ, AUXADC, EFUSE and more) is from F\_FXO\_CK (26MHz or 20MHz). The clock frequency of GPTIMER is from either F\_FXO\_D2\_CK (13MHz or 10MHz) or F\_RTC\_CK (32kHz).
- **Clock-out**
  - Default output from CLKOUT pin (CLKO0~CLKO4) is the F\_FRTC\_CK clock. It also can output F\_FXO\_CK clock (26MHz or 20MHz) or XPLL clock (26MHz, 24.576MHz or 22.5792MHz) by setting GPIO\_CLKO\_CTRL\_A and GPIO\_CLKO\_CTRL\_B.

26MHz or 40MHz XO is selected on reset as a default CPU clock. This clock source is input to a set of cascaded PLL (BBPLL1 and BBPLL2) thus allowing to increase the CPU frequency ( $F_{CPU}$ ) up to 192MHz when V<sub>CORE</sub> is 1.15V. Several prescalers enable the configuration of the fast bus clock, the maximum frequency of the AHB and APB bus ( $F_{BUS}$ ) is 96MHz, while the maximum frequency of low-speed bus domains is 26MHz or 20MHz (divided from 40MHz XO clock). The frequency ratio of  $F_{CPU}$  and  $F_{BUS}$  needs to be 2:1. The devices with an embedded low jitter XPLL achieve better I2S performance. The XPLL can output either 24.576MHz for 48kHz base I2S sample rate or 22.5792MHz for 44.1kHz base I2S sample rate.

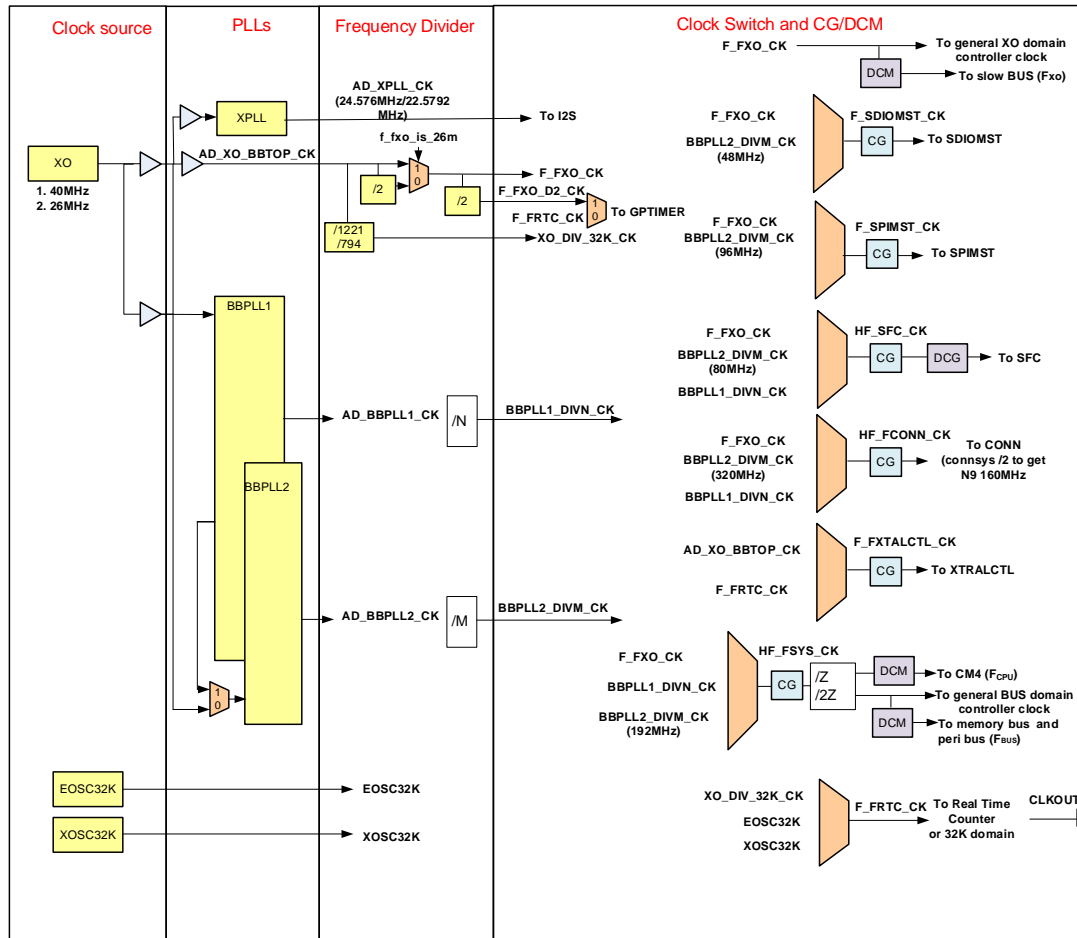


Figure 2.3-1. MT5932 clock source architecture

## 2.4. Serial interfaces

### 2.4.1. Universal Asynchronous Receiver Transmitter (UART)

MT5932 chipset houses three UART interfaces that provide full duplex serial communication between the baseband chipset and external devices. UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rates from 110bps up to 921,600bps and baud rate auto-detection function. They provide hardware and software flow control of the RTS/CTS signals.

UARTs can configure data transfer lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits by software. They can be served by the DMA controller.

### 2.4.2. Serial Peripheral Interface (SPI)

MT5932 chipset features one SPI master controller and one SPI slave controller to receive and transmit device data using single, dual and quad SPI protocol. The SPI controllers can communicate at up to 48 Mbps.

The chip select signal and SPI clock of SPI master controllers are configurable. The SPI controllers also support DMA mode for large amounts of data transmission.

### 2.4.3. Inter-Integrated Circuit (I2C) Interface

MT5932 chipset provides two I2C master controllers. There are three types of speed modes in the I2C controllers: standard mode (100kbps), fast mode (400kbps) and high-speed mode (3.4Mbit/s), supporting 7-bit/10-bit addressing and can be served by the DMA controller. The I2C package size supports up to 1,024 bytes per transfer and 1,024 transfers per transaction in DMA mode and 8 bytes per transfer in non-DMA mode.

START/STOP/REPEATED START condition can be increased to support single or multi transfer. These features can be configured by software based on design requirements.

### 2.4.4. Inter-IC Sound Interface (I2S)

MT5932 chipset provides two Inter-IC Sound Interface (I2S) controllers. The controllers can be selected as master or slave. There are two types of transfer protocols in the I2S controllers: one is the I2S protocol, supporting 24-bit, 16-bit addressing and mono, stereo transaction; the other is the TDM protocol, supporting 16-bit addressing and TDM32, TDM64, TDM128 transaction.

I2S controllers can be served by the DMA controller and the sample rate can support either 16, 24, 48, 96, 192kHz or 11.025, 22.05, 44.1kHz when sharing only one internal PLL. Detailed specifications of the I2S and TDM are shown in Table 2.4-1 and Table 2.4-2.

**Table 2.4-1. I2S protocol specifications**

I2S Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b I2S1: 16b/24b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo
Slave Mode	I2S0: 16b I2S1: 16b/24b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo

**Table 2.4-2. TDM protocol specifications**

TDM Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b	<ul style="list-style-type: none"> <li>XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64</li> <li>XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, TDM32/TDM64</li> <li>XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, TDM32/TDM64</li> </ul>
Slave Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128) XPLL 22.5792MHz (either of the following): <ul style="list-style-type: none"> <li>11.025, 22.05, 44.1, 88.2 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128)</li> <li>176.4 kHz, TDM32/TDM64</li> </ul> XPLL 24.576MHz (either of the following): <ul style="list-style-type: none"> <li>8, 12, 16, 24, 32, 48, 96 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128)</li> <li>192 kHz, TDM32/TDM64</li> </ul>

### 2.4.5. SD memory card controller

MT5932 supports the SD memory card bus protocol, as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0.

Furthermore, the controller also partially supports the SDIO card specification version 2.0. However, the controller can only be configured as the host of the SD memory card. Hereafter, the controller is abbreviated as the SD controller.

Main features of the controller:

- 32-bit access for control registers
- 8, 16 and 32-bit access for FIFO in PIO mode
- Built-in CRC circuit
- Supports PIO mode, basic DMA mode and descriptor DMA mode for SD controller.
- Interrupt capabilities
- Data rate of up to 48Mbps in 1-bit mode and 48x4 Mbps in 4-bit mode. The module is targeted at 48MHz operating clock.
- Programmable serial clock rate on SD bus (256 gears)
- Card detection capabilities (MT5932 uses the EINT controller for card detection)
- Does not support SPI mode for SD memory card.
- Does not support suspend/resume for SD memory card.

## 2.5. Peripherals

### 2.5.1. Pulse-Width Modulation (PWM)

There are five PWM controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers can be configured to use 40MHz, 13MHz or 32kHz clock source to support a wide range of output pulse frequencies.

### 2.5.2. General Purpose Input/Output (GPIO)

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output (push-pull or open-drain) or as an input (with or without pull-up or pull-down) that supports input floating with buffer gating to reduce power consumption. Most of the GPIOs are multiplexed with peripheral functions and have selectable output driving strength. The maximum toggling speeds of a single GPIO are listed in Table 2.5-1.

If the MCU handles more than one GPIO at a time or receives an interrupt, a rapid performance degradation may occur.

Dedicated IOs operate at higher speeds depending on the peripheral or interface usage. For example, PWM IOs can output 20 MHz when V<sub>CORE</sub> is 1.15V.

**Table 2.5-1. GPIO speeds when the Cortex-M4 cache is enabled**

V <sub>CORE</sub>	Cortex-M4 speed	Maximum toggling speed of single GPIO pin
1.15V	192MHz	1MHz
1.15V	96MHz	500kHz



VCORE	Cortex-M4 speed	Maximum toggling speed of single GPIO pin
0.85V	N/A	N/A (Cortex-M4 is in deep sleep mode)

### 2.5.3. General Purpose Timer (GPT)

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes and can operate on one of the two clock sources; RTC clock (32.768kHz) and system clock (13MHz).

### 2.5.4. Real Time Clock (RTC)

The RTC module provides time and data information, as well as 32.768kHz clock source. The clock is selected between three clock sources — one from an external (XOSC32) and two from an internal (XO, EOSC32). The RTC block has an independent power supply. When the MT5932 platform is at retention mode, a dedicated regulator will supply power to the RTC block. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum value. The year span is supported until up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

### 2.5.5. True Random Number Generator (TRNG)

The TRNG is a device in power-down domain that generates random numbers from the ring oscillator (RO) outputs. Various types of ROs are adopted, including Hybrid Fibonacci Ring Oscillator (H-FIRO), Hybrid Ring Oscillator (H-RO) and Hybrid Galois Ring Oscillator (H-GARO). Interrupt request (IRQ) will be issued once the random data is successfully generated.

### 3. Wi-Fi RF Subsystem

#### 3.1. Wi-Fi radio characteristics

##### 3.1.1. Wi-Fi RF block diagram

Front-end loss with an external balun (2.4GHz band with band insertion loss of 1dB).

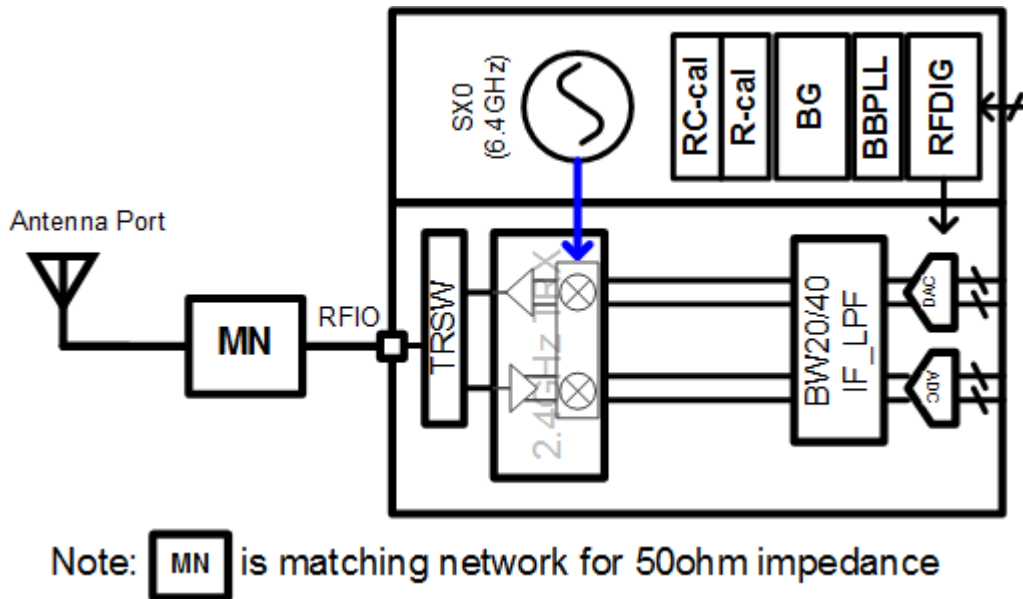


Figure 3.1-1. 2.4GHz RF block diagram

##### 3.1.2. Wi-Fi 2.4GHz band RF receiver specifications

The specifications listed in Table 3.1-1 are measured at the antenna port, including the front-end loss.

Table 3.1-1. 2.4GHz RF receiver specifications

Parameter	Description	Performance			
		Minimum	Typical	Maximum	Unit
Frequency range	Center channel frequency	2412		2484	MHz
RX sensitivity	1 Mbps CCK	-	-97.5	-	dBm
	2 Mbps CCK	-	-94.5	-	dBm
	5.5 Mbps CCK	-	-92.5	-	dBm
	11 Mbps CCK	-	-89.5	-	dBm
RX sensitivity	BPSK rate 1/2, 6 Mbps OFDM	-	-94.5	-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-93.3	-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-91.5	-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-89.1	-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-85.8	-	dBm

Parameter	Description	Performance			
	16QAM rate 3/4, 36 Mbps OFDM	-	-82.4	-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-78.2	-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-77.0	-	dBm
RX sensitivity 20MHz bandwidth Mixed mode 800ns guard interval Non-STBC	MCS 0, BPSK rate 1/2	-	-93.9	-	dBm
	MCS 1, QPSK rate 1/2	-	-90.7	-	dBm
	MCS 2, QPSK rate 3/4	-	-88.3	-	dBm
	MCS 3, 16QAM rate 1/2	-	-85.3	-	dBm
	MCS 4, 16QAM rate 3/4	-	-81.8	-	dBm
	MCS 5, 64QAM rate 2/3	-	-77.4	-	dBm
	MCS 6, 64QAM rate 3/4	-	-76	-	dBm
	MCS 7, 64QAM rate 5/6	-	-74.8	-	dBm
RX sensitivity 40MHz bandwidth Mixed mode 800ns guard interval Non-STBC	MCS 0, BPSK rate 1/2	-	-90.5	-	dBm
	MCS 1, QPSK rate 1/2	-	-87.7	-	dBm
	MCS 2, QPSK rate 3/4	-	-85.2	-	dBm
	MCS 3, 16QAM rate 1/2	-	-81.7	-	dBm
	MCS 4, 16QAM rate 3/4	-	-78.6	-	dBm
	MCS 5, 64QAM rate 2/3	-	-74.0	-	dBm
	MCS 6, 64QAM rate 3/4	-	-72.7	-	dBm
	MCS 7, 64QAM rate 5/6	-	-71.5	-	dBm
Maximum receive level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-20	-	dBm
Receive adjacent Channel rejection	1 Mbps CCK	-	40	-	dBm
	11 Mbps CCK	-	40	-	dBm
	BPSK rate 1/2, 6 Mbps OFDM	-	34	-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	22	-	dBm
	HT20, MCS 0, BPSK rate 1/2	-	33	-	dBm
	HT20, MCS 7, 64QAM rate 5/6	-	15	-	dBm
	HT40, MCS 0, BPSK rate 1/2	-	29	-	dBm
	HT40, MCS 7, 64QAM rate 5/6	-	9	-	dBm

### 3.1.3. Wi-Fi 2.4GHz band RF transmitter specifications

The specifications listed in Table 3.1-2 are measured at the antenna port including the front-end loss.

**Table 3.1-2. 2.4GHz RF transmitter specifications**

Parameter	Description	Performance			
		Minimum	Typical	Maximum	Unit

Parameter	Description	Performance			
Frequency range		2412	-	2484	MHz
Output power with spectral mask and EVM compliance	1 Mbps CCK	-	19	-	dBm
	11 Mbps CCK	-	19	-	dBm
	6 Mbps OFDM	-	18.5	-	dBm
	54 Mbps OFDM	-	16.5	-	dBm
	HT20, MCS 0	-	17.5	-	dBm
	HT20, MCS 7	-	15.5	-	dBm
	HT40, MCS 0	-	16.5	-	dBm
	HT40, MCS 7	-	14.5	-	dBm
TX EVM	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20, MCS 0	-	-	-5	dB
	HT20, MCS 7	-	-	-28	dB
	HT40, MCS 0	-	-	-5	dB
	HT40, MCS 7	-	-	-28	dB
Output power variation <sup>(1)</sup>	TSSI closed-loop control across all temperature ranges and channels and VSWR $\leq$ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power	Second harmonic	-	-45	-43	dBm/MHz
	Third harmonic	-	-45	-43	dBm/MHz

<sup>(1)</sup> No SYSRAM data is retained in these scenarios.

## 4. Power Management Unit

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### 4.1. Overview

The power management unit (PMU) manages the power supply of the chip, including baseband, processor, memory, camera, vibrator and more. There are two power input sources for MT5932:

- 1) AVDD33\_RTC for RTC timer control.

This is operated by wider input voltage range from 1.62V to 3.63V and supports real time clock control and alarm logic. Because of the ultra-low input voltage and lower current consumption, it can efficiently enhance battery lifetime by alkaline or other portable batteries.

- 2) AVDD33\_BUCK for PMU control.

A single regulated 3.3V power supply is required for the MT5932. It could be from an external DC-DC converter to convert a higher voltage supply to 3.3V or boost from a lower voltage supply to 3.3V. The PMU contains Under-Voltage Lockout (UVLO) circuit, several Low Drop-out Regulators (LDOs), a high efficiency buck converter and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection and low output noise.

### 4.2. Low-power operating mode

The MT5932 power state diagram is shown in Figure 4.2-1. In **ACTIVE** mode, the Cortex-M4 and N9 power states operate independently, and both have Idle, Active and Sleep modes. When both are in sleep mode, the chipset enters **SLEEP** mode. In **SLEEP** mode, the PMU is in low power mode with low current consumption.

**RETENTION** mode provides a lower current consumption than **SLEEP** mode. It is suitable for applications that remain idle for a long period. To enter **RETENTION** mode is software configurable and to exit, use RTC timer or EINT.

**OFF** mode is controlled by the CHIP\_EN signal and in this state, only always-on PMU logics are alive to maintain the lowest current consumption.

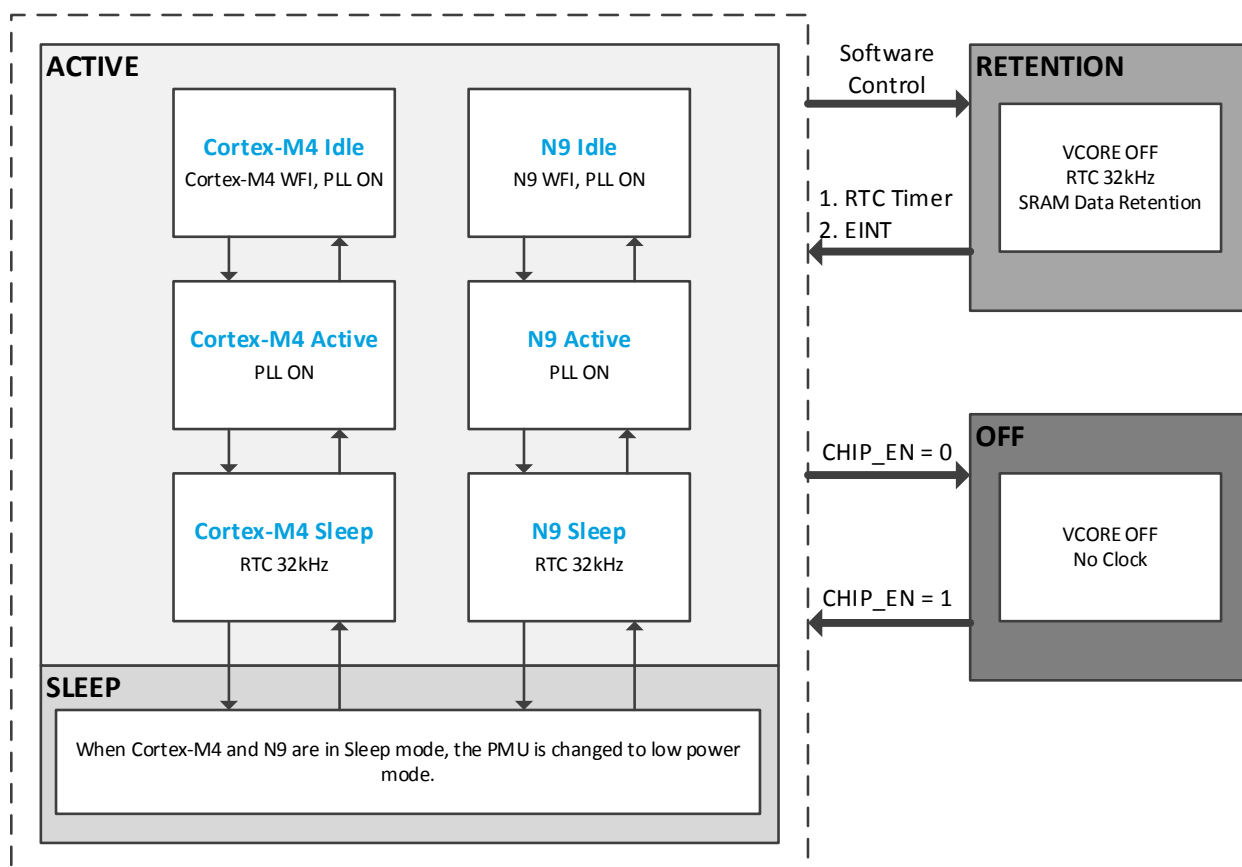


Figure 4.2-1. MT5932 Cortex-M4 and N9 power state and power mode

### 4.3. PMU architecture

The 3.3V power source is directly supplied to the switching regulator, digital IOs and RF-related circuit. It is converted to 1.45V by the buck converter for low voltage circuits. The built-in digital LDOs and RF LDOs convert 1.45V to 1.15V for digital, RF and BBPLL core circuits. The three LDOs are CLDO, SLDO-H and MLDO. SLDO-H stands for sleep mode LDO, CLDO stands for digital core LDO, and MLDO stands for internal or external memory LDO.

In **ACTIVE** mode, the buck converter converts 1.45V output to other subsystems in MT5932. It can operate in either PFM mode or PWM mode. With an external on-board LC filter (2.2μH inductor and 10μF cap), it outputs a low ripple 1.45V to Wi-Fi RF system and CLDO input power. In **ACTIVE** mode, CLDO is under BUCK domain, and then it outputs 1.15V for the whole chip's digital logic.

In **SLEEP** mode, BUCK output voltage will be kept by SLDO-H. The SLDO-H also generates 1.45V output voltage for Wi-Fi RF subsystem and CLDO input power. While MT5932 is in **SLEEP** mode, CLDO will reduce its output level from 1.15V to 0.85V for the chipset's digital logic to reduce power consumption.

In **RETENTION** mode, BUCK, CLDO, SLDO-H and MLDO are shut down. During this mode, only always-on PMU logics, RTC timer controller and retention SRAM are alive to keep lower current consumption.

Once MT5932 goes into **OFF** mode (controlled by CHIP\_EN), BUCK, CLDO, SLDO-H, MLDO and RTC controller will be shut down. During this mode, only some PMU AO domain blocks are alive to keep lowest current consumption.

### 4.4. Power performance

Table 4.4-1 lists example current consumptions in VBAT domain.

**Table 4.4-1. Current consumption in different power modes**

Operation Mode		Test Conditions <sup>(1)</sup>	Current Consumptions <sup>(2)</sup>	Unit
Power Mode	Scenario			
OFF	OFF	<ul style="list-style-type: none"> <li>CHIP_EN keeps low</li> </ul>	< 0.5	μA
RETENTION	RETENTION	<ul style="list-style-type: none"> <li>RTC Timer</li> <li>0KB SRAM data retention</li> </ul>	2.7	μA
		<ul style="list-style-type: none"> <li>RTC Timer</li> <li>8KB SRAM data retention</li> </ul>	4.7	μA
SLEEP	SLEEP_ext_32Khz	<ul style="list-style-type: none"> <li>Cortex-M4 in sleep state</li> <li>TCM 96KB SRAM is retained</li> <li>XTAL 32kHz</li> </ul>	85	μA
	SLEEP_int_32Khz	<ul style="list-style-type: none"> <li>Cortex-M4 in sleep state</li> <li>TCM 96KB SRAM is retained</li> <li>Internal 32kHz</li> </ul>	355	μA
ACTIVE	Wi-Fi TX	<ul style="list-style-type: none"> <li>CCK 19dBm</li> <li>N9 in idle state</li> <li>Cortex-M4 in sleep state</li> <li>TCM 96KB SRAM is retained</li> <li>XTAL 32kHz</li> </ul>	248	mA
		<ul style="list-style-type: none"> <li>OFDM 16.5dBm</li> <li>N9 in idle state</li> <li>Cortex-M4 in active state</li> <li>TCM 96KB SRAM is retained</li> <li>XTAL 32kHz</li> </ul>	220	mA
	Wi-Fi RX	<ul style="list-style-type: none"> <li>HT20_MCS7</li> <li>N9 in active state</li> <li>Cortex-M4 in active state</li> <li>XTAL 32kHz</li> </ul>	42	mA
		<ul style="list-style-type: none"> <li>HT20_MCS7</li> <li>N9 in idle state</li> <li>Cortex-M4 in sleep state</li> <li>XTAL 32kHz</li> </ul>	21	mA
ACTIVE and SLEEP	DTIM = 1	<ul style="list-style-type: none"> <li>Cortex-M4 in sleep state</li> <li>TCM 96KB SRAM is retained</li> <li>XTAL 32kHz</li> </ul>	630	μA

<sup>(1)</sup> No SYSRAM data is retained in these scenarios.

<sup>(2)</sup> Conditions: VBAT and VDDIO at 3.3V, temperature at 25°C, typical corner IC, XTAL at 26MHz

## 5. Pin Description

### 5.1. MT5932 pin list

For MT5932, a WLCSP 3.223mm x 3.223mm, 56-ball, 0.4mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 5.1-1.

	1	2	3	4	5	6	7	8	
A	SFSCK	SFSOUT	DVDD_MLDO	GPIO0		XO	AVSS15_WF0_LF		A
B	DVDD_IO_1	SFSCS0	SFSHOLD	GPIO1	AVDD15_XO	AVDD15_WF0_TX	AVSS15_WF0_TRX	WF0_GRFIO	B
C	SFSIN	SFSWP	GPIO2	GPIO3	DVDD_CORE	AVDD33_WF0_GTX			C
D	AVSS33_MISC	AVSS33_MISC	GND	GND	DVDD_CORE	AVDD33_WF0_GPA	AVSS33_WF0_GPA	AVSS_WF0_GBALUN	D
E	AVDD15_V2P5NA	AVSS33_BUCK	GND		GPIO4	GPIO19	GPIO20		E
F		LXBK	GND	EXT_PWR_EN	RTC_EINT	DVDD_CORE	GPIO16	GPIO17	F
G	AVDD33_BUCK	AVDD15_CLDO	AVDD33_MISC	XOUT	XIN	GPIO15	GPIO14	DVDD_IO_0	G
H	AVDD12_CLDO	AVDD18_MLDO	AVDD33_VRTC	CHIP_EN		GPIO13	GPIO11	GPIO12	H
	1	2	3	4	5	6	7	8	

Figure 5.1-1. MT5932 ball diagram and top view

#### 5.1.1. MT5932 pin coordination

Table 5.1-1. MT5932 ball coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	SFSCK	B1	DVDD_IO_1	C1	SFSIN
D1	AVSS33_MISC	E1	AVDD15_V2P5NA	G1	AVDD33_BUCK
H1	AVDD12_CLDO	A2	SFSOUT	B2	SFSCS0
C2	SFSWP	D2	AVSS33_MISC	E2	AVSS33_BUCK



Pin#	Net name	Pin#	Net name	Pin#	Net name
F2	LXBK	G2	AVDD15_CLDO	H2	AVDD18_MLDO
A3	DVDD_MLDO	B3	SFSHOLD	C3	GPIO2
D3	GND	E3	GND	F3	GND
G3	AVDD33_MISC	H3	AVDD33_VRTC	A4	GPIO0
B4	GPIO1	C4	GPIO3	D4	GND
F4	EXT_PWR_EN	G4	XOUT	H4	CHIP_EN
B5	AVDD15_XO	C5	DVDD_CORE	D5	DVDD_CORE
E5	GPIO4	F5	RTC_EINT	G5	XIN
A6	XO	B6	AVDD15_WF0_TRX	C6	AVDD33_WF0_G_TX
D6	AVDD33_WF0_G_PA	E6	GPIO19	F6	DVDD_CORE
G6	GPIO15	H6	GPIO13	A7	AVSS15_WF0_LF
B7	AVSS15_WF0_TRX	D7	AVSS33_WF0_G_PA	E7	GPIO20
F7	GPIO16	G7	GPIO14	H7	GPIO11
B8	WF0_G_RFIO	D8	AVSS_WF0_G_BALUN	F8	GPIO17
G8	DVDD_IO_0	H8	GPIO12		

### 5.1.2. MT5932 pin types

**Table 5.1-2. Acronym for pin types and I/O structure**

Name	Abbreviation	Description
Pin Type	AI	Analog input
	AO	Analog output
	AIO	Analog bi-direction
	DI	Digital input
	DO	Digital output
	DIO	Digital bi-direction
	P	Power
	G	Ground
I/O Structure	TYPE0	Pull-up/down 3.63V tolerance
	TYPE1	Pull-up/down 5V tolerance
	TYPE2	Pull-up/down 5V tolerance SDIO characteristic support
	TYPE3	Pull-up/down 5V tolerance Analog input/output

**Table 5.1-3. MT5932 pin function description and power domain**

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
<b>Real-time clock</b>						
F5	RTC_EINT	DIO	TYPE0	Dedicated EINT input in RTC	-	VBAT_RTC
G4	XOUT	AIO	-	Input pin for 32K crystal	-	VBAT_RTC
G5	XIN	AIO	-	Input pin for 32K crystal	-	VBAT_RTC
<b>Wi-Fi radio interface</b>						
A6	XO	AI	-	DCXO 26/40MHz input	-	AVDD15_XO
B6	AVDD15_WF0_TRX	P	-	Wi-Fi TRX 1.5V power input	-	-
C6	AVDD33_WF0_G_TX	P	-	Wi-Fi TX 3.3V power input	-	-
D6	AVDD33_WF0_G_PA	P	-	Wi-Fi PA 3.3V power input ( $V_{RF}$ )	-	-
A7	AVSS15_WF0_LF	G	-	Wi-Fi LF ground	-	-
B7	AVSS15_WF0_TRX	G	-	Wi-Fi TRX ground	-	-
D7	AVSS33_WF0_G_PA	G	-	Wi-Fi PA ground	-	-
D8	AVSS_WF0_G_BALUN	G	-	Wi-Fi BALUN ground	-	-
B8	WF0_G_RFIO	AIO	-	Wi-Fi RF IO	-	AVDD33_WF0_G_PA (AO)/ AVDD15_WF0_TRX (AI)
B5	AVDD15_XO	P	-	XO 1.5V power input	-	-
<b>Power management unit</b>						
H4	CHIP_EN	AI	-	Chip enable	-	VBAT_RTC
F4	EXT_PWR_EN	AO	-	PMU enable	-	VBAT_RTC
G3	AVDD33_MISC	P	-	Power input	-	-
H3	AVDD33_VRTC	P	-	RTC domain power supply ( $V_{RTC}$ )	-	-
H2	AVDD18_MLDO	P	-	MLDO power output for SF	-	-
G2	AVDD15_CLDO	P	-	CLDO power input from BUCK	-	-
F2	LXBK	P	-	SW node for BUCK	-	-
D1	AVSS33_MISC	G	-	GND of	-	-

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
				AVDD33_MISC		
D2	AVSS33_MISC	G	-	GND of AVDD33_MISC	-	-
E2	AVSS33_BUCK	G	-	GND of AVDD33_BUCK	-	-
E1	AVDD15_V2P5NA	P	-	Internal power of BUCK	-	-
G1	AVDD33_BUCK	P	-	Buck power input (V <sub>BAT</sub> )	-	-
H1	AVDD12_CLDO	P	-	CLDO power output for core power	-	-
<b>General purpose I/O</b>						
A4	GPIO0	DIO	TYPE3	General purpose input/output, Pin 0	<ul style="list-style-type: none"> <li>• UART (1)</li> <li>• I2C (1)</li> <li>• I2S Master/Slave</li> <li>• Cortex-M4 JTAG</li> <li>• External front-end support</li> <li>• BT_PRI1</li> <li>• PWM (0)</li> </ul>	DVDD_IO_1
B4	GPIO1	DIO	TYPE3	General purpose input/output, Pin 1	<ul style="list-style-type: none"> <li>• UART (1)</li> <li>• I2C (1)</li> <li>• I2S Master/Slave</li> <li>• Cortex-M4 JTAG</li> <li>• External front-end support</li> <li>• BT_PRI3</li> <li>• PWM (1)</li> </ul>	DVDD_IO_1
C3	GPIO2	DIO	TYPE3	General purpose input/output, Pin 2	<ul style="list-style-type: none"> <li>• UART (1)</li> <li>• PWM (0)</li> <li>• I2S Master/Slave</li> <li>• Cortex-M4 JTAG</li> <li>• CLK00</li> <li>• BT_PRI0</li> <li>• External front-end support</li> </ul>	DVDD_IO_1
C4	GPIO3	DIO	TYPE3	General purpose input/output, Pin 3	<ul style="list-style-type: none"> <li>• UART (1)</li> <li>• PWM (1)</li> <li>• I2S Master/Slave</li> <li>• Cortex-M4 JTAG</li> </ul>	DVDD_IO_1

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
E5	GPIO4	DIO	TYPE1	General purpose input/output, Pin 4	<ul style="list-style-type: none"> <li>• External front-end support</li> <li>• SPI Slave (0)</li> <li>• SPI Master (0)</li> <li>• Cortex-M4 JTAG</li> <li>• External front-end support</li> </ul>	DVDD_IO_1
H7	GPIO11	DIO	TYPE2	General purpose input/output, Pin 11	<ul style="list-style-type: none"> <li>• PWM (3)</li> <li>• UART (2)</li> <li>• SDIO Master</li> <li>• SDIO Slave</li> <li>• CLK02</li> <li>• External front-end support</li> <li>• I2S Master/Slave</li> </ul>	DVDD_IO_0
H8	GPIO12	DIO	TYPE2	General purpose input/output, Pin 12	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• UART (2)</li> <li>• SDIO Master</li> <li>• SDIO Slave</li> <li>• External front-end support</li> <li>• I2S Master/Slave</li> </ul>	DVDD_IO_0
H6	GPIO13	DIO	TYPE2	General purpose input/output, Pin 13	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• UART (2)</li> <li>• SDIO Master</li> <li>• SDIO Slave</li> <li>• CLK04</li> <li>• I2S Master/Slave</li> </ul>	DVDD_IO_0
G7	GPIO14	DIO	TYPE2	General purpose input/output, Pin 14	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• I2S Master/Slave</li> <li>• SDIO Master</li> <li>• SDIO Slave</li> <li>• PWM (4)</li> <li>• CLK04</li> </ul>	DVDD_IO_0
G6	GPIO15	DIO	TYPE2	General purpose input/output, Pin 15	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• I2S Master/Slave</li> <li>• SDIO Master</li> </ul>	DVDD_IO_0

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
					<ul style="list-style-type: none"> <li>• SDIO Slave</li> <li>• I2C (1)</li> <li>• PWM (3)</li> </ul>	
F7	GPIO16	DIO	TYPE2	General purpose input/output, Pin 16	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• I2S Master/Slave</li> <li>• SDIO Master</li> <li>• SDIO Slave</li> <li>• I2C (1)</li> </ul>	DVDD_IO_0
F8	GPIO17	DIO	TYPE3	General purpose input/output, Pin 17	<ul style="list-style-type: none"> <li>• SPI Slave (1)</li> <li>• SPI Master (1)</li> <li>• I2S Master/Slave</li> <li>• PWM (5)</li> <li>• CLK03</li> <li>• AUXADC0</li> <li>• BT_PRI0</li> </ul>	DVDD_IO_0
E6	GPIO19	DIO	TYPE3	General purpose input/output, Pin 19	<ul style="list-style-type: none"> <li>• PMU_GOTO_SLEEP</li> <li>• I2S Master/Slave</li> <li>• CLK04</li> <li>• I2C (1)</li> <li>• ZCV</li> <li>• CLK03</li> <li>• PMU_RGU_RSTB</li> </ul>	DVDD_IO_0
E7	GPIO20	DIO	TYPE3	General purpose input/output, Pin 20	<ul style="list-style-type: none"> <li>• UART (0)</li> <li>• I2C (1)</li> <li>• PWM (5)</li> <li>• AUXADC2</li> <li>• WIFI_EXT_CLK</li> </ul>	DVDD_IO_0
<b>External SF I/O</b>						
A1	SFSCCK	DIO	TYPE0	External flash clock output	-	DVDD_MLDO
A2	SFSOUT	DIO	TYPE0	External flash data input	-	DVDD_MLDO
B2	SFSCS0	DIO	TYPE0	External flash select output	-	DVDD_MLDO
C2	SFSWP	DIO	TYPE0	External flash write protect	-	DVDD_MLDO

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
B3	SFSHOLD	DIO	TYPE0	External flash data hold output	-	DVDD_MLDO
C1	SFSIN	DIO	TYPE0	External flash data output	-	DVDD_MLDO
<b>Digital IO power</b>						
B1	DVDD_IO_1	P	-	Power input of GPIO left group (V <sub>IO_1</sub> )	-	-
G8	DVDD_IO_0	P	-	Power input of GPIO right group (V <sub>IO_0</sub> )	-	-
A3	DVDD_MLDO	P	-	Power input of SF/EMI group	-	-
<b>Digital core power</b>						
C5	DVDD_CORE	P	-	Core power	-	-
D5	DVDD_CORE	P	-	Core power	-	-
F6	DVDD_CORE	P	-	Core power	-	-
<b>Digital ground</b>						
D3	DVSS	G	-	Ground	-	-
D4	DVSS	G	-	Ground	-	-
E3	DVSS	G	-	Ground	-	-
F3	DVSS	G	-	Ground	-	-

## 5.2. MT5932 pin multiplexing

The MT5932 platform offers 14 GPIO pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on the pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count. To facilitate application use, the software can configure which clock to send outside the chip. There are four clock-out ports embedded in 14 GPIO pins, and each clock-out can be programmed to output an appropriate clock source. In addition, when two GPIOs function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

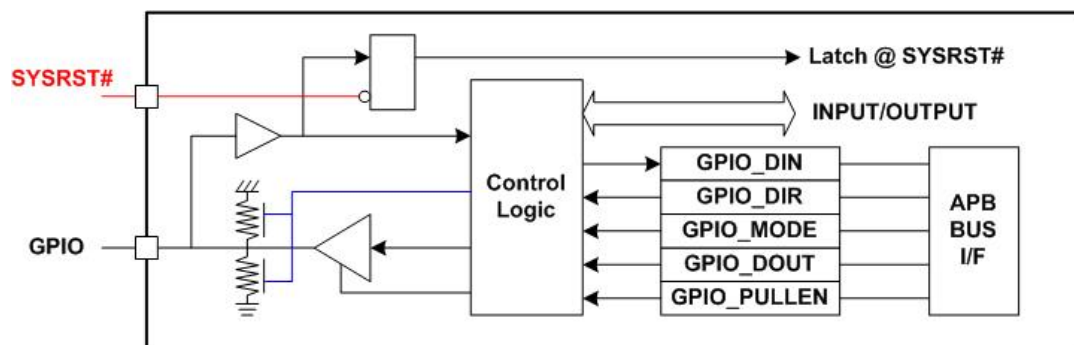


Figure 5.2-1. GPIO block diagram

Peripheral functions and signals are listed in Table 5.2-1 are shown in the table below. SDIO, SPI Master and SPI Slave peripheral interfaces can support signal groups allocated on different pins.

Table 5.2-1. Peripheral functions and signals

Alternate Function	Signals
SDIO Master	MA_MC0_CK MA_MC0_CM0 MA_MC0_DA0 MA_MC0_DA1 MA_MC0_DA2 MA_MC0_DA3
SDIO Slave	SLV_MC0_CK SLV_MC0_CM0 SLV_MC0_DA0 SLV_MC0_DA1 SLV_MC0_DA2 SLV_MC0_DA3
UART (0)	URXD0 UTXD0 U0RTS U0CTS
UART (1)	URXD1 UTXD1 U1RTS U1CTS
UART (2)	URXD2 UTXD2 U2RTS U2CTS
I2C (1)	SCL1 SDA1
I2S Master/Slave	I2S_RX I2S_TX I2S_WS I2S_CK

Alternate Function	Signals
I2S Master/Slave	TDM_RX TDM_TX TDM_WS TDM_CK TDM_MCLK
SPI Master (0)	SPIMST_A_SCK SPIMST_A_CS SPIMST_A_SIO0 SPIMST_A_SIO1 SPIMST_A_SIO2 SPIMST_A_SIO3
SPI Master (1)	SPIMST_B_SCK SPIMST_B_CS SPIMST_B_SIO0 SPIMST_B_SIO1 SPIMST_B_SIO2 SPIMST_B_SIO3
SPI Slave (0)	SPISLV_A_SCK SPISLV_A_CS SPISLV_A_SIO0 SPISLV_A_SIO1 SPISLV_A_SIO2 SPISLV_A_SIO3
SPI Slave (1)	SPISLV_B_SCK SPISLV_B_CS SPISLV_B_SIO0 SPISLV_B_SIO1 SPISLV_B_SIO2 SPISLV_B_SIO3
PWM (0)	PWM0
PWM (1)	PWM1
PWM (2)	PWM2
PWM (3)	PWM3
PWM (4)	PWM4
PWM (5)	PWM5
AUXADC	AUXADCIN_0 AUXADCIN_2 AUXADCIN_3
Cortex-M4 JTAG	JTDI JTMS JTCK JTRST_B JTDO



Alternate Function	Signals
External front-end support	WIFI_ANT_SEL0 WIFI_ANT_SEL1 WIFI_ANT_SEL2 WIFI_ANT_SEL3 WIFI_ANT_SEL4

**Table 5.2-2. PinMux description**

Ball Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7	Aux Func.8	Aux Func.9	Aux Func.10
GPIO_0	GPIO0	EINT0		U1RTS	SCL1	I2S_RX	JTDI		WIFI_ANT_S EL0	BT_PRI1	PWM0
GPIO_1	GPIO1	EINT1		U1CTS	SDA1	I2S_TX	JTMS		WIFI_ANT_S EL1	BT_PRI3	PWM1
GPIO_2	GPIO2	EINT2		URXD1	PWM0	I2S_WS	JTCK	CLKO0		BT_PRI0	WIFI_ANT_S EL4
GPIO_3	GPIO3	EINT3		UTXD1	PWM1	I2S_CK	JTRST_B			WIFI_ANT_S EL2	I2S_CK
GPIO_4	GPIO4	SPISLV_A_SI O2	SPIMST_A_SI O2	EINT4		I2S_MCLK	JTDO			WIFI_ANT_S EL3	I2S_MCLK
GPIO_11	GPIO11	EINT11	PWM3	URXD2	MA_MC0_CK	SLV_MC0_CK	CLKO2			WIFI_ANT_S EL0	I2S_RX
GPIO_12	GPIO12	SPISLV_B_SI O3	SPIMST_B_SI O3	UTXD2	MA_MC0_C M0	SLV_MC0_C M0	EINT12			WIFI_ANT_S EL1	I2S_TX
GPIO_13	GPIO13	SPISLV_B_SI O2	SPIMST_B_SI O2	U2RTS	MA_MC0_D A0	SLV_MC0_D A0	CLKO4		EINT13		I2S_WS
GPIO_14	GPIO14	SPISLV_B_SI O1	SPIMST_B_SI O1	TDM_RX	MA_MC0_D A1	SLV_MC0_D A1	PWM4		EINT14		CLKO4
GPIO_15	GPIO15	SPISLV_B_SI O0	SPIMST_B_SI O0	TDM_TX	MA_MC0_D A2	SLV_MC0_D A2	SCL1		EINT15		PWM3
GPIO_16	GPIO16	SPISLV_B_SC K	SPIMST_B_S CK	TDM_WS	MA_MC0_D A3	SLV_MC0_D A3	SDA1		EINT16		
GPIO_17	GPIO17	SPISLV_B_CS	SPIMST_B_C S	TDM_CK	PWM5	CLKO3	AUXADC0		EINT17		BT_PRI0
GPIO_19	GPIO19	URXD0	EINT19	SCL1		PWM5	AUXADC2	WIFI_EXT_CL K			
GPIO_20	GPIO20	UTXD0	EINT20				AUXADC3				

## 6. Electrical Characteristics

### 6.1. Absolute maximum ratings

**Table 6.1-1. Absolute maximum ratings for power supply**

Symbol or pin name	Description	Min.	Max.	Unit
AVDD33_MISC	Power input	-0.3	3.63	V
AVDD33_VRTC	RTC domain power supply ( $V_{RTC}$ )	-0.3	3.63	V
AVDD18_MLDO	MLDO power output for SF	-0.3	3.63	V
AVDD15_CLDO	CLDO power input from BUCK	-0.3	1.595	V
AVDD33_BUCK	Buck power input ( $V_{BAT}$ )	-0.3	3.63	V
AVDD12_CLDO	CLDO power output for core power	-0.3	1.265	V

**Table 6.1-2. Absolute maximum ratings for I/O power supply**

Symbol or pin name	Description	Min.	Typ.1	Typ.2	Max.	Unit
DVDD_IO_0	Power supply for GPIO group 0	1.62	1.8	3.3	3.63	V
DVDD_IO_1	Power supply for GPIO group 1	1.62	1.8	3.3	3.63	V
DVDD_MLDO	Power supply for SF/EMI IO 1.8V group	1.62	1.8	-	1.98	V

**Table 6.1-3. Absolute maximum ratings for voltage input**

Symbol or pin name	Description	Min.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	-0.3	3.63	V
VIN1	Digital input voltage for IO Type 1	-0.3	5.5	V
VIN2	Digital input voltage for IO Type 2	-0.3	5.5	V
VIN3	Digital input voltage for IO Type 3	-0.3	5.5	V

**Table 6.1-4. Absolute maximum ratings for storage temperature**

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

### 6.2. Operating conditions

#### 6.2.1. General operating conditions

**Table 6.2-1. General operating conditions**

Item	Description	Condition	Min.	Typ.	Max.	Unit
F <sub>CPU</sub>	Internal Cortex-M4 & TCM & Cache clock	VCORE = 1.15V	0	-	192	MHz

Item	Description	Condition	Min.	Typ.	Max.	Unit
F <sub>MEMS</sub>	Internal memory (SFC and EMI) related AHB and APB clock. Synchronous with F <sub>CPU</sub> .	V <sub>CORE</sub> = 1.15V	0	-	96	MHz

**Table 6.2-2. Recommended operating conditions for power supply**

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD33_MISC	Power input	2.97	3.3	3.63	V
AVDD33_VRTC	RTC domain power supply (V <sub>RTC</sub> )	1.62	3.3	3.63	V
AVDD18_MLDO	MLDO power output for SF	1.62	1.8	1.98	V
AVDD15_CLDO	CLDO power input from BUCK	1.305	1.45	1.595	V
AVDD33_BUCK	Buck power input (V <sub>BAT</sub> )	2.97	3.3	3.63	V
AVDD12_CLDO	CLDO power output for core power	1.035	1.15	1.265	V

**Table 6.2-3. Recommended operating conditions for voltage input**

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	-0.3	-	DVDIO+0.3	V
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V

**Table 6.2-4. Recommended operating conditions for operating temperature**

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
T <sub>c</sub>	Operating temperature	-30	-	85	°C

## 6.2.2. Input or output port characteristics

**Table 6.2-5. Electrical characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH0	Digital high input current for IO Type 0	<ul style="list-style-type: none"> <li>PU/PD disabled</li> <li>DVDIO = 3.3, 2.8, 1.8V,</li> <li>DVDIO * 0.65 &lt; VIN0 &lt; DVDIO + 0.3V</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>PU enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>DVDIO * 0.75 &lt; VIN0 &lt; DVDIO</li> </ul>	-35	-	5	μA
		<ul style="list-style-type: none"> <li>PD enabled</li> </ul>	7	-	70	μA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		<ul style="list-style-type: none"> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>DVDIO * 0.75 &lt; VIN0 &lt; DVDIO</li> </ul>				
DIIL0	Digital low input current for IO Type 0	<ul style="list-style-type: none"> <li>PU/PD disabled</li> <li>DVDIO = 3.3/2.8/1.8V,</li> <li>-0.3V &lt; VIN0 &lt; DVDIO*0.35</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>PU enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>0 &lt; VIN0 &lt; DVDIO * 0.25</li> </ul>	-60	-	6	μA
		<ul style="list-style-type: none"> <li>PD enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>0 &lt; VIN0 &lt; DVDIO * 0.25</li> </ul>	-5	-	40	μA
DIOH0	Digital high output current for IO Type 0	<ul style="list-style-type: none"> <li>DVOH = 2.805V</li> <li>DVDIO = 3.3V</li> <li>Max. driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>DVOH = 2.38V</li> <li>DVDIO = 2.8V</li> <li>Max. driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>DVOH = 1.53V</li> <li>DVDIO = 1.8V</li> <li>Max. driving mode</li> </ul>	8	-	-	mA
DIOL0	Digital low output current for IO Type 0	<ul style="list-style-type: none"> <li>DVOL = 0.495V</li> <li>DVDIO = 3.3V</li> <li>Max. driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>DVOL = 0.442V</li> <li>DVDIO = 2.8V</li> <li>Max. driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>DVOL = 0.27V</li> <li>DVDIO = 1.8V</li> <li>Max. driving mode</li> </ul>	8	-	-	mA
DRPU0	Digital I/O pull-up resistance for IO Type 0	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 0V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0</li> </ul>	40	85	190	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V</li> </ul>	80	160	320	kΩ
DRPD0	Digital I/O pull-down resistance for IO Type 0	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V</li> </ul>	80	160	320	kΩ
DVOH0	Digital output high voltage for IO Type 0	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	2.4	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	1.89	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	1.215	-	-	V
DVOL0	Digital output low voltage for IO Type 0	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	-	-	0.495	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	-	-	0.42	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	-	-	0.27	V
DIIH1	Digital high input current for IO Type 1	<ul style="list-style-type: none"> <li>PU/PD disabled</li> <li>DVDIO = 3.3, 2.8, 1.8V,</li> <li>DVDIO * 0.65 &lt; VIN1 &lt; DVDIO + 0.3V</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>4.5V &lt; VIN1 &lt; 5.5V</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>PU enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>DVDIO * 0.75 &lt; VIN1 &lt; DVDIO</li> </ul>	-35		5	μA
		<ul style="list-style-type: none"> <li>PD enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>DVDIO * 0.75 &lt; VIN1 &lt; DVDIO</li> </ul>	7		70	μA
DIIL1	Digital low input current for IO Type 1	<ul style="list-style-type: none"> <li>PU/PD disabled</li> <li>DVDIO = 3.3, 2.8, 1.8V,</li> <li>-0.3V &lt; VIN1 &lt; DVDIO * 0.35</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>PU enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>0 &lt; VIN1 &lt; DVDIO * 0.25</li> </ul>	-60	-	-6	μA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		<ul style="list-style-type: none"> <li>PD enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li>0 &lt; VIN1 &lt; DVDIO * 0.25</li> </ul>	-5	-	40	μA
DIOH1	Digital high output current for IO Type 1	<ul style="list-style-type: none"> <li>DVOH = 2.805V</li> <li>DVDIO = 3.3V</li> <li>Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>DVOH = 2.38V</li> <li>DVDIO = 2.8V</li> <li>Max. driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>DVOH = 1.53V</li> <li>DVDIO = 1.8V</li> <li>Maximum driving mode</li> </ul>	8	-	-	mA
DIOL1	Digital low output current for IO Type 1	<ul style="list-style-type: none"> <li>DVOL = 0.495V</li> <li>DVDIO = 3.3V</li> <li>Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>DVOL = 0.442V</li> <li>DVDIO = 2.8V</li> <li>Maximum driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>DVOL = 0.27V</li> <li>DVDIO = 1.8V</li> <li>Maximum driving mode</li> </ul>	8	-	-	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 0V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V</li> </ul>	80	160	320	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V</li> </ul>	40	85	190	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V</li> </ul>	80	160	320	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DVOH1	Digital output high voltage for IO Type 1	• DVDIO = 3.3V	2.4	-	-	V
		• DVDIO = 2.8V	1.89	-	-	V
		• DVDIO = 1.8V	1.215	-	-	V
DVOL1	Digital output low voltage for IO Type 1	• DVDIO = 3.3V	-	-	0.495	V
		• DVDIO = 2.8V	-	-	0.42	V
		• DVDIO = 1.8V	-	-	0.27	V
DIIH2	• Digital high input current for IO Type 2	• PU/PD disabled • DVDIO = 3.3, 2.8, 1.8V, • DVDIO * 0.65 < VIN2 < DVDIO + 0.3V	-5	-	5	μA
		• DVDIO = 3.3V • 4.5V < VIN2 < 5.5V	-5	-	5	μA
		• PU enabled, RSEL1 • DVDIO = 3.3, 2.8, 1.8V • DVDIO * 0.75 < VIN2 < DVDIO	-60	-	5	μA
		• PU enabled, RSEL2 • DVDIO = 3.3, 2.8, 1.8V • DVDIO * 0.75 < VIN2 < DVDIO	-120	-	5	μA
		• PD enabled, RSEL1 • DVDIO = 3.3, 2.8, 1.8V • DVDIO * 0.75 < VIN2 < DVDIO	10	-	110	μA
		• PD enabled, RSEL2 • DVDIO = 3.3, 2.8, 1.8V • DVDIO * 0.75 < VIN2 < DVDIO	20	-	220	μA
DIIL2	Digital low input current for IO Type 2	• PU/PD disabled, • DVDIO = 3.3, 2.8, 1.8V, • -0.3V < VIN2 < DVDIO * 0.65	-5	-	5	μA
		• PU enabled, RSEL1 • DVDIO = 3.3, 2.8, 1.8V • 0 < VIN2 < DVDIO *	-100	-	-10	μA



Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		0.25				
		<ul style="list-style-type: none"> <li>• PU enabled, RSEL2</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• <math>0 &lt; VIN2 &lt; DVDIO * 0.25</math></li> </ul>	-200	-	-20	μA
		<ul style="list-style-type: none"> <li>• PD enabled, RSEL1</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• <math>0 &lt; VIN2 &lt; DVDIO * 0.25</math></li> </ul>	-5	-	60	μA
		<ul style="list-style-type: none"> <li>• PD enabled, RSEL2</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• <math>0 &lt; VIN2 &lt; DVDIO * 0.25</math></li> </ul>	-5	-	120	μA
DIOH2	Digital high output current for IO Type 2	<ul style="list-style-type: none"> <li>• DVOH = 2.805V</li> <li>• DVDIO = 3.3V</li> <li>• Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOH = 2.38V</li> <li>• DVDIO = 2.8V</li> <li>• Maximum driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOH = 1.53V</li> <li>• DVDIO = 1.8V</li> <li>• Maximum driving mode</li> </ul>	8	-	-	mA
DIO L2	Digital low output current for IO Type 2	<ul style="list-style-type: none"> <li>• DVOL = 0.495V</li> <li>• DVDIO = 3.3V</li> <li>• Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOL = 0.42V</li> <li>• DVDIO = 2.8V</li> <li>• Maximum driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOL = 0.27V</li> <li>• DVDIO = 1.8V</li> <li>• Maximum driving mode</li> </ul>	8	-	-	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	<ul style="list-style-type: none"> <li>• DVDIO = 3.3V</li> <li>• VIN = 0V, RSEL1</li> </ul>	25	45	100	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 0V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V, RSEL1</li> </ul>	50	100	200	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V, RSEL2</li> </ul>	25	50	100	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V, RSEL1</li> </ul>	50	100	200	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V, RSEL2</li> </ul>	25	50	100	kΩ
DVOH2	Digital output high voltage for IO Type 2	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	2.805	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	2.38	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	1.53	-	-	V
DVOL2	Digital output low voltage for IO Type 2	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	-	-	0.495	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	-	-	0.42	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	-	-	0.27	V
DIIH3	Digital high input current for IO Type 3	<ul style="list-style-type: none"> <li>PU/PD disabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li><math>DVDIO * 0.65 &lt; VIN3 &lt; DVDIO + 0.3V</math></li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li><math>4.5V &lt; VIN3 &lt; 5.5V</math></li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>PU enabled</li> <li>DVDIO = 3.3, 2.8, 1.8V</li> <li><math>DVDIO * 0.75 &lt; VIN3</math></li> </ul>	-35	-	5	μA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		< DVDIO				
		<ul style="list-style-type: none"> <li>• PD enabled</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• DVDIO * 0.75 &lt; VIN3 &lt; DVDIO</li> </ul>	7	-	70	μA
DIIL3	Digital low input current for IO Type 3	<ul style="list-style-type: none"> <li>• PU/PD disabled</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• -0.3V &lt; VIN3 &lt; DVDIO * 0.65</li> </ul>	-5	-	5	μA
		<ul style="list-style-type: none"> <li>• PU enabled</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• 0 &lt; VIN3 &lt; DVDIO * 0.25</li> </ul>	-60	-	-6	μA
		<ul style="list-style-type: none"> <li>• PD enabled</li> <li>• DVDIO = 3.3, 2.8, 1.8V</li> <li>• 0 &lt; VIN3 &lt; DVDIO * 0.25</li> </ul>	-5	-	40	μA
DIOH3	Digital high output current for IO Type 3	<ul style="list-style-type: none"> <li>• DVOH = 2.805V</li> <li>• DVDIO = 3.3V</li> <li>• Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOH = 2.38V</li> <li>• DVDIO = 2.8V</li> <li>• Maximum driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOH = 1.53V</li> <li>• DVDIO = 1.8V</li> <li>• Maximum driving mode</li> </ul>	8	-	-	mA
DIOL3	Digital low output current for IO Type 3	<ul style="list-style-type: none"> <li>• DVOL = 0.495V</li> <li>• DVDIO = 3.3V</li> <li>• Maximum driving mode</li> </ul>	24	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOL = 0.42V</li> <li>• DVDIO = 2.8V</li> <li>• Maximum driving mode</li> </ul>	20	-	-	mA
		<ul style="list-style-type: none"> <li>• DVOL = 0.27V</li> </ul>	8	-	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DRPU3	Digital I/O pull-up resistance for IO Type 3	<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>Maximum driving mode</li> </ul>				
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 0V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 0V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 0V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V, RSEL1</li> </ul>	50	100	200	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 0V, RSEL2</li> </ul>	25	50	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> <li>VIN = 3.3V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V, RSEL1</li> </ul>	25	45	100	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> <li>VIN = 2.8V, RSEL2</li> </ul>	10	23	50	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V, RSEL1</li> </ul>	50	100	200	kΩ
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> <li>VIN = 1.8V, RSEL2</li> </ul>	25	50	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	2.805	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	2.38	-	-	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	1.53	-	-	V
DVOL3	Digital output low voltage for IO Type 3	<ul style="list-style-type: none"> <li>DVDIO = 3.3V</li> </ul>	-	-	0.495	V
		<ul style="list-style-type: none"> <li>DVDIO = 2.8V</li> </ul>	-	-	0.42	V
		<ul style="list-style-type: none"> <li>DVDIO = 1.8V</li> </ul>	-	-	0.27	V

### 6.2.3. ESD electrical sensitivity

**Table 6.2-6. ESD electrical characteristics of MT5932**

ESD mode	Description	Pin name	Min.	Max.	Unit
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ESD mode	Description	Pin name	Min.	Max.	Unit
HBM	All pins exclude RF pins	JESD22-A114-F	-2000	2000	V
	RF pins	JESD22-A114-F	-1000	1000	V
CDM	All pins exclude RF pins	JESD22-C101-D	-500	500	V
	RF pins	JESD22-C101-D	-250	250	V

## 7. System Configuration

### 7.1. Mode selection

**Table 7.1-1. Mode selection table**

Mode Selection	Pin name	Description	Trapping condition
DCXO source frequency select	GPIO_17	GND : XO input is 26MHz (default) DVDD_IO_0 : XO input is 40MHz	Power-on reset
32kHz clock source select	GPIO_14	GND : 32kHz source is from external DVDD_IO_0 : 32kHz source is from internal (divided from 26/40MHz clock) (default)	Power-on reset
Boot with host interface (HIF_EN)	GPIO_4	GND : Boot with host interface enabled DVDD_IO_1 : Boot with host interface disabled (default)	Power-on reset
Host interface select (active if HIF_EN is enabled)	GPIO_13	(Active if HIF_EN = 1) GND : Host interface via SPI slave DVDD_IO_0 : Host interface via SDIO slave (default)	Power-on reset
Boot ROM bypass select	GPIO_16	GND : Boot up bypass boot ROM (directly jump to flash) DVDD_IO_0 : Boot up with boot ROM (default)	Power-on reset
JTAG pins fixed for use	GPIO_15	GND : JTAG pins fixed for JTAG use DVDD_IO_0 : JTAG pins as GPIO (configurable after boot up) (default)	Power-on reset
UART download	GPIO_12	GND : Enter UART download mode in Boot ROM DVDD_IO_0 : Skip UART download in Boot ROM (default)	Power-on reset or system reset

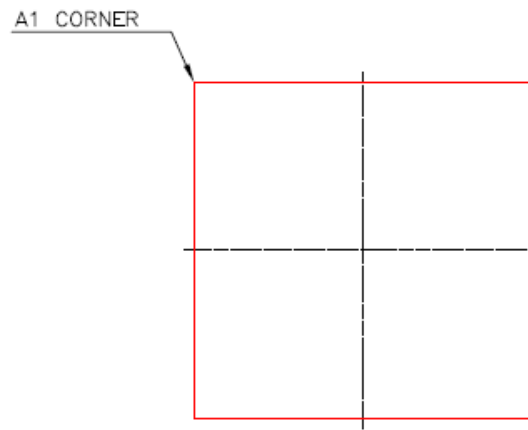
Note 1: Strapping resistors for default option are implemented as internal pull-down or internal pull-up 47kΩ.

Note 2: If non-default option is used, it is recommended to use pull-down or pull-up 10kΩ as external strapping resistors.

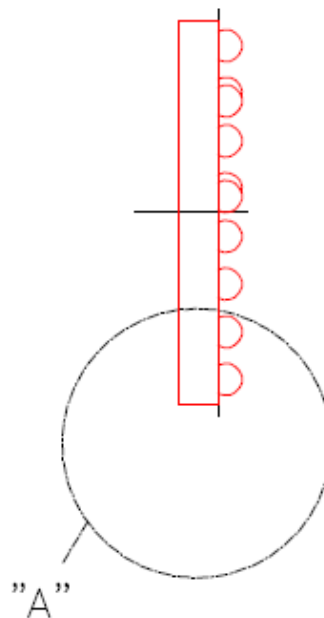
Note 3: SDIO master and slave interfaces are limited to 1-bit mode if the 32kHz source is external.

## 8. Package Description

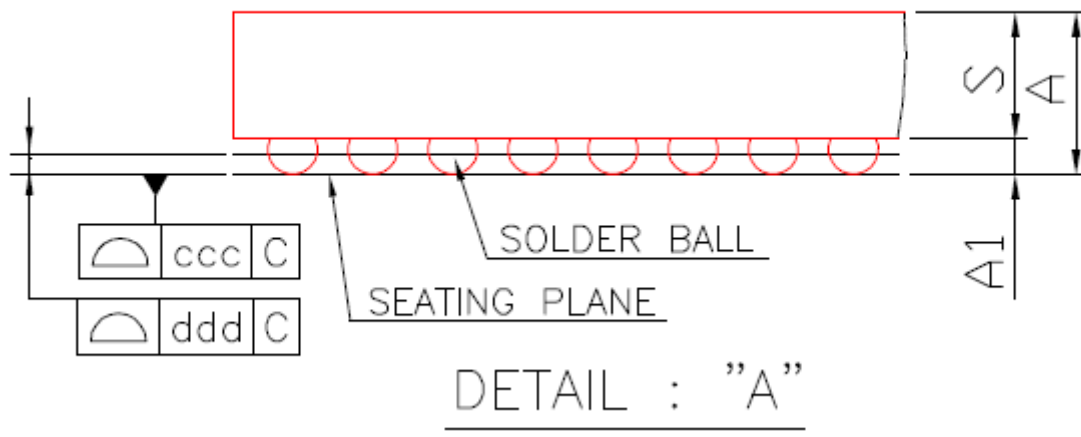
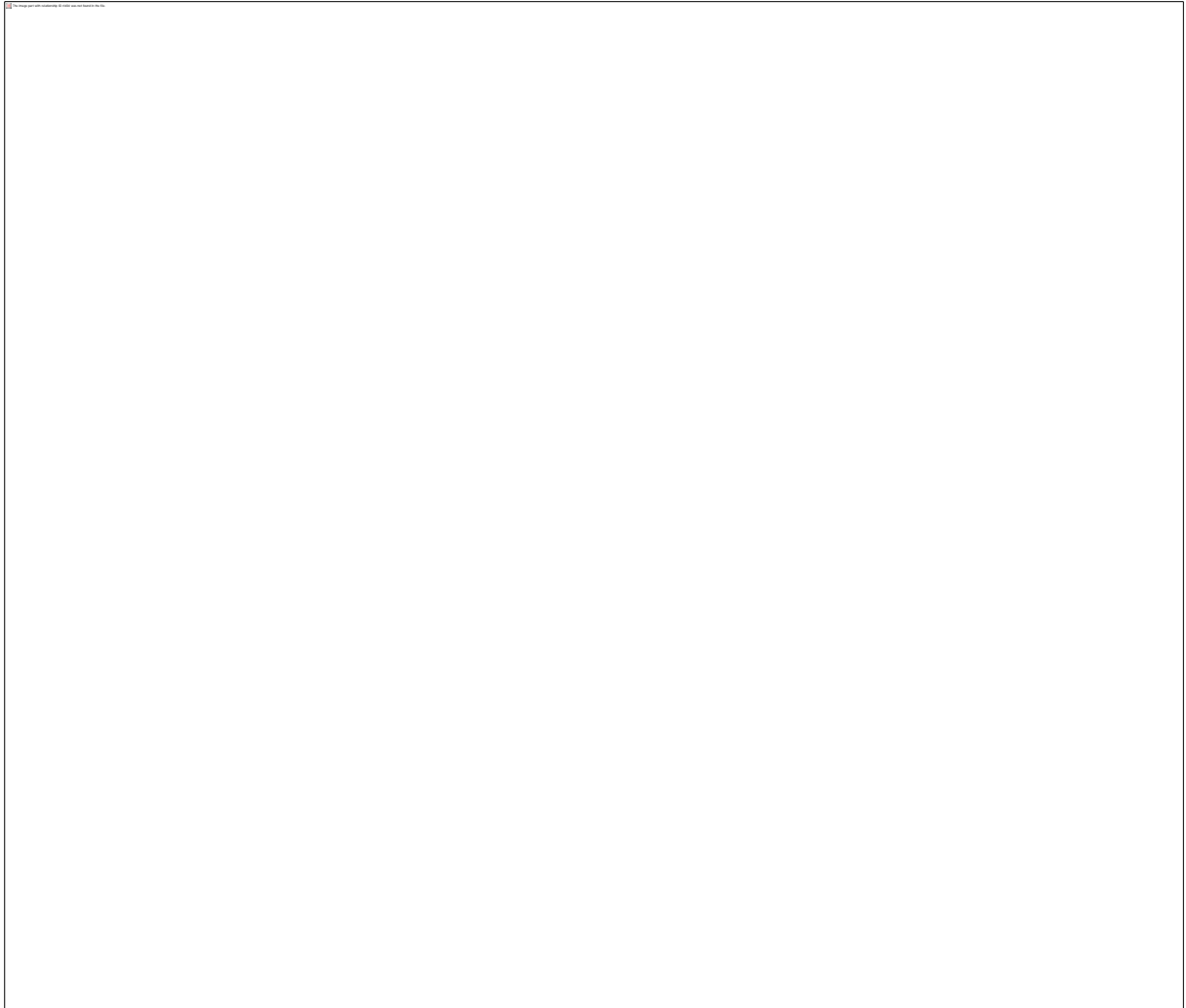
### 8.1. MT5932 mechanical data of the package



TOP VIEW



SIDE VIEW





Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX
Package Type			WLCSP		
Body Size	X	D	3.1824	3.2230	3.2480
	Y	E	3.1824	3.2230	3.2480
Ball Pitch	X	eD	0.400		
	Y	eE	0.400		
Total Thickness		A	0.490	0.530	0.570
Back Side Coating		A2	---		
Wafer Thickness		S	0.305	0.330	0.355
Ball Diameter			0.250		
Stand Off		A1	0.170	0.200	0.230
Ball Width		b	0.240	0.270	0.300
Package Edge Tolerance		aaa	+0.0250 -0.0406		
Coplanarity		ccc	0.030		
Ball Offset (Package)		ddd	0.050		
Ball Offset (Ball)		eee	0.015		
Ball Count		n	56		
Edge Ball Center to Center	X	D1	2.800		
	Y	E1	2.800		
Edge Ball Center to Package Edge	X	gD	0.2015		
	Y	gE	0.2105		

Figure 8.1-1. Outlines and dimensions of MT5932 WLCSP 3.223mm x 3.223mm x 0.53mm, 56-ball package

## 8.2. MT5932 thermal operating specifications

Table 8.2-1. MT5932 thermal operating specifications

Description	Value	Unit
Thermal resistance from device junction to package case	54.8	C/W

## 8.3. MT5932 lead-frame packaging

The MT5932 platform is provided in a lead-free package and meets RoHS requirements.

## 9. Ordering Information

### 9.1. MT5932 top marking definition

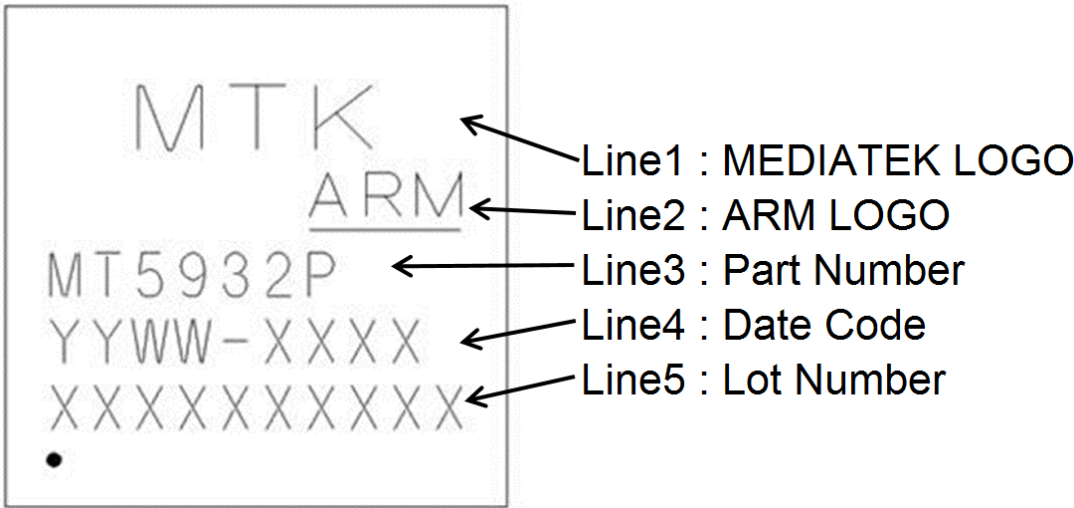


Figure 9.1-1. Mass production top marking of MT5932

Table 9.1-1. Ordering information

Product number	Package	Description
MT5932P	WLCSP	3.223mm x 3.223mm x 0.53mm 56-ball WLCSP with 0.4mm ball pitch