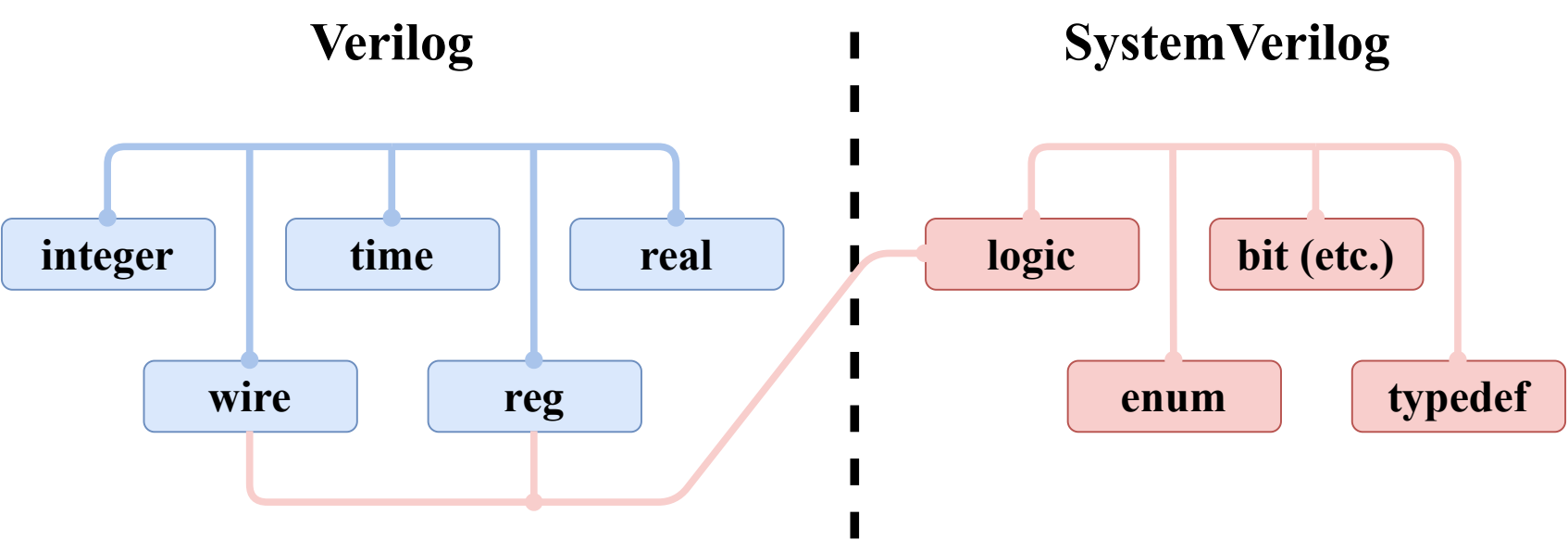
Verilog
SystemVerilog
integer
time
real
wire
reg
logic
bit (etc.)
enum
typedef