UM11225

NXP SE05x T=1 Over I^2C Specification

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User manual

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Document information

Information	Content
Keywords	I^2C T=1 ISO7816 SE05x
Abstract	Specification for the data link layer protocol T=1 over I^2C on the SE05x

Revision History

Revision history

Revision number	Date	Description
1.2	2020-12-10	Updated legal information
1.1	2020-01-08	Modifications: • Added definition for DPWT (Power Wake-Up Time) • Updated figure Figure 2 • Updated figure Figure 6 with STOP condition and MPOT • Updated figure Figure 9 • Updated figure Figure 11 • Update table Table 13 to remove IRQCT and SEAL (not supported by this product) • Updated chapter Section 2 add further statement to first item of the list. • Updated chapter Section 2.1.1.1 to remove statement about multiple NAD values • Updated chapter Section 2.1.1.2.3 to include further explanation on the Interface soft reset request and SE Chip reset request S-Block and add a new statement for WTX request • Updated chapter Section 2.4.2 • Updated chapter Section 3 to update list of characteristics for I²C • Updated chapter Section 3.1.1 to include statement that if I²C bus is free both lines SDA and SCL shall be HIGH • Added chapter SE I²C Default Values Section 3.1.1.4
1.0	2019-06-06	Initial version

1 Introduction

T=1 is a peer to peer, half duplex transmission protocol defined in ISO/IEC 7816-3. T=1 protocol usage is very common in the smart card domain. This document specifies how ISO/IEC 7816-3 T=1 protocol shall be used to transfer APDUs between a hosting device (HD) and a Secure Element (SE) using serial physical interfaces based on I^2C .

In view of the OSI protocol stack the serial physical interface I^2C , shall serve as physical layers. A customized ISO/IEC 7816-3 T=1 protocol shall be used as data link layer.

2 Data Link Layer (T=1)

This specification uses a Data Link Layer based on T=1 half duplex communication protocol as defined in ISO/IEC 7816-3. Proprietary extensions are added to ISO/IEC 7816-3 T=1 protocol to improve performance and to support additional features.

The main characteristics of this transmission protocol are the following:

- The transmission protocol starts with a first block transmitted by the hosting device (HD); it continues with alternating the right to transmit a block. Consequently, the HD shall always read the response of a previous request before issuing a new request to ensure the command and response sequence is always kept.
- A block is the smallest data unit that can be exchanged. A block may be used to convey:
  - Application data transparent to the transmission protocol.
  - Transmission control data including transmission error handling.
- The block structure allows checking the received block before processing the conveyed data.

The transmission protocol applies the principle of the OSI reference model. Three layers are defined:

1. The serial physical interface -I²C .
2. The data link layer based on T=1 half duplex communication protocol as defined in ISO/IEC 7816-3.
3. The application layer that processes commands, which involves the exchange of at least one block or chain of blocks in each direction.

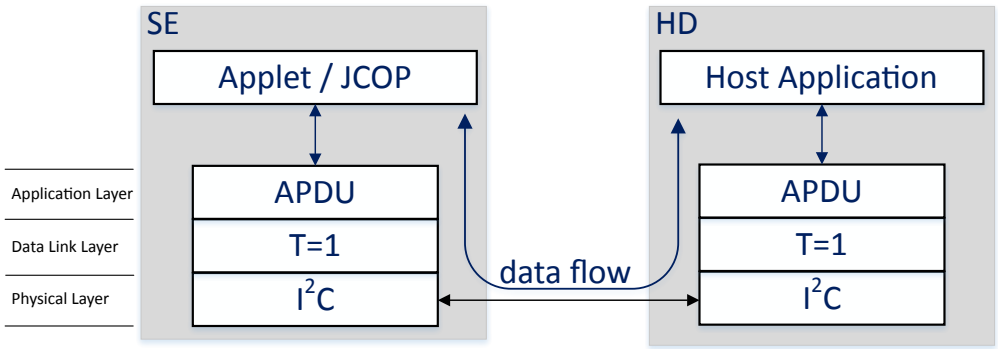

Figure 1. T=1 over I²C Communication Stack

Figure 1 shows data flow and communication layers in accordance to the OSI model of the T=1 communication stack over I²C interface.

- On the highest layer, the Application Layer, the ISO7816 APDU protocol is located. Applications and applets shall only use ISO7816 Application Protocol Data Units (APDUs) for communication.
- The T=1 protocol is the Data Link Layer. APDUs which shall be transmitted are split up in several frames and enveloped by a T=1 prologue and epilogue before they are passed to the next layer.
- The Physical Layer represents the serial physical interface layer – I²C . This layer is responsible for transmitting/receiving T=1 frame bytes.

2.1 T=1 Block Frame Format

The T=1 block frame consists of three fields as shown in Table 1.

1. **Prologue Field** consists of
   a. Node Address byte (NAD)
   b. Protocol Control Byte (PCB)
   c. Information Field Length (LEN)
2. **Information Field (INF)** consists of zero to LEN bytes. This field shall be present only if LEN is non-zero
3. **Epilogue Field** conveys the error detection code of the block. Two bytes cyclic redundancy code (CRC) is used for error detection as defined in [1].

Table 1. T=1 Frame Format

Prologue field (mandatory)			Information field (optional)	Epilogue field (mandatory)
NAD (1 byte)	PCB (1 byte)	LEN (1 byte)	INF (0 to LEN bytes)	CRC16 (2 bytes)

2.1.1 Prologue Field

One-byte LEN field is used in a 3-byte prologue and is used for blocks with 0 to 0xFE bytes in information field. Table 2 shows the 3-byte prologue field format.

Table 2. 3-Byte Prologue

3-byte Prologue field		
NAD (1 byte)	PCB (1 byte)	LEN (1 byte)

2.1.1.1 Node Address Byte (NAD)

The node address byte (NAD) identifies the source and the intended destination of the block. Bits 1 to 4 encode the source node address (SAD) and bits 5 to 8 encode the destination node address (DAD). Values '0xFF' and '0x00' are invalid for NAD. DAD and SAD shall never have the same value.

Table 3. NAD Format

Destination address (DAD)	Source address (SAD)
8 – 5	4 – 1

Table 4 lists proposed SAD and DAD values.

Table 4. SAD/DAD values

Communication Direction	DAD	SAD	NAD value
HD to SE	0x5	0xA	0x5A
SE to HD	0xA	0x5	0xA5

2.1.1.2 Protocol Control Byte (PCB)

The protocol control byte (PCB) conveys information required to control transmission. PCB indicates the block frame type and defines whether the block is an I-Block, a R-Block or a S-Block.

- An information block (I-Block) is used to convey information for use by the application layer.

- A receive ready block (R-Block) is used to convey a positive or negative acknowledgement.
- A supervisory block (S-Block) is used to exchange control information between the HD and the SE.

2.1.1.2.1 Coding Of I-Block PCB

Bit-8 of the PCB is set to 0 for an I-Block.

- Bit-7 encodes the send-sequence number denoted N(S). N(S) alternates between 1 and 0.
- Bit-6 is the more-data bit denoted M-bit. M-bit is used for I-Block chaining.
- Bits 5 to 1 are reserved for future use and shall be set to 0.

Table 5. Coding of I-Block PCB

Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1
0	N(S)	M	0	0	0	0	0

The chaining function allows the HD or the SE to transmit information (application data) longer than IFSC or IFSD. If the HD or the SE must transmit information longer than IFSC or IFSD respectively, it shall divide the information into pieces, each with length less than or equal to IFSC or IFSD and shall transmit each piece in a block using the chaining function.

The M-bit in PCB controls the chaining of I-Blocks. The value of the M-bit indicates the state of the I-Block.

- If M = 1, then the I-Block is chained to the next block, which shall be an I-Block.
- If M = 0, then the I-Block is not chained to the next block.

If the receiver correctly receives a more-data I-Block, then it shall transmit R(N(R)), where N(R) is set to N(S) of the expected I-Block.

2.1.1.2.2 Coding of R-Block PCB

Bits 8 and 7 of the PCB are set to 10b for an R-Block.

- Bit-5 encodes the expected sequence number denoted N(R).
- Bits 1 and 2 encode the error code. Refer to Table 7 for the supported error codes
- Remaining bits are reserved for future use and shall be set to 0.

Table 6. Coding of R-Block PCB

Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1
1	0	0	N(R)	0	0	Error code	

Table 7. R-Block Error codes

Bit-2	Bit-1	Error definition
0	0	Error-free acknowledgement
0	1	CRC error
1	0	Other error

R-Block is used to:

- Indicate error and request the sender to re-transmit the last block
- Acknowledge error-free reception of I-Block in case of chaining

2.1.1.2.3 Coding of S-Block PCB

Bits 8 and 7 of the PCB are set to 11b for an S-Block. Remaining bits are used to encode S-Block request/response commands as listed in Table 9.

Table 8. Generic S-Block Coding

Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1
1	1	Request/Response command					

Table 9. Coding of S-Block PCB

S-Block Command	Bits 1 to 6	INF	Description
RESYNC request	000000b	Absent. LEN = 0	Command to re-synchronize and reset I-Block sequence number to zero
RESYNC response	100000b		Response command to acknowledge RESYNC request
IFS request	000001b	IFS size	Command to request IFS length change. INF field holds the requested IFS size. Refer to Section 2.1.2.1 for details
IFS response	100001b		Response command to acknowledge IFS request
ABORT request	000010b	Absent. LEN = 0	Command to request chain abortion
ABORT response	100010b		Response command to acknowledge ABORT request
WTX request	000011b	integer multiplier of the BWT	Command to request Waiting Time extension
WTX response	100011b		Response command to acknowledge WTX request
Interface soft reset request	001111b	Absent. LEN = 0	Command to request for a soft reset of the logical connection.
Interface soft reset response	101111b	ATR bytes	Response command to acknowledge interface reset request. Refer to section Section 2.2 for details
End of APDU session request	000101b	Absent. LEN = 0	Command to indicate end of APDU session.
End of APDU session response	100101b		Response command to acknowledge end of APDU command. SE shall reset the protocol context and initiate power saving sequence after sending the command response.
SE Chip reset request	000110b	Absent. LEN = 0	Command to request reset of SE.
SE Chip reset response	100110b		Response command to acknowledge SE chip reset command. SE shall do a power reset after sending the command response.
Get ATR request	000111b	Absent. LEN = 0	Command to retrieve ATR bytes without resetting SE

Table 9. Coding of S-Block PCB*...continued*

S-Block Command	Bits 1 to 6	INF	Description
Get ATR response	100111b	ATR bytes	Response command to acknowledge Get ATR request. ATR bytes are send in INF field

Interface soft reset request S-Block command shall reset both protocol context and SE context with respect to the logical connection. SE shall send the command response with ATR bytes in INF field once the context reset is complete. HD shall not send this command as a response to WTX request. On soft reset, SE shall discard any pending response block on the logical connection. After Host has send the Interface soft reset request S-Block Host must ensure that for DMPOT SCL and SDA lines are in the default state HIGH.

HD shall use **End of APDU session request** S-Block command to indicate end of APDU session on the logical connection. SE shall reset the protocol context of the logical connection and may initiate power saving sequence after sending response to this command. SE shall wake up automatically if HD sends a T=1 block.

SE Chip reset request S-Block command shall reset SE chip. SE shall do self-reset once the response command is send to the HD. After Host has send the SE Chip reset request S-Block Host must ensure that for DPWT SCL and SDA lines are in the default state HIGH.

HD shall always respond to a **WTX request** with a WTX response.

2.1.1.3 Information Field Length (LEN)

The Information Field Length (LEN) byte(s) encodes the number of bytes in the information field of the block.

- The value ‘00’ encodes zero: INF is absent.
- One-byte LEN shall be used in Prologue field if the information field size is less than 0xFF bytes.

2.1.2 Information Field (INF)

The contents of the information field bytes depend upon the block type.

Table 10. Block Types

Block type	Information field usage
I-Block	Application data (C-APDU/R-APDU)
R-Block	Absent
S-Block	Refer to Table 9 for details

2.1.2.1 Information Field Size (IFS)

The Information Field Size (IFS) defines the maximum size of information field (INF) that a block can hold.

- IFSC defines the IFS of the SE
- IFSD defines the IFS of the HD

This protocol uses the same value for both IFSC and IFSD and both values are always in sync. ATR includes the maximum IFSC value of the SE.

SE shall use the maximum IFS size indicated in ATR on init. HD may use IFS request S-Block command to reduce the IFS size. SE shall acknowledge the request by IFS response S-Block command if the requested IFS size can be supported. SE shall reset the IFS to maximum value on soft reset.

IFS size of each logical connection shall be maintained separately. Soft reset command send on one logical connection shall reset the IFS of that logical connection only.

2.1.3 Epilogue Field (CRC)

The epilogue field conveys the error detection code of the block. Cyclic redundancy code (CRC) is used for error detection.

CRC shall be computed for all bytes in Prologue and INF fields.

2.2 Answer to Reset (ATR)

SE shall return ATR bytes as a response to Soft Reset request or Get ATR request S-Block command. INF bytes of interface soft reset/Get ATR S-Block response command shall hold the ATR bytes.

2.2.1 ATR – Common Structure

This section describes the common structure of the ATR, irrespective of the Physical Layer that is used.

Table 11. ATR – Common Structure

Name	Length	Description
PVER	1	Protocol Version. This version of the specification defines version '01' of the protocol. Higher versions shall be backward compatible with lower versions. Lower versions may miss some new capabilities of higher versions.
VID	5	Vendor ID according to [7816-4]
Length of DLLP	1	Length of Data Link Layer Parameters
DLLP	Var.	Data Link Layer Parameters: See Table 12
PLID	1	Physical Layer ID (always I²C so fixed to 2)
Length of PLP	1	Length of Physical Layer Parameters
PLP	Var.	Physical Layer Parameters: See Table 13
Length of HB	1	Length of Historical Bytes
HB	Var.	Historical Bytes

2.2.2 ATR – Specific Parameters for Data Link Layer

This section describes the parameters provided by the ATR for the Data Link Layer.

Table 12. ATR – Specific Parameters for Data Link Layer

Name	Length	Description
BWT	2	Block Waiting Time (in ms)
IFSC	2	Maximum Information Field Size of the SE (in bytes)

2.2.3 ATR – Specific Parameters for I²C Physical Layer

This section describes the parameters provided by the ATR when the I²C Physical Layer is used.

Table 13. ATR – Specific Parameters for I²C Physical Layer

Name	Length	Description
MCF	2	Maximal I²C Clock Frequency at which the SE may operate (in kHz)
Configuration	1	Method for SE Data Available that shall be used by the HD to detect that response data may be read from the SE: • b1-b3: RFU Support of the I²C High Speed Mode : • b4 = 0: HS mode not supported • b4 = 1: HS mode supported
MPOT	1	Minimum Polling Time (conditional to Polling Mode support) (in ms)
RFU	1	Not used for this product
RFU	2	Not used for this product
SEGT	2	Secure Element Guard Time (in µs)
WUT	2	Wake-Up Time (in µs): when receiving a Wake-Up Byte, time after which the SE is ready to receive a command.

2.3 Rules for Error-Free Operation

To ensure error free operation, this protocol shall follow below rules in addition to the rules listed in section 11.6.2 of [1].

2.3.1 Initialization

SE shall be in Receive state after power-on boot. The HD shall transmit the first block. First block shall be either an I-Block with N(S) = 0 denoted I(0, M), or an S-Block.

SE shall be in Send state after receiving S(Interface soft reset request) to send out the ATR, but shall reset the protocol context.

Note: It is recommended that HD should use S(Interface soft reset request) after power-on boot to ensure HD and SE are synchronized.

2.3.2 Processing

SE shall enter Process state on receiving the command block from the HD and shall exit Process state and go to Send state once the command is processed. When response is read out by the HD, SE shall go to Receive state again.

2.3.3 Acknowledgement

I-Blocks are acknowledged by sending the next I-Block.

Without chaining or at the last block of a chain, I(Na(S), 0) transmitted by A is implicitly acknowledged by I(Nb(S), M) transmitted by B.

With chaining, I(Na(S), 1) transmitted by A is acknowledged by R(Nb(R)) transmitted by B, with Nb(R) indicating the send-sequence number of the next expected block.

2.3.4 Waiting Time Extension

If the SE requires more than BWT to process the previously received command block, it shall transmit S(WTX request) S-Block command. The HD shall acknowledge by sending S(WTX response).The new processing time starts at the leading edge of the last character of S(WTX response).

SE shall transmit S(WTX request) for both I-Block and S-Block commands if the processing of the command requires more than BWT.

2.4 Error handling

This protocol shall follow below rules to handle errors in addition to the error handling rules listed in section 11.6.3 of [1].

2.4.1 Re-transmission

In case of a transmission error, where the HD either

- fails to receive an error-free block from SE, or
- repeatedly receives an R-Block from SE.

HD shall make a maximum of ten further attempts in succession by sending an R-Block to the SE or retransmitting the previously block.

HD shall transmit S(Interface soft reset request) after the maximum of retransmission attempts.

2.4.2 Error Recovery

If the SE in Send state cannot send the complete command response block to the HD, because HD sends a new command block, before reading complete command response block, SE shall go to Receive state to receive the new command block. Command response block shall be discarded. In this case SE behaves as if a S(Interface soft reset request) has been received..

3 Physical Interfaces

Serial physical interfaces, I^2C , shall be used by this protocol to transmit/receive protocol data frames.

- SE shall be in Receive state after power-on boot
- SE shall switch to Processing state once HD finishes to write the protocol command block.
- SE shall switch to Sending state once processing is done and SE is ready with protocol response block.
- SE shall switch back to Receive state once HD reads-out the response from SE
- After sending S(Interface soft reset request) HD shall ensure that for DMPOT both SDA and SCL are in default state HIGH.
- SE shall be in Send state after S(Interface soft reset request) to transmit ATR.

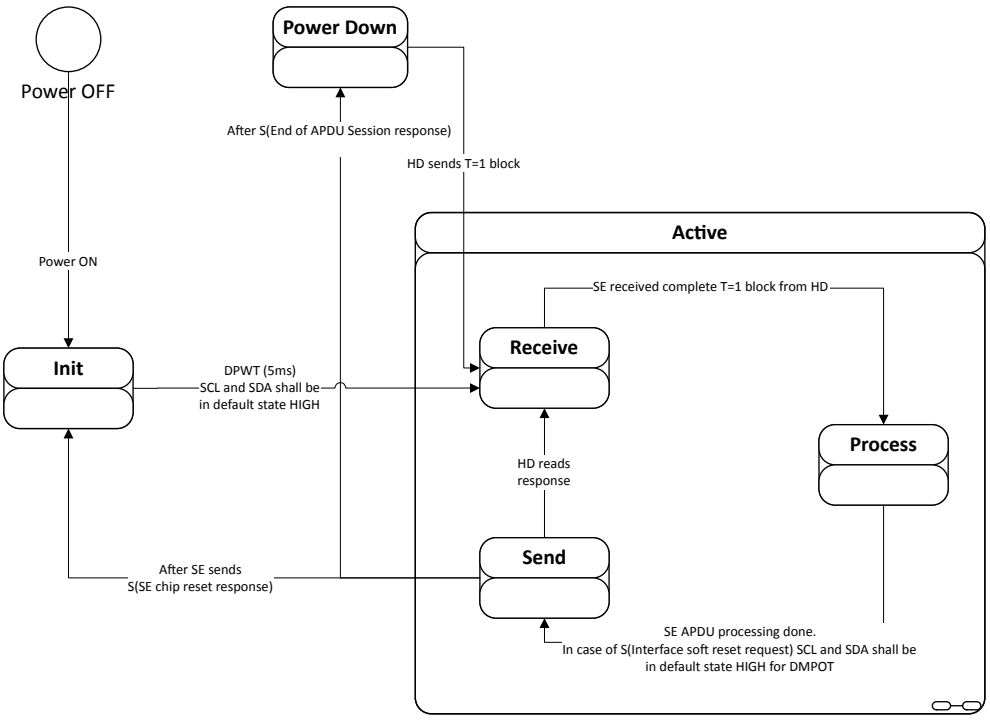

Figure 2. SE I^2C Slave State Machine

3.1 I^2C Interface

3.1.1 Description

I^2C Interface is a half-duplex communication interface. Only two wires are required to establish connection between one I^2C master and several slaves - clock line (SCL) and data line (SDA).

SE shall be the I^2C slave and HD shall act as the I^2C master.

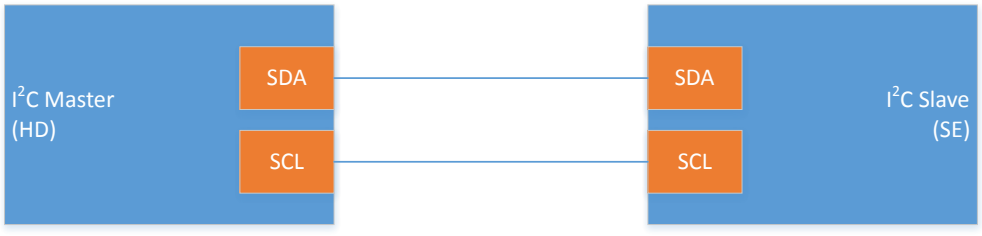

Figure 3. Simplified I²C Schematics

Note: When the bus is free or idle, both lines SCL and SDA shall be HIGH.

3.1.1.1 SE I²C Receive State

In receive state, SE is idle and is waiting for protocol command block from the HD. In this state SE shall:

- ACK I²C WRITE request from HD

Figure 4 shows the format of I²C frame that encapsulates T=1 protocol block frame from HD to SE. HD shall start the frame with I²C start condition and end with I²C stop condition. HD shall not use repeated start to send/receive any frame. HD shall send the complete T=1 frame in one fragment (in one I²C write cycle).

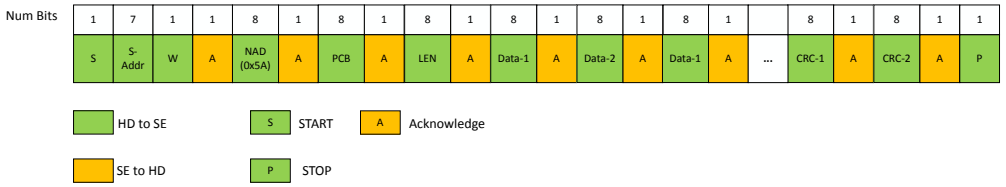

Figure 4. I²C Frame - HD to SE

HD shall follow below sequence to send a frame to the Slave:

1. Send I²C start condition
2. Send the I²C address of the slave with the R/W bit low (Write to Slave)
3. Send T=1 Block bytes
4. Send I²C stop condition

The HD may abort the frame transmission by sending Stop. On detecting Stop condition, SE shall switch to processing data state. In this state the frame will be analyzed. If the frame is not a valid T=1 frame, the error recovery mechanism gets activated which defines that the SE shall respond with an R-Block. Hence SE enters the Send state to send appropriate R-Block. The HD must read the R-Block following which SE enters the Receive state and waits for the next T=1 frame.

Figure 5. HD Sends Data to SE

3.1.1.2 SE I²C Processing State

SE shall switch from receiving state to processing state on receiving the I²C STOP sequence from the HD. In processing state:

- SE shall NACK any I²C WRITE request from HD
- SE shall NACK any I²C READ request from HD if busy

HD shall poll for the response from SE by sending a one byte read request to SE. HD shall ignore and retry if SE NACK the I²C read request. After receiving a NACK from the SE, HD shall wait MPOT before sending a new read request.

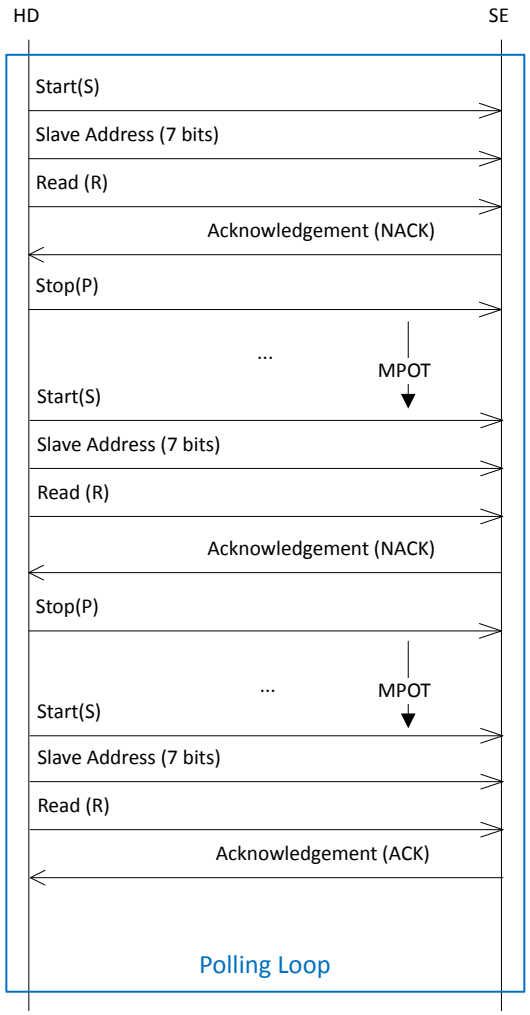

Figure 6. HD Polling SE for Response Data

3.1.1.3 SE I²C Send State

SE shall switch to send state once command processing is complete and is ready to send the protocol response command block. In send state:

- SE shall ACK I²C READ request from the HD.

Figure 7 shows the format of I²C frame that encapsulates T=1 protocol block frame from SE to HD. SE shall be in send state until all response bytes are read-out by the HD or the HD sends a new WRITE request. HD may read the response bytes in multiple I²C READ transactions (see Figure 8) or in a single I²C READ transaction. SE shall switch back to receive state once all response bytes are read-out by the HD. If HD sends a new WRITE request, SE shall switch to receive state and shall abort sending of response bytes.

If the HD reads more data bytes than SE has available, SE sends a IDLE byte (0xFF) to indicate that it does not have data to send.

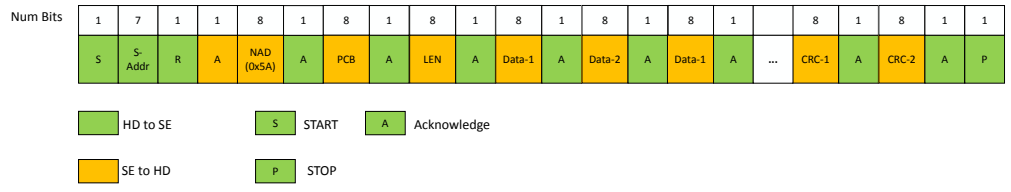

Figure 7. I²C frame - SE to HD

Figure 8. I²C multiple frames - SE to HD

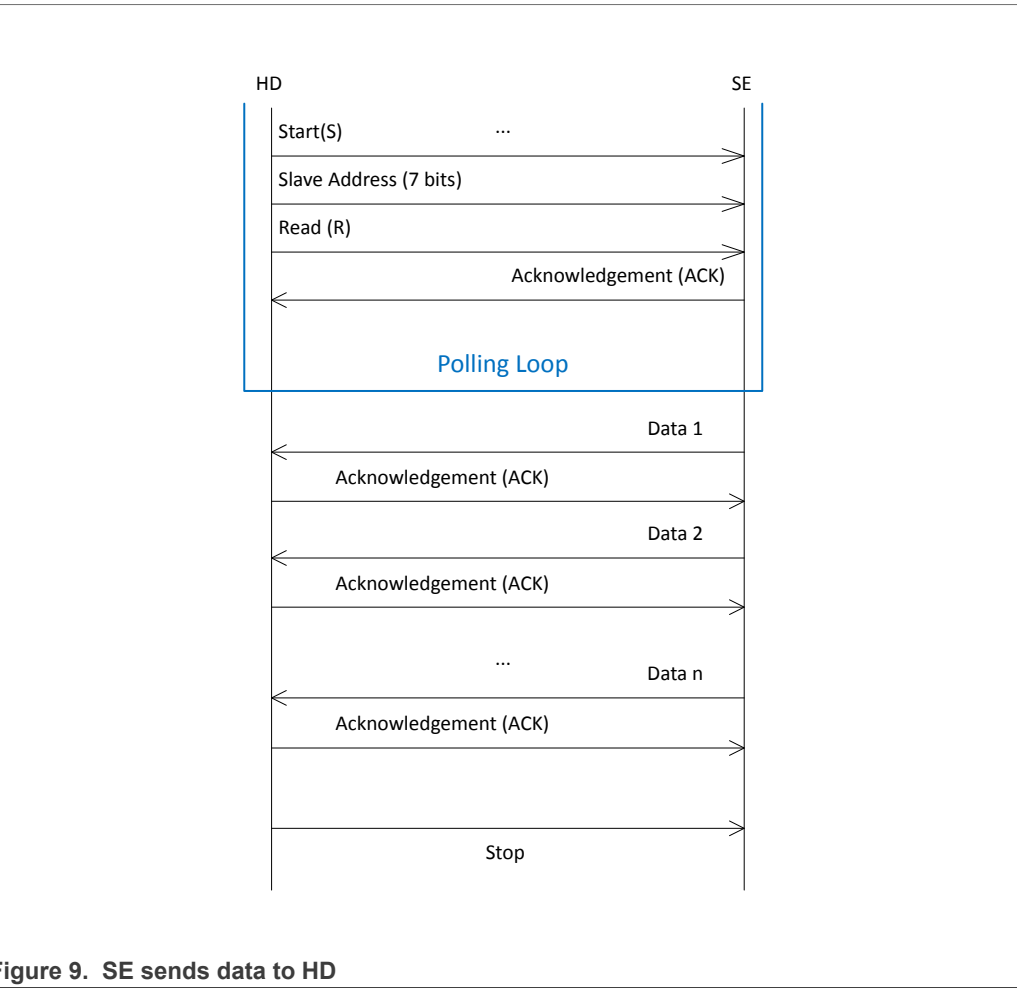

Figure 9. SE sends data to HD

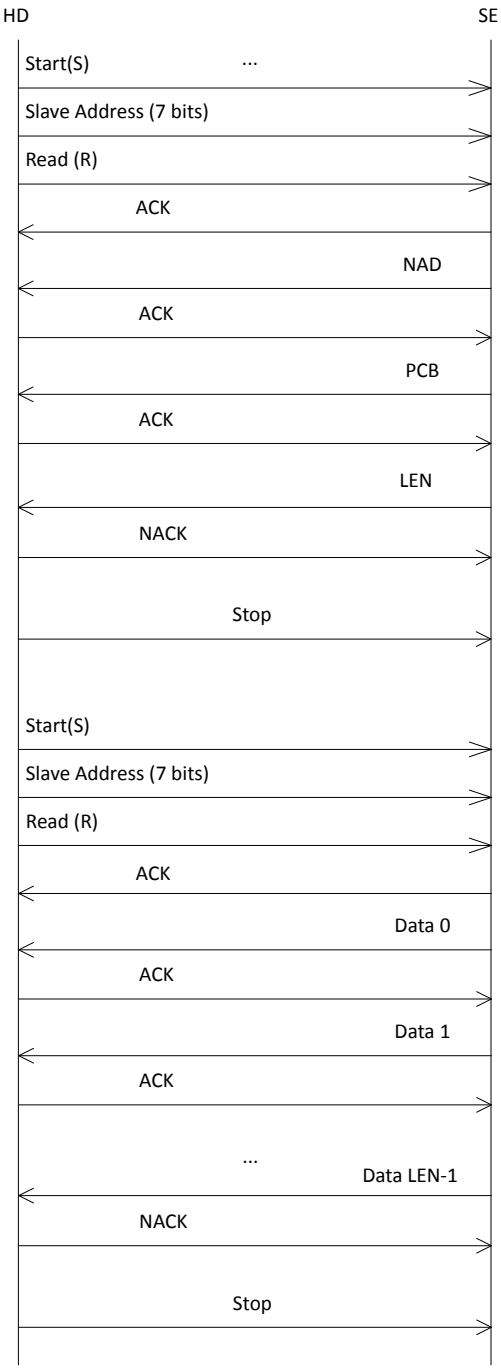

Figure 10. I²C multiple frames - SE to HD

Figure 11 shows the HD read sequence flow diagram.

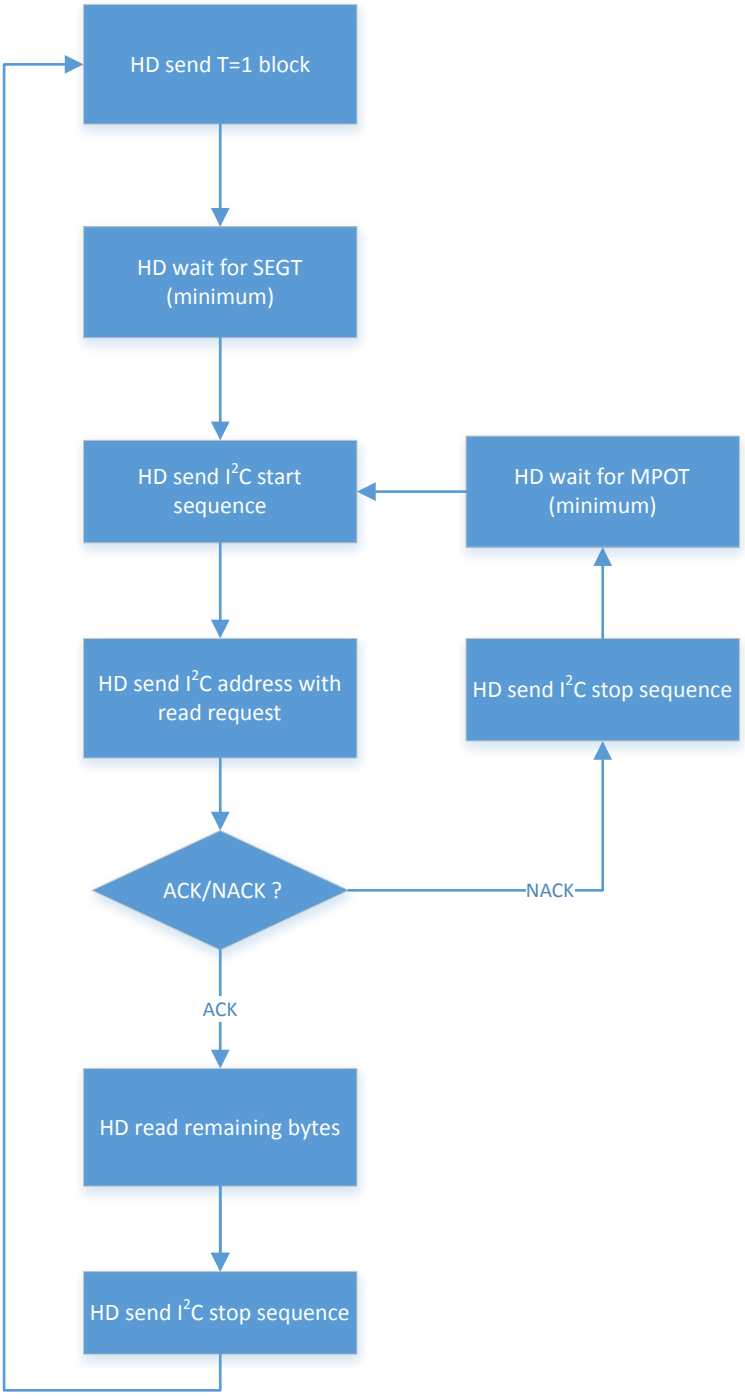

Figure 11. HD Read Sequence

3.1.1.4 SE I²C Default Values

SE shall use the following default values for the I²C parameters:

Table 14. I²C Default Values

Parameter	Value	Unit	Description
DSEGT	10	us	Default SEGT value
DMPOT	1	ms	Default MPOT value
DPWT	5	ms	Default Power-Wakeup Time value

4 Abbreviations and Notations

Table 15. Abbreviations

Abbreviation	Meaning
APDU	Application Protocol Data Unit
ATR	Answer to Reset
BWT	Block Waiting Time: maximum delay between the leading edge of the last character of the command block received by the SE and the leading edge of the first character of the next response block transmitted by the SE. It represents the maximum time the SE may take to send its response. It is used to detect cases where the SE does not respond or takes too long to respond. The SE shall send a WTX signal if it wishes more time to process a command and build the corresponding response.
IDLE byte	IDLE byte has a value of 0xFF. It indicates SE is idle and does not have any more bytes to send.
CRC	Cyclic Redundancy Code
DAD	Destination Node Address
HD	Hosting Device (master of a I^2C communication)
KhZ	1000 Hertz
I-Block	Information Block
IFS	Maximum Information Field Size
IFSC	Maximum information field size of SE
IFSD	Maximum information field size of Hosting Device
INF	Information Field
LEN	LENgth byte(s)
NAD	Node Address Byte
MPOT	Minimum Polling Time
POT	Polling Time: time interval between two polling requests made by the HD. This time interval shall be chosen by the HD based on the performances of the SE. The chosen value shall not be lower than the Minimum Polling Time (MPOT) communicated by the SE in the ATR.
MSB	Most Significant Bit
PCB	Protocol Byte
DPWT	Default Power Wake-Up Time: Time HD shall wait after power on before it starts to communicate with the SE.
R-Block	Receive Ready Block
SAD	Source Node Address
S-Block	Supervisory Block
SCL	Serial Clock Line
SDA	Serial Data Line
SE	Secure Element
SEGT	Secure Element Guard Time. Waiting time required by the SE between two I^2C accesses.

Table 15. Abbreviations...*continued*

Abbreviation	Meaning
WUT	Time taken by the SE to leave Power-Saving Mode and get ready to receive data.

5 References

[1] **ISO/IEC 7816-3:2006** Identification cards – Integrated circuit cards – Part 3: Cards with contacts – Electrical interface and transmission protocols

6 Legal information

6.1 Definitions

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