Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course
Integrated Systems Architecture

Master degree in Electrical Engineering

Group: 26

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Contents

CHAPTER 1

Lab 1: design and implementation of a digital filter

1.1 Reference model development

According to the formulas given to us to calculate the specifications of the filter, we know that

- **Even** group number $\Rightarrow p = 1 \Rightarrow$ **FIR** filter
- $x = 8$ (*Pourreza*) $\Rightarrow N = 2^p \cdot (x \mod 2) + 6 \cdot p = 8$
- $y = 7$ (*Ferrero*) $\Rightarrow n_b = y \mod 7) + 8 = 8$

1.1.1 Matlab model

According to the previous calculation, we are tasked with creating a 8-bit structured FIR filter with an architecture of order 8th. The specified cut-off frequency is 2 kHz. The filter is constructed using Matlab, and the frequency response of the filter is shown in Figure 1.1.

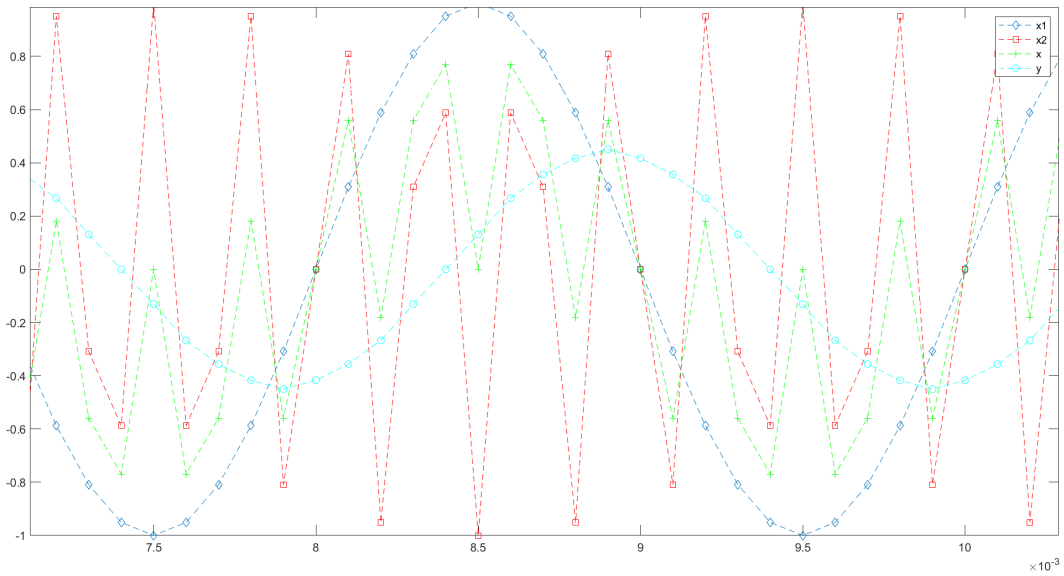


Figure 1.1: The image show the input wave (x1,x2) and the combined form (x) with frequency of 500 Hz and 3.5 kHz and the output from the filter (y)

The coefficients of the filter have one bit for the integer part and $n_b - 1 = 7$ bits for the fractional part. They correspond to the integer values shown in Table 1.1.

Table 1.1: Filter's coefficients

Coefficients	float value	integer value
b_0	0	0
b_1	0.0234	3
b_2	0.1094	14
b_3	0.2188	28
b_4	0.2656	34
b_5	0.2188	28
b_6	0.1094	14
b_7	0.0234	3
b_8	0	0

1.1.2 C model and THD

The number of bits after each multiplication is 14 and the THD is -39.58 dB.

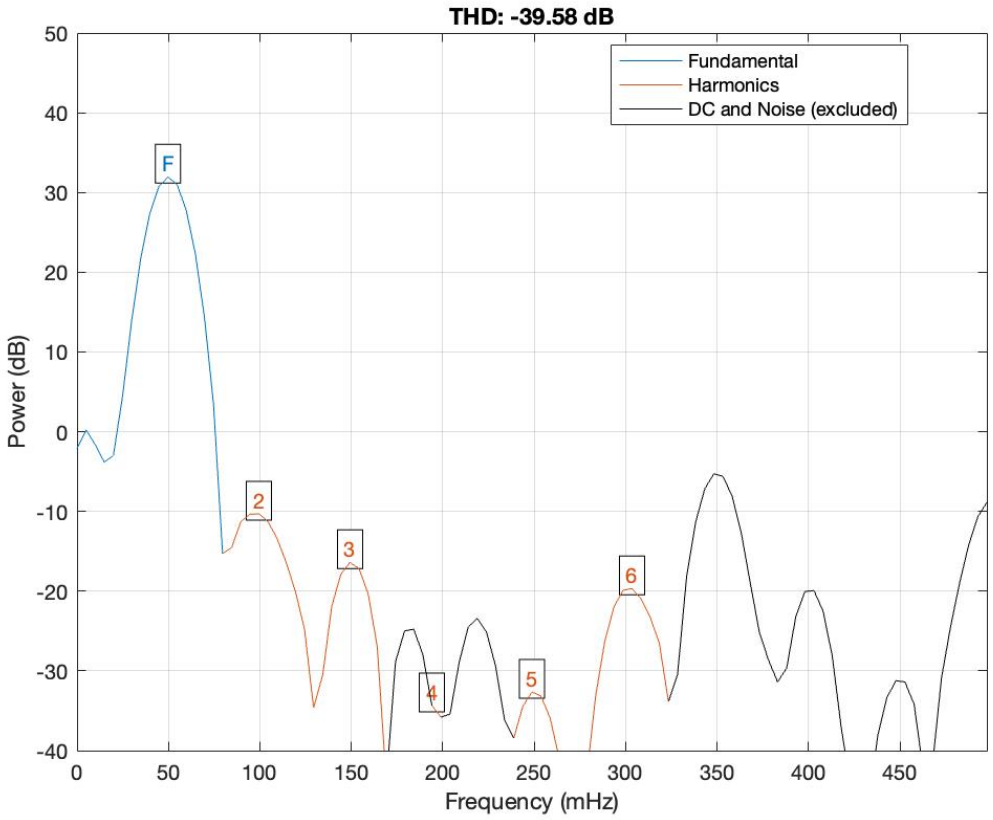


Figure 1.2: Total harmonic distortion of the filter from Matlab

1.1.3 Explanations, comparisons and comments

As it can be observed, the coefficients obtained as the result of the matlab and c simulations are very similar. The Matlab results are a little wider than C results but they have the same behaviour, as shown in the figure 1.3 below:

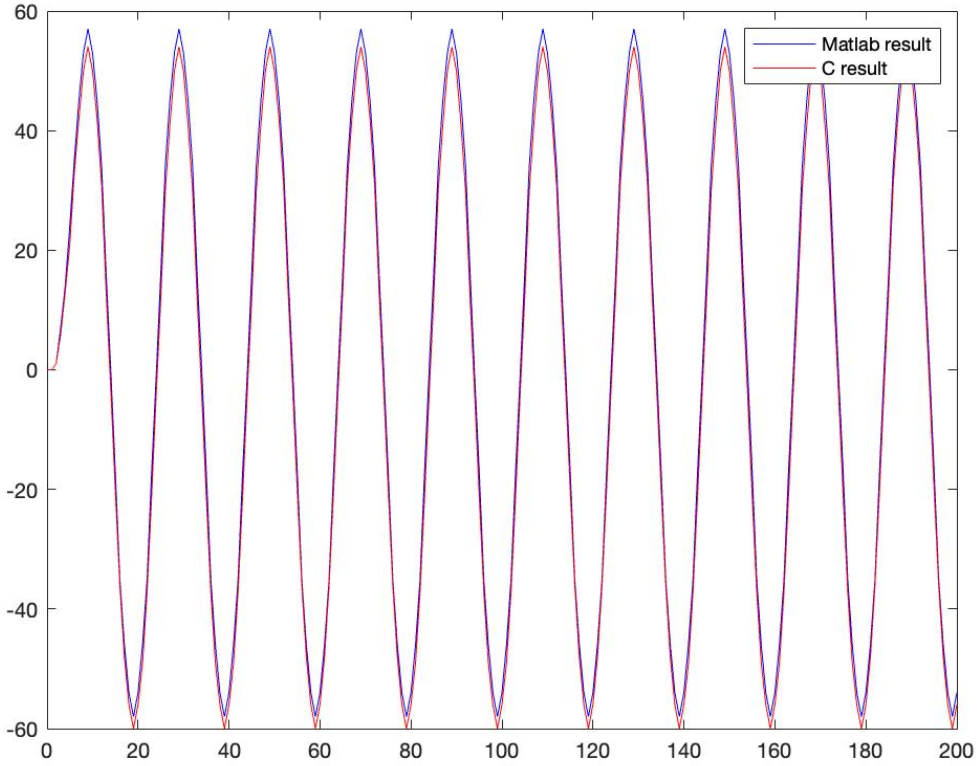


Figure 1.3: The image show the results obtained from Matlab, in blue, and from C code, in red.

1.2 VLSI implementation

1.2.1 Architecture

The architecture of the filter is shown in Figure 1.4

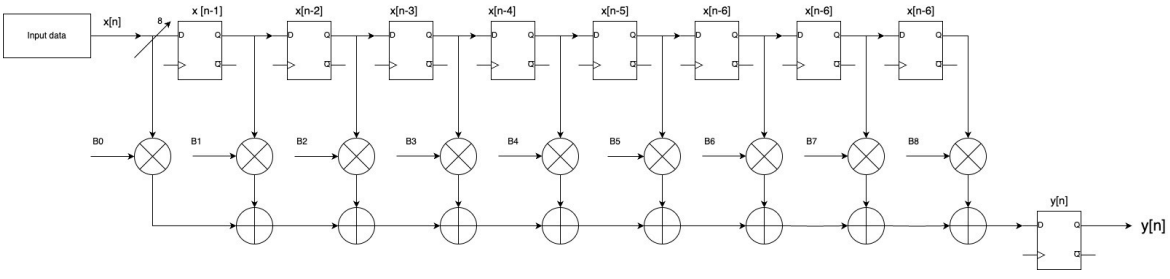


Figure 1.4: Architecture of FIR filter

To create the architecture we wrote the following VHDL code:

Listing 1.1: VHDL code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity myfir is
port
(
  DIN    : in   signed(7 downto 0);
  DOUT   : out    signed(7 downto 0);
  B0     : in   signed(7 downto 0);
  B1     : in   signed(7 downto 0);
  B2     : in   signed(7 downto 0);
  B3     : in   signed(7 downto 0);
  B4     : in   signed(7 downto 0);
  B5     : in   signed(7 downto 0);
  B6     : in   signed(7 downto 0);
  B7     : in   signed(7 downto 0);
  B8     : in   signed(7 downto 0);
  VIN    : in   std_logic;
  VOUT   : out    std_logic;
  RST_n    : in   std_logic;
  CLK    : in   std_logic
);
end myfir;

architecture behavior of myfir is

  signal DIN_in : signed(7 downto 0);
  signal x1,x2,x3,x4,x5,x6,x7,x8 : signed(7 downto 0);
  signal m0,m1,m2,m3,m4,m5,m6,m7,m8 : signed(15 downto 0);
  signal n0,n1,n2,n3,n4,n5,n6,n7     : signed(7 downto 0);

  begin

  m0 <= DIN_in * B0;
  m1 <= x1   * B1;
  m2 <= x2   * B2;
  m3 <= x3   * B3;
  m4 <= x4   * B4;
  m5 <= x5   * B5;
  m6 <= x6   * B6;
  m7 <= x7   * B7;
  m8 <= x8   * B8;

  n0 <= m0(14 downto 7)+  m1(14 downto 7);
  n1 <= n0        +  m2(14 downto 7);
  n2 <= n1        +  m3(14 downto 7);
  n3 <= n2        +  m4(14 downto 7);
  n4 <= n3        +  m5(14 downto 7);
  n5 <= n4        +  m6(14 downto 7);
  n6 <= n5        +  m7(14 downto 7);
  n7 <= n6        +  m8(14 downto 7);

  shift_register : process (CLK,DIN)
  begin

    if CLK'event and CLK = '1' then
```

```
      if VIN = '1' then
        DIN_in <= DIN;
        x8 <= x7;
        x7 <= x6;
        x6 <= x5;
        x5 <= x4;
        x4 <= x3;
        x3 <= x2;
        x2 <= x1;
        x1 <= DIN;
        DOUT <= n7;
        VOUT <= '1';
      else
        VOUT <= '0';
      end if;

      if RST_n = '0' then

        DIN_in <=   to_signed(0 ,8);
        x8 <=     to_signed(0 ,8);
        x7 <=     to_signed(0 ,8);
        x6 <=     to_signed(0 ,8);
        x5 <=     to_signed(0 ,8);
        x4 <=     to_signed(0 ,8);
        x3 <=     to_signed(0 ,8);
        x2 <=     to_signed(0 ,8);
        x1 <=     to_signed(0 ,8);
        DOUT <=   to_signed(0 ,8);
        VOUT <= '0';

      end if;

    end if;

  end process shift_register;



end behavior;
```

Simulation

To process all the samples the simulation lasts 1030 ns. A snapshot from 0 ns to 82 ns is shown in Figure 1.5 to highlight the behaviour of the filter when VIN moves from 0 to 1 and viceversa.

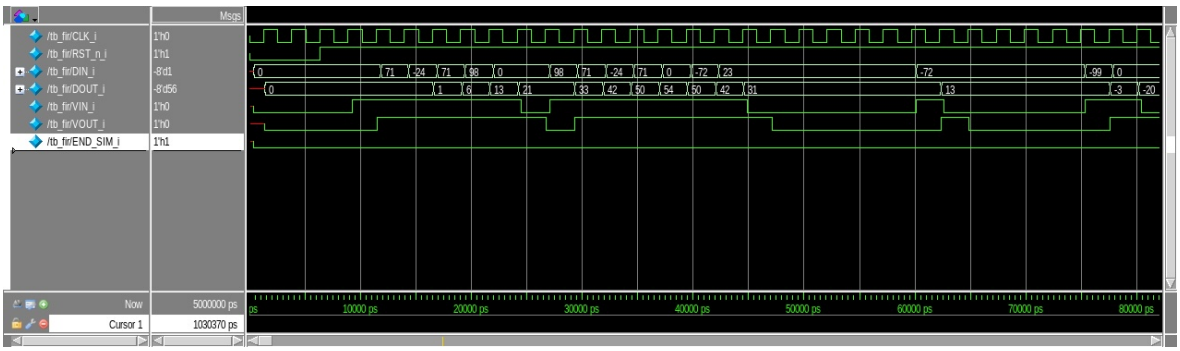


Figure 1.5: Simulation of the FIR filter when VIN moves from 0 to 1 and viceversa

As we can see from the table 1.2 result for both C program and VHDL are the same and it means VHDL work correctly.

C	VHDL
0	0
0	0
1	1
6	6
13	13
21	21
33	33
42	42
50	50
54	54
...	...
-49	-49
-56	-56
-60	-60
-56	-56
-49	-49
-37	-37
-21	-21
-4	-4
12	12
30	30
41	41
...	...
50	50
42	42
31	31
13	13
-3	-3
-20	-20
-36	-36
-48	-48
-56	-56
-60	-60
-56	-56

Table 1.2: Basic filter and C result

1.2.2 Logic synthesis

Reports showing slack met and power consumption are shown below. Results of the synthesis are shown in Table 1.3.

Table 1.3: This table describe the behaviour of the system: A is the area, P is the power consumption and T is the simulation time.

f_M = 393.7 MHz	A = 2961.6 nm^2	P = 1836 μW	T = 1030 ns
$f_M/2$ = 196.8 MHz	A = 2922.2 nm^2	P = 917 μW	T = 2060 ns

Table 1.4: This table describe the system at which we have applied clock gating: A is the area, P is the power consumption and T is the simulation time.

f_M = 393.7 MHz	A = 3025.5 nm^2	P = 1949 μW	T = 973.6 ns
$f_M/2$ = 196.8 MHz	A = 2842.7 nm^2	P = 886 μW	T = 1946.8 ns

1.2.3 Place and route

Snapshots showing no timing violation (timeDesign Summary table for both setup and hold modes) and power consumption are shown in Figures 1.6, 1.7 and 1.8.

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  2.662  |  2.928  |   N/A   |  2.662  |
|           TNS (ns):|  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |   N/A   |    0    |
|          All Paths:|   91    |   64    |   N/A   |   91    |
+--------------------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 59.761%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

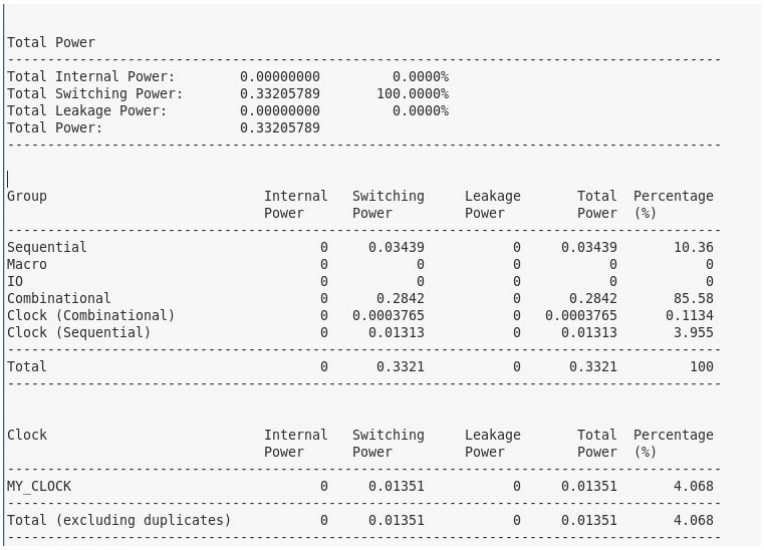
Figure 1.6: Setup Time

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg |reg2cgate| default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  0.097  |  0.097  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |   N/A   |    0    |
|          All Paths:|   64    |   64    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+

Density: 59.761%
       (100.000% with Fillers)
------------------------------------------------------------
```

Figure 1.7: Hold Time



```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.00000000         0.0000%
Total Switching Power:       0.33205789       100.0000%
Total Leakage Power:         0.00000000         0.0000%
Total Power:                 0.33205789
-----------------------------------------------------------------------------------------

Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                             0     0.03439           0     0.03439       10.36
Macro                                  0           0           0           0           0
IO                                     0           0           0           0           0
Combinational                          0      0.2842           0      0.2842       85.58
Clock (Combinational)                  0   0.0003765           0   0.0003765      0.1134
Clock (Sequential)                     0     0.01313           0     0.01313       3.955
-----------------------------------------------------------------------------------------
Total                                  0      0.3321           0      0.3321         100
-----------------------------------------------------------------------------------------


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
MY_CLOCK                               0     0.01351           0     0.01351       4.068
-----------------------------------------------------------------------------------------
Total (excluding duplicates)           0     0.01351           0     0.01351       4.068
-----------------------------------------------------------------------------------------
```

Figure 1.8: Power

Results of the place and route are shown in Table 1.5.

Table 1.5: Caption for my table: A is the area, P is the power consumption and T is the simulation time.

$$f_M/2 = 196.8 \text{ MHz} \;\Big|\; \text{A} = 2835.3\ nm^2 \;\Big|\; \text{P} = 332.1\ \mu W \;\Big|\; \text{T} = 1946.8 \text{ ns}$$

1.2.4 Explanations, comparisons and comments

As it can be observed from the table 1.4 and the table 1.5 the values are quite similar but we have a reduction in power by doing the place and route and also the area reduces slightly.

1.3 Advanced architecture development

By incorporating both pipelining and unfolding techniques into the filter design, we successfully obtained the following formulas, figure 1.9 and figure 1.10:

$$\begin{aligned}
y[3k] &= b0 \cdot x[3k] + b1 \cdot x[3k-1] + b2 \cdot x[3k-2] + b3 \cdot x[3k-3] + b4 \cdot x[3k-4] + b5 \cdot x[3k-5] + b6 \cdot x[3k-6] + b7 \cdot x[3k-7] + b8 \cdot x[3k-8] \\
y[3k+1] &= b0 \cdot x[3k+1] + b1 \cdot x[3k] + b2 \cdot x[3k-1] + b3 \cdot x[3k-2] + b4 \cdot x[3k-3] + b5 \cdot x[3k-4] + b6 \cdot x[3k-5] + b7 \cdot x[3k-6] + b8 \cdot x[3k-7] \\
y[3k+2] &= b0 \cdot x[3k+2] + b1 \cdot x[3k+1] + b2 \cdot x[3k] + b3 \cdot x[3k-1] + b4 \cdot x[3k-2] + b5 \cdot x[3k-3] + b6 \cdot x[3k-4] + b7 \cdot x[3k-5] + b8 \cdot x[3k-6]
\end{aligned}$$

Figure 1.9: Unfolding formula

$$\begin{aligned}
y[3k] &= b0 \cdot x[3k-3] + b1 \cdot x[3k-4] + b2 \cdot x[3k-5] + b3 \cdot x[3k-6] + b4 \cdot x[3k-7] + b5 \cdot x[3k-8] + b6 \cdot x[3k-9] + b7 \cdot x[3k-10] + b8 \cdot x[3k-11] \\
y[3k+1] &= b0 \cdot x[3k-2] + b1 \cdot x[3k-3] + b2 \cdot x[3k-4] + b3 \cdot x[3k-5] + b4 \cdot x[3k-6] + b5 \cdot x[3k-7] + b6 \cdot x[3k-8] + b7 \cdot x[3k-9] + b8 \cdot x[3k-10] \\
y[3k+2] &= b0 \cdot x[3k-1] + b1 \cdot x[3k-2] + b2 \cdot x[3k-3] + b3 \cdot x[3k-4] + b4 \cdot x[3k-5] + b5 \cdot x[3k-6] + b6 \cdot x[3k-7] + b7 \cdot x[3k-8] + b8 \cdot x[3k-9]
\end{aligned}$$

Figure 1.10: Pipeline formula

The architecture of the designed advance filter can be seen in 1.11:

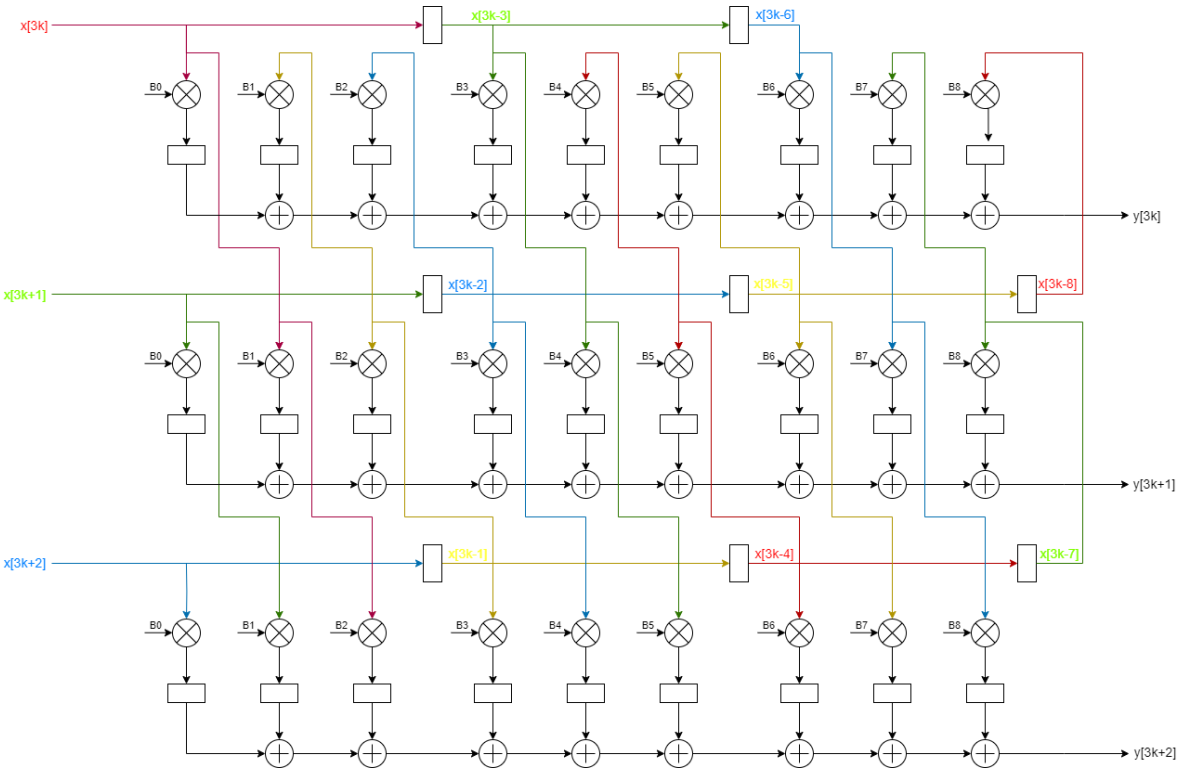


Figure 1.11: Architecture of the advanced FIR filter

By clock period of 100 ns it takes 13250 ns to process all samples. A snapshot from simulation of the advance FIR filter shows the behaviour of the filter. This snapshot is shown in 1.12.

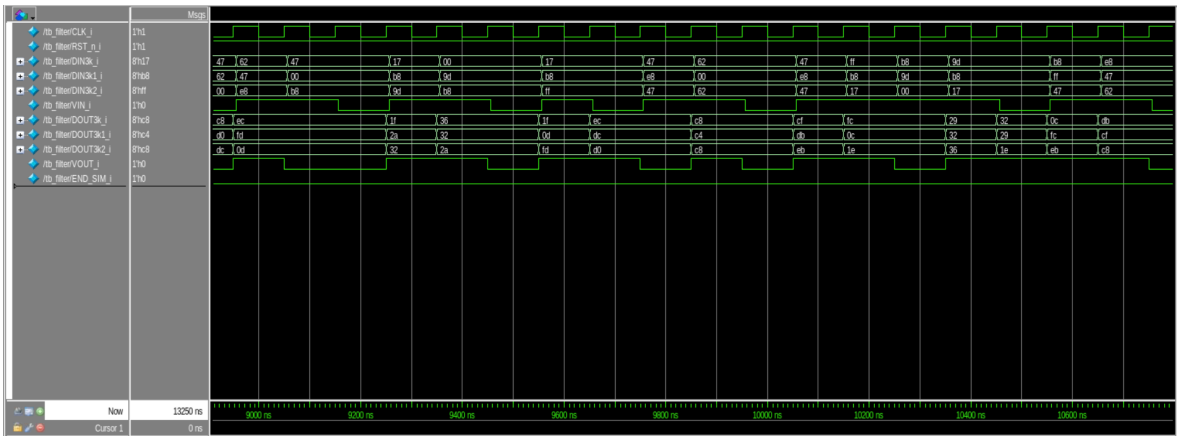


Figure 1.12: Advance architecure simulation

C	VHDL
0	0
0	0
1	1
6	6
13	13
21	21
33	33
42	42
50	50
54	54
...	...
-49	-49
-56	-56
-60	-60
-56	-56
-49	-49
-37	-37
-21	-21
-4	-4
12	12
30	30
41	41
...	...
50	50
42	42
31	31
13	13
-3	-3
-20	-20
-36	-36
-48	-48
-56	-56
-60	-60
-56	-56

Table 1.6: Advance filter and C result

As we can see from table 1.6 the result of the C program and the advance FIR filter report equal results and this means that our filter is working properly.

1.3.1 Logic synthesis

By running the synthesizer and gradually extending the clock period from zero, the slack reaches zero at 1.40 ns, resulting in a maximum frequency of 714.29 MHz. Figures 1.13, 1.14 and 1.15 illustrate slack met, area, and power consumption.

```
clock MY_CLOCK (rise edge)                                  1.40       1.40
clock network delay (ideal)                                 0.00       1.40
clock uncertainty                                          -0.07       1.33
Mul_result_3K_0_b_reg[6][6]/CK (DFF_X1)                     0.00       1.33 r
library setup time                                         -0.04       1.29
data required time                                                     1.29
--------------------------------------------------------------------------------
data required time                                                     1.29
data arrival time                                                     -1.29
--------------------------------------------------------------------------------
slack (MET)                                                            0.00
```

Figure 1.13: Summary of Timing Report utilizing the Maximum Frequency achievable

```
Number of ports:                         1612
Number of nets:                          8783
Number of cells:                         6837
Number of combinational cells:           6431
Number of sequential cells:               331
Number of macros/black boxes:               0
Number of buf/inv:                       1182
Number of references:                      66

Combinational area:               8950.634020
Buf/Inv area:                      684.418002
Noncombinational area:            1496.781946
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 10447.415966
```

Figure 1.14: Summary of Area Report utilizing the Maximum Frequency achievable

```
Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   1.2057 mW   (56%)
  Net Switching Power  = 961.7158 uW   (44%)
                         ---------
Total Dynamic Power    =   2.1675 mW  (100%)

Cell Leakage Power     = 234.3583 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         334.5500          46.0288          2.6053e+04           406.6318  (  16.93%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational    871.1861         915.6873          2.0831e+05          1.9952e+03  (  83.07%)
--------------------------------------------------------------------------------------------------
Total          1.2057e+03 uW      961.7161 uW      2.3436e+05 nW      2.4018e+03 uW
```

Figure 1.15: Summary of Power Report utilizing the Maximum Frequency achievable

1.3.2 Place and route

As we can see from figure 1.17 and figure 1.16 the timeDesign summary both for hold and setup modes show no timing violation. The power consumption is also shown in figure 1.18.

```
------------------------------------------------------------
      timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.142  |  0.258  |  0.142  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   356   |   330   |   354   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  | Nr nets(terms)   |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 58.150%
      (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

Figure 1.16: timeDesign summary table for setup

```
------------------------------------------------------------
     timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.112  |  0.112  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   330   |   330   |    0    |
+--------------------+---------+---------+---------+

Density: 58.150%
     (100.000% with Fillers)
------------------------------------------------------------
```

Figure 1.17: timeDesign summary table for hold

```
Total Power
----------------------------------------------------------------------------------------------
Total Internal Power:        1.18451853        51.8351%
Total Switching Power:       0.87516671        38.2977%
Total Leakage Power:         0.22548207         9.8672%
Total Power:                 2.28516730
----------------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
----------------------------------------------------------------------------------------------
Sequential                       0.4484     0.06107     0.02605      0.5355       23.43
Macro                                 0           0           0           0           0
IO                                    0           0           0           0           0
Combinational                    0.7279      0.7312      0.1993       1.658       72.57
Clock (Combinational)          0.008214     0.08293   0.0001529     0.09129       3.995
Clock (Sequential)                    0           0           0           0           0
----------------------------------------------------------------------------------------------
Total                            1.185      0.8752      0.2255       2.285         100
----------------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
----------------------------------------------------------------------------------------------
VDD                       1.1      1.185      0.8752      0.2255       2.285         100


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
----------------------------------------------------------------------------------------------
MY_CLOCK                       0.008214     0.08293   0.0001529     0.09129       3.995
----------------------------------------------------------------------------------------------
Total (excluding duplicates)   0.008214     0.08293   0.0001529     0.09129       3.995
----------------------------------------------------------------------------------------------
```

Figure 1.18: Summary of Power Report after place and route

1.3.3 Explanations, comparisons and comments

From what we can see from the figure 1.13 and consequentially the maximum frequency achievable by the new parallelized and pipelined circuit. The new achieved speed is thanks to the new design that as expected also increases the power required to operate as we can see in figure 1.15. Another penalizing factor is the increase in area due to the additional gates used, because of this the new design comes up to be more than 3.5 times larger than the original design as we can see in figure 1.14. After we processes the code inside Innovus we got very similar results to the previous simulations. As we can see in figure 1.18 the power consumption decreases from 2.4 μW to 2.28 μW due to the improved accurateness of Innovus.