OPL1000

ULTRA-LOW POWER 2.4GHZ WI-FI + BLUETOOTH SMART SOC

Data Sheet

Non-NDA Version

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REVISION HISTORY

Date	Version	Contents Updated
05/17/2018	0.1	• Initial Release
06/30/2018	0.2	• Updated General Description, Features, Block Diagram, Functional Descriptions, Pin Description, Security features, Package Information and Ordering Guide
10/12/2018	0.3	• Updated for accuracy
04/04/2018	0.4	• Added AUXADC chapter
06/30/2018	0.5	• Updated Pin Layout and Pin Description
10/12/2018	0.6	• Updated Features and Pin Description
01/18/2019	0.7	• Update current value

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1. GENERAL DESCRIPTION

The OPL1000 SoC features a fully integrated 2.4GHz radio transceiver and baseband processor for Wi-Fi 802.11b and Bluetooth® Smart applications. The SoC can be used as a standalone application-specific communication processor or as a wireless data link in hosted MCU systems where ultra-low power is critical. The OPL1000 supports flexible memory architecture for storing profiles, stacks and custom application codes, and can be updated using Over-The-Air (OTA) technology. Qualified Bluetooth Smart protocol stack and Wi-Fi TCP/IP stack are stored in a dedicated ROM. The OPL1000 is equipped with dual processors, ARM® Cortex®-M0 and M3, for handling different processes. All software runs on the ARM® Cortex®-M0 processor while more intensive application-specific activities run on the ARM® Cortex®-M3 processor. The OPL1000 can be connected to any external MCU through SPI, I2C or UART interfaces and sensors or other devices through GPIOs. The transceiver interfaces directly to the antenna and is fully compliant with the Wi-Fi 802.11b and Bluetooth 5.0 BLE standards. With integrated antenna switch, RF balun, power amplifier (PA) and low noise amplifier (LNA), the OPL1000 allows both Wi-Fi and Bluetooth Smart to minimize PCB design area and external component requirement.

2. FEATURES

The OPL1000 complies with ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

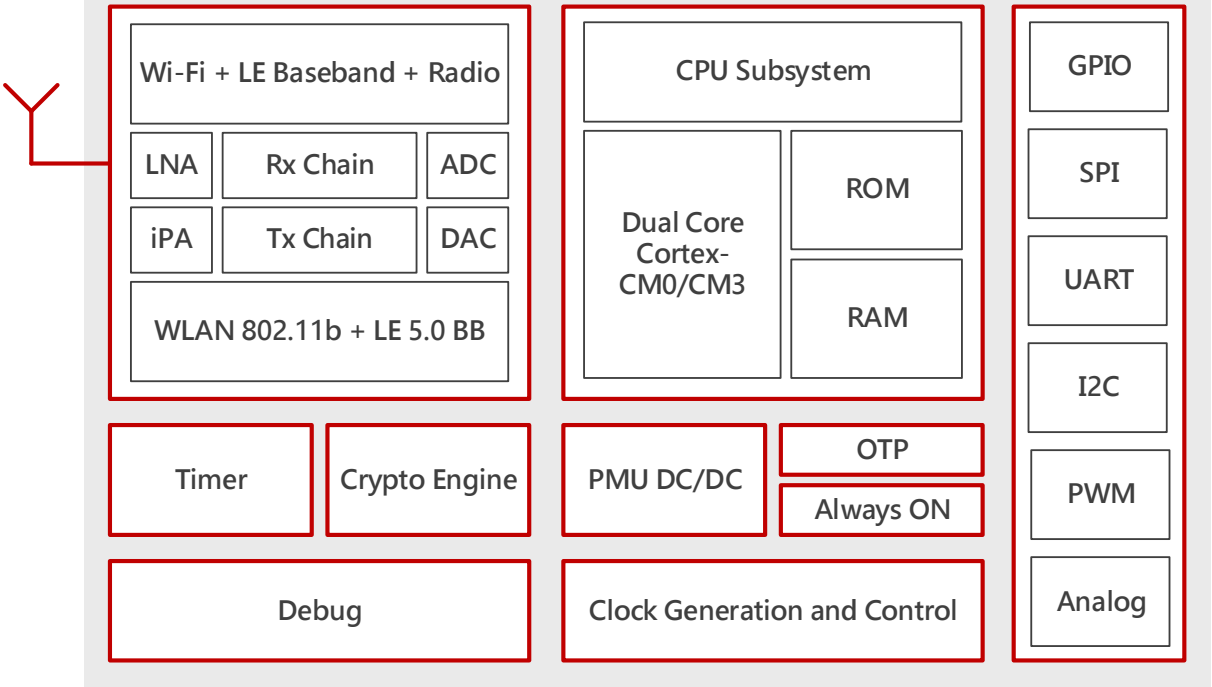
- Processors
  - ARM® Cortex®-M3 Application Processor
  - ARM® Cortex®-M0 Link Controller
- Wi-Fi
  - 802.11b up to 11Mbps
  - Supports STA mode
  - WPA/WPA2 security supported
  - Automatic beacon scanning and discovery
  - Built-in TCP/IP stack
  - Integrated dual power amplifiers: low (-2 dBm), high (+10 dBm) †

    † Optional internal T/R switch by-pass mode available to increase to +12dBm
- Bluetooth Smart
  - Compliant with Bluetooth 5.0 BLE specifications with 2Mbps rate capability
  - Slave mode support
  - All GATT-based profiles supported
  - Built-in BLE stack
  - 0 to 10 dBm transmit output power
  - -93 dBm receive sensitivity
- HW Crypto Engine
  - AES-128/256 bits Encryption
  - P-192/256 ECDH (Elliptic Curve Diffie-Hellman) Key Generation
  - SHA2
  - TRNG
- Power Management
  - Integrated Buck DC-DC converter
- General purpose, capture and sleep timers
- FW OTA (Over-The-Air) update support

- Digital Interfaces
  - General purpose I/Os: 24
  - Two UARTs with hardware flow control up to 3Mbps
  - Three SPI+™ interfaces
  - One I2C bus at 100 kHz, 400 kHz
- Analog Interfaces
  - 10-bit Auxiliary ADC inputs up to 16 channels
  - Six GPIO pins with 16mA driving capability
  - Six PWMs
- Radio Transceiver
  - Fully integrated dual-mode 2.4 GHz CMOS transceiver
  - Single wire antenna: no external matching and no external T/R switch required
- Package
  - 48-pin QFN, 6 mm x 6 mm

3. BLOCK DIAGRAM

Figure 1: OPL1000 Block Diagram



4. PIN DEFINITIONS

4.1. Pin Layout

4.2. Pin Description

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU and Memory

5.2. Timer

5.3. Radio

5.4. Wi-Fi Baseband

5.5. Bluetooth Low Energy

5.6. Network Stack Support

6. INTERFACES

The OPL1000 provides various control interfaces for easy access to network stack from customer applications.

6.1. General Purpose Input/Output (GPIO)

6.2. Peripheral Transport Subsystem (PTS)

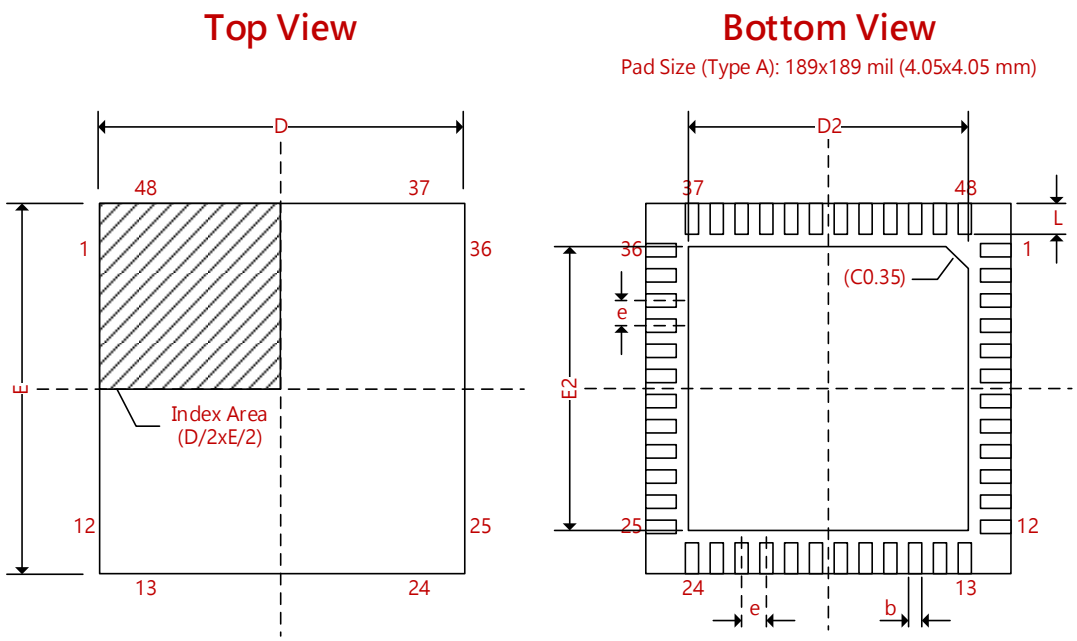
7. SECURITY

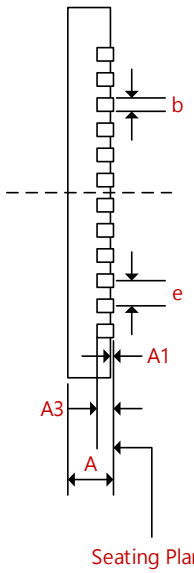
Industry leading hardware-based security accelerator is included in the OPL1000. The supported features include the following:

- Software API support:
  - AES Encryption/Decryption
  - AES-CMAC
  - AES CCM
  - TRNG
  - ECDH Key Pair Generation
  - DH Key
  - HMAC-SHA1
  - SHA2
- Wi-Fi security support:
  - 802.11i-2007
  - WPA-PSK (TKIP) / WPA2-PSK (AES) / Mix Mode
- LE security support:
  - Security manager
  - Improved privacy with low power consumption (LE Privacy 1.2 and Secure Connections)
  - P256 Key Pair (ECDH Key Pair)

8. PACKAGE INFORMATION

Figure 3: OPL1000 QFN48 Packaging Drawing





Symbol	Package Type		
	TQFN		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
L	0.30	0.40	0.50
e	0.40 BSC.		

		Exposed Pad Dimension		
Type A	Pad Size	D2/E2		
	189x189	Min	Nom	Max
	(4.05x4.05)	3.95	4.05	4.15

9. ORDERING INFORMATION

Part Number	Package	Description	Ambient Operating Temperature
OPL1000TKQGT†	6x6mm QFN	2.4GHz single band Wi-Fi 802.11b+LE 5.0	-30 to 70°C

† "T" for "Tape & Reel"

CONTACT

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