OPL1000

ULTRA-LOW POWER 2.4GHZ WI-FI + BLUETOOTH SMART SOC

Development Board HDK

OPULINKS

OPL1000-HDK-R06 | Version 0.6

REVISION HISTORY

Date	Version	Contents Updated
04/04/2018	0.1	• Initial Release
04/23/2018	0.2	• Updated Chapters “DC power outing and decoupling” and “ Getting started” for better understanding • Modified the following figures: RF oscillator design、RF external Flash and Mode_strap common PIN circuit、IoT motherboard reference design、IoT Module Board reference design • Added Chapter “ Development Setup”
06/30/2018	0.3	• Updated for new package
08/04/2018	0.4	• Updated schematic and layout file
09/30/2018	0.5	• Updated schematic and layout file
10/10/2018	0.6	• Updated schematic and layout file

TABLE OF CONTENTS

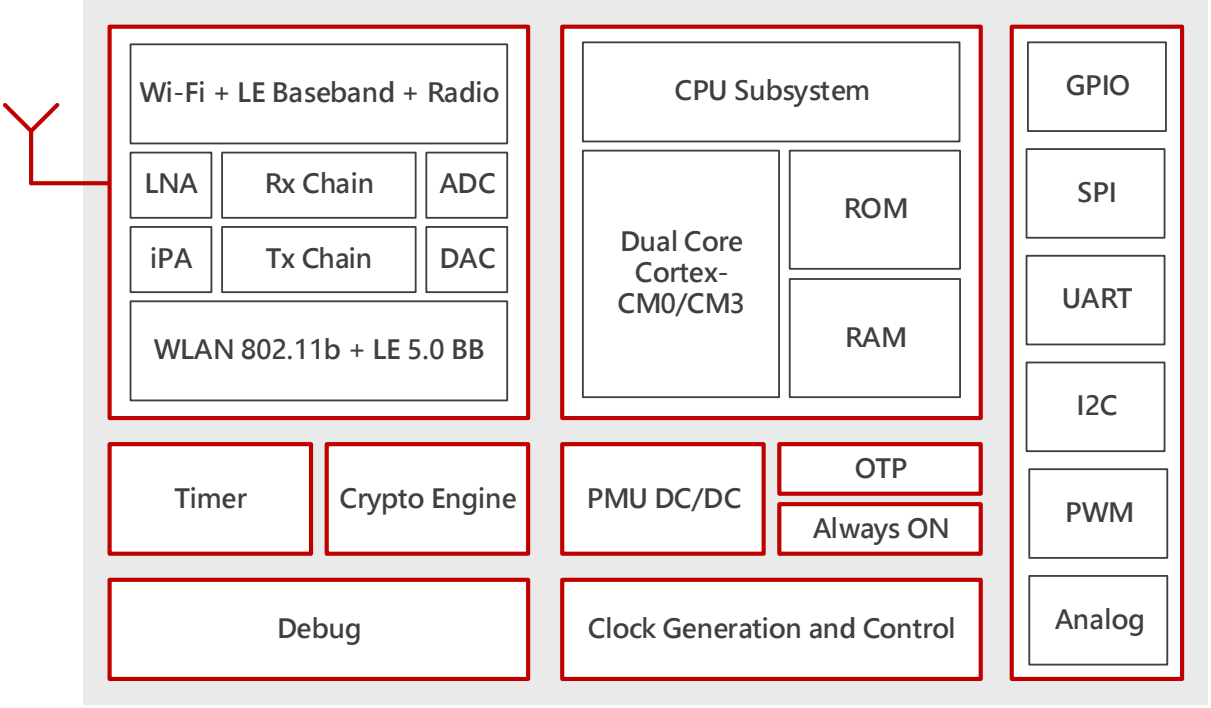
LIST OF FIGURES

1. ABSTRACT

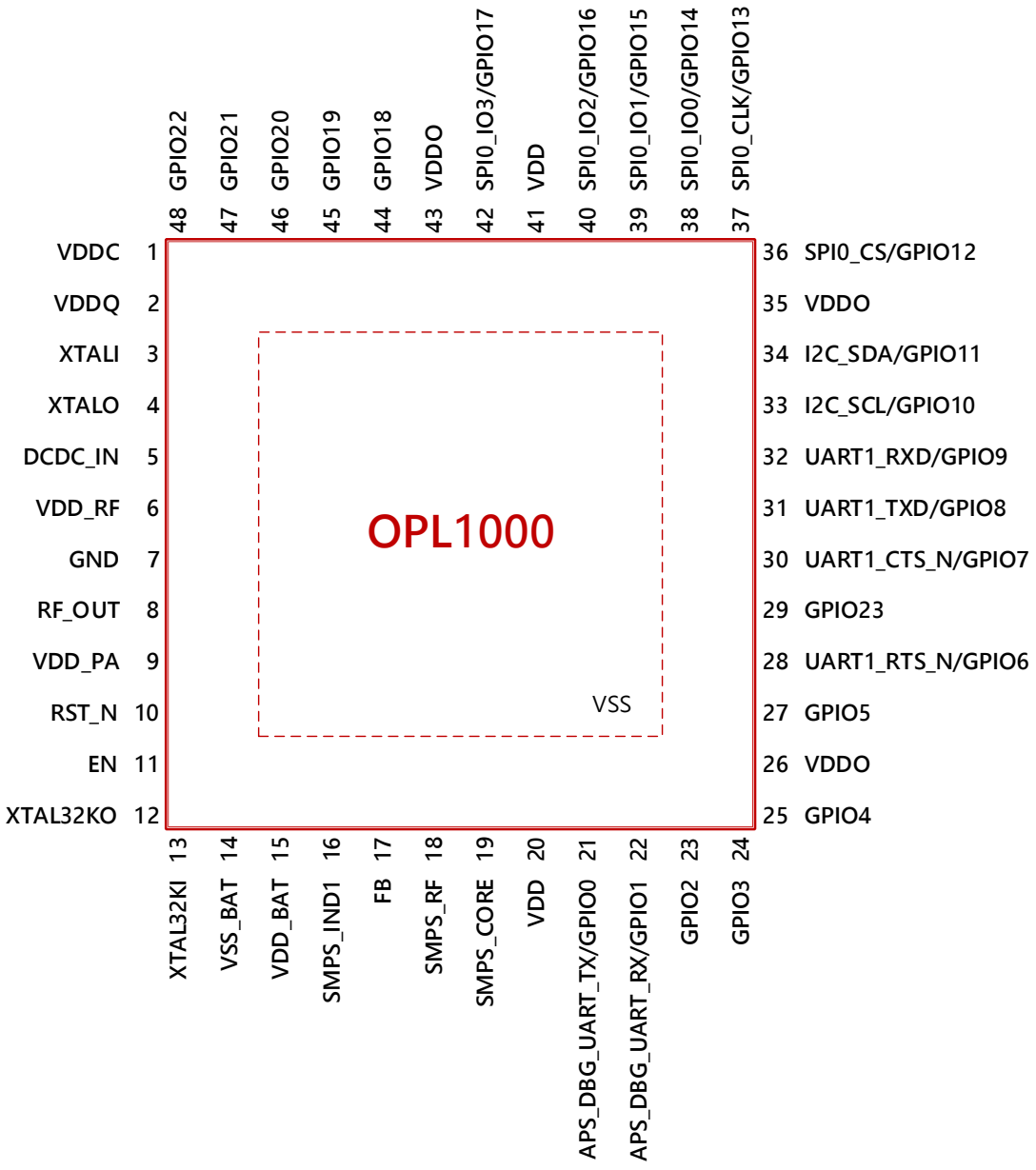
OPL1000 is a single-chip with Wi-Fi 802.11b & Bluetooth® functionality of highly integrated wireless connectivity in satisfying all requirements of Wi-Fi & Bluetooth connection, with latest technology in offering the lowest power consumption, smallest package while supporting the most interfaces, with ultra-low production cost, in pioneering the latest application domain as the chip every customer's development cannot do without.

2. INTRODUCT

OPL1000 is a highly integrated application processing chip (SoC) with high cost-performance ratio and ultra-low power consumption, as it offers a total solution for Wi-Fi 802.11b and Bluetooth® connectivity with dual-core ARM® 32-bit MCUs to meet the diverse needs of IoT universe, while the product also features ample peripheral interface supporting all kinds of texting transmission, effective collection and processing of distributed data for applications in cloud network systems, as well as provides real-time monitoring, along with functions such as messaging encryption, and compliance in transmission protocols for messaging authentication, etc. All efforts point to the ultimate goals of expedited realization in consumer electronic product development and mass production fulfillment, when applied in segments such as smart home appliances, industrial / factory automation, intelligent security alarm and fire-safety (connection network linkage) system, access and attendance control, smart power grid, environmental and ecological monitoring, and pollution prevention, etc.



3. CHIP PACKAGE AND COMMON GROUND



Pin Name	Type	Location	Function Description
VDDC	P	1	Digital core power output
VDDQ	P	2	OTP power supply for programming mode
XTALI	I	3	External crystal input pin
XTALO	O	4	External crystal output pin
DCDC_IN	P	5	Analog LDO supply input
VDD_RF	P	6	RF LDO output. Connects with external capacitor to ground.
GND	P	7	Ground
RF_OUT	IO	8	RF input/output with on-chip T/R switch
VDD_PA	P	9	PA power supply with external capacitor
RST_N	I	10	Reset input signal, Low active
EN	I	11	Enable input, pull high is necessary
XTAL32KO	O	12	External 32K crystal output pin
XTAL32KI	I	13	External 32K crystal input pin
VSS_BAT	G	14	Buck Ground
VDD_BAT	P	15	Power supply
SMPS_IND1	P	16	DC-DC power converter inductor pin
FB	I	17	Feedback pin
SMPS_RF	P	18	DC-DC converter output
SMPS_CORE	P	19	DC-DC converter output
VDD	P	20	Digital core power
APS_DBG_UART_TX / GPIO0[†]	IO	21	APS UART serial data transmit
APS_DBG_UART_RX / GPIO1[†]	IO	22	APS UART serial data receive
GPIO2[†]	IO	23	General Purpose Input/Output
GPIO3[†]	IO	24	General Purpose Input/Output
GPIO4[†]	IO	25	General Purpose Input/Output
VDDO	P	26	Power supply for IO pad

Pin Name	Type	Location	Function Description
GPIO5†	IO	27	General Purpose Input/Output
UART1_RTS_N / GPIO6†	IO	28	UART Request to Send (default) / General Purpose Input/Output
GPIO23†	IO	29	General Purpose Input/Output
UART1_CTS_N / GPIO7†	IO	30	UART Clear to Send (default) / General Purpose Input/Output
UART1_TXD / GPIO8†	IO	31	UART serial data transmit (default) / General Purpose Input/Output
UART1_RXD / GPIO9†	IO	32	UART serial data receive (default) / General Purpose Input/Output
I2C_SCL / GPIO10†	IO	33	I2C serial clock line (default) / General Purpose Input/Output
I2C_SDA / GPIO11†	IO	34	I2C serial data line (default) / General Purpose Input/Output
VDDO	P	35	Power supply for IO pad
SPI0_CS / GPIO12†	O	36	SPI Chip Select (default) / General Purpose Input/Output
SPI0_CLK / GPIO13†	O	37	SPI serial clock (default) / General Purpose Input/Output
SPI0_IO0 / GPIO14†	IO	38	SPI input/output (default) / General Purpose Input/Output
SPI0_IO1 / GPIO15†	IO	39	SPI input/output (default) / General Purpose Input/Output
SPI0_IO2 / GPIO16†	IO	40	SPI input/output (default) / General Purpose Input/Output
VDD	P	41	Digital core power
SPI0_IO3 / GPIO17†	IO	42	SPI input/output (default) / General Purpose Input/Output
VDDO	P	43	Power supply for IO pad
GPIO18†	IO	44	General Purpose Input/Output
GPIO19†	IO	45	General Purpose Input/Output

Pin Name	Type	Location	Function Description
GPIO20†	IO	46	General Purpose Input/Output
GPIO21†	IO	47	General Purpose Input/Output
GPIO22†	IO	48	General Purpose Input/Output
VSS	P	E-Pad	Common Ground

† Multi-function pins. Please refer to the Pin Multiplexing Table below for the multi-functions provided.

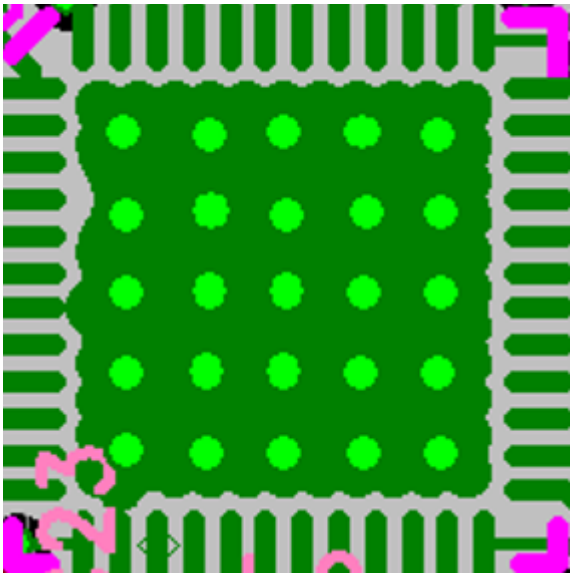
4. RF CIRCUIT

OPL1000 utilizes a minute number of components, facilitating connection from antenna to the RF_OUT (pin 8) on the IC, as the chip integrates an automatic Transmit/Receive two-way switch (T/R switch) in achieving a highly-simplified design to support various required applications, and for further information, please refer to the content of “CHIP PACKAGE AND COMMON GROUND".

5. GROUND PLANES

As VSS (e-Pad) integrated RF, baseband, grounding (GND), of Buck DC-DC converter, and that of external interface, complemented by the first layer exposed Cu soldering, in order to achieve the optimal grounding and cooling area, while large number of grounding via are installed in RF on PCB to prevent the amplification of parasitic effect caused by current circuit, as via is also instrumental in preventing cross-coupling between RF signal and other signals. Both circuits of power and Buck DC-DC converter must take into consideration of component circuit current, enlarged width and the shortest path.

Illustration 1: Via



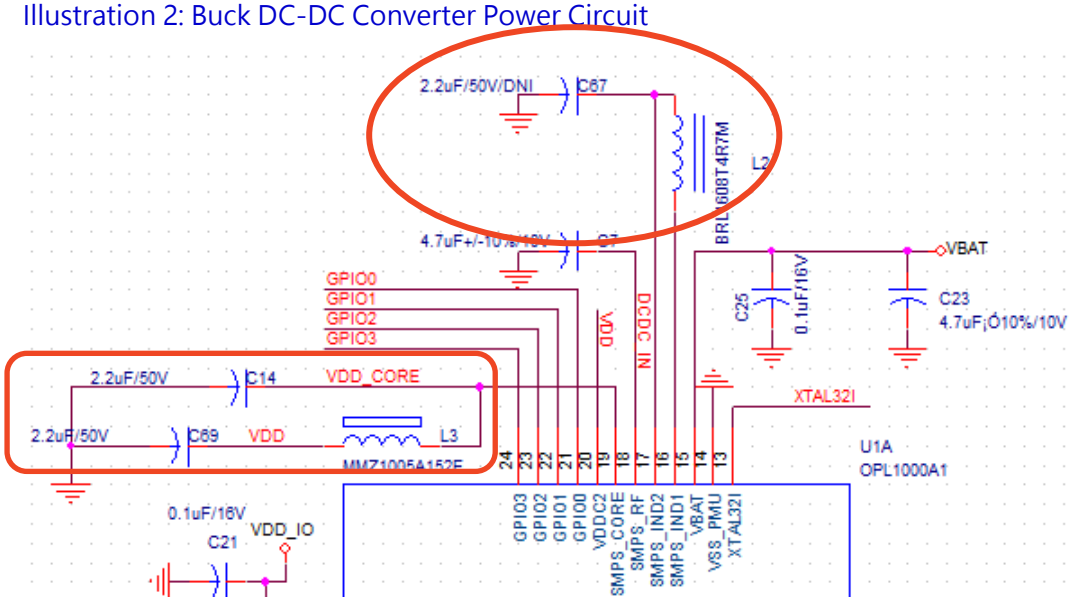
6. DC POWER OUTING AND DECOUPLING

In order to achieve minimal power consumption, users may, under all types of operational modes, control the power modules in the control chip in OPL1000 chip of internal high-performance Buck & LDO DC-Dc Converter. The system power, with input of decoupled capacitor from external battery power originated from VDD_BAT (pin 15), reduces noise with in-chip Buck DC-DC Converter, respectively in,

1. RF Power System: output of 1.3 VDC at SMPS_RF (pin 18), via decoupled capacitor, then input at DCDC_IN (pin 5), before generating 1.1V, via LDO, at VDD_RF (pin 6), with decoupled capacitor, in order to provide the power required by RF. Furthermore, VDD_PA (pin 9) is the main power supply of PA power amplifier, which is of the same voltage as VDD_BAT, and requires decoupling capacitor added.
2. Inner-Core System: PI circuits are added at SMPS_CORE (pin 19) and VDD (pin 20), and connected via decoupled capacitor VDD (pin 41), in order to lower noise. VDDC (pin 10 is required to be added with decoupling capacitor, in order to lower noise.
   VDDO (pin 26, pin 35, & pin 43) is the power for IO interface, of the same voltage as VDD_BAT.

Buck DC-DC converter, through SMPS_IND1 (pin 16), series with inductor L2 to FB (pin 17), as inductor should be located near chip with minimum area, while the locations of grounding of output capacitor and input capacitor should be close to each other (the nearer the better), with board diagram shown below.

Illustration 2: Buck DC-DC Converter Power Circuit



Inductor L2 wiring should be widened with its path most shortened

Larger decoupled capacitor is recommended to be used for power circuit, as it should be near the chip without elongated grounding circuit in layout so as to avoid parasitic inductance, and thereby leading to accidental circuit feedback. RF power circuit adopts smaller decoupled capacitor, and should be located near the chip, with the circuit below for reference.

Grounding Limitation of Capacitor C67

The reference ground plane of this capacitor is VSS_BAT, which, in layout, should be located near the ground plane of the decoupled capacitor of VBAT to form an independent circuit.

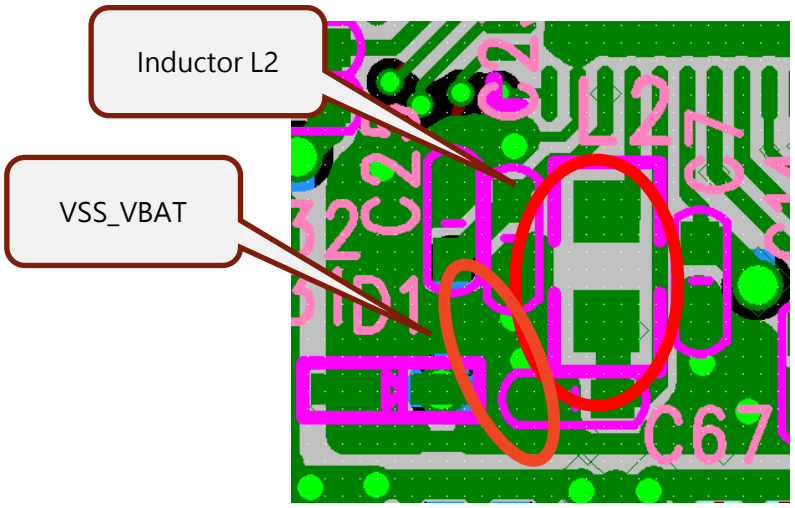
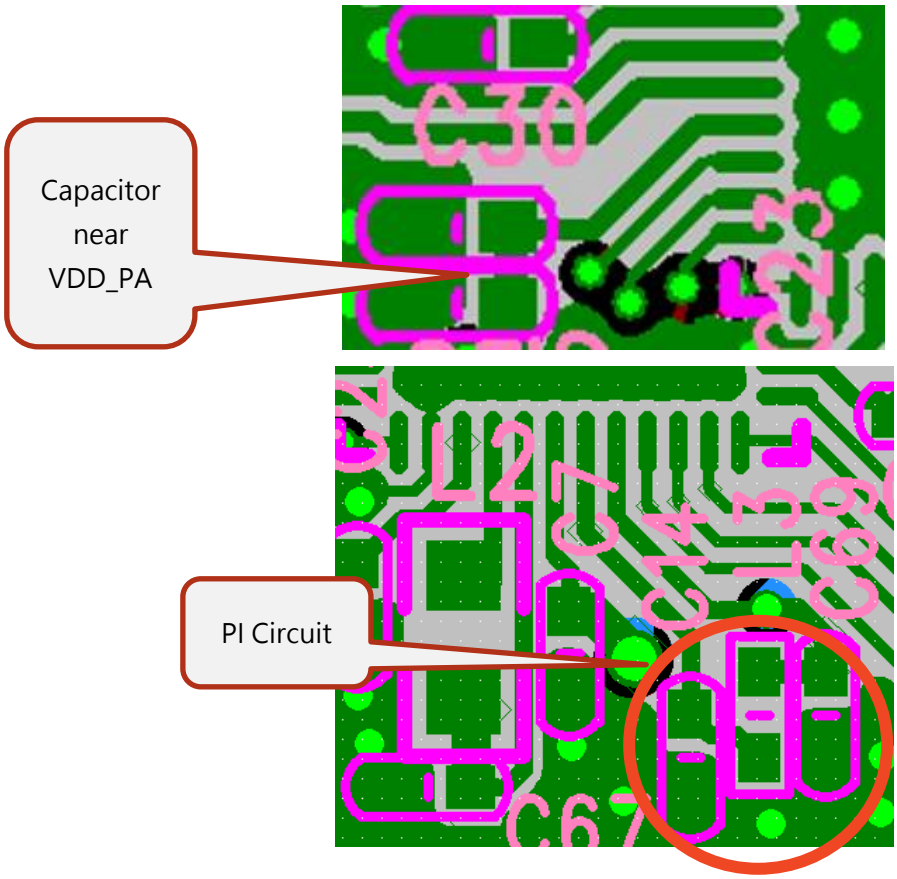


Illustration 3: RF Power Circuit



7. GETTING STARTED

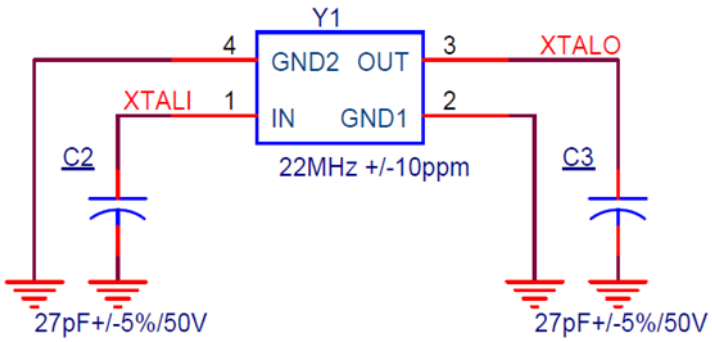
Users can product different layouts based on respective development or application purposes, with some modes are suitable/applicable for particular applications.

GPIO14	GPIO13	GPIO12	GPIO6	Strapping Mode
0	0	0	1	Digital debug mode
0	0	1	0	ICE mode
0	0	1	1	JTAG mode
0	1	0	0	DFT mode
0	1	0	1	OTP programming mode
0	1	1	0	MBIST mode
0	1	1	1	AUXADC debug mode
1	0	0	0	RF debug mode
1	0	0	1	Radio mode
1	0	1	0	Normal function mode

7.1. Oscillator

The chip includes Internal RC OSC、32.768 KHz crystal & 22 MHz crystal oscillator circuit, and please note that the selection of deviation value would directly affect system performance, as the capacitor wiring should be made as short as possible, and C2 & C3 can be optimized according to specifications of different manufacturers. (22 MHz crystal is made by Abracon with LLCpart-number of ABM：10W-22.0000MHZ-4-B1U-T3)(Used Abracon LLC part number ABM:10W-22.0000MHZ-4-B1U-T3 as 22MHz Crystal)

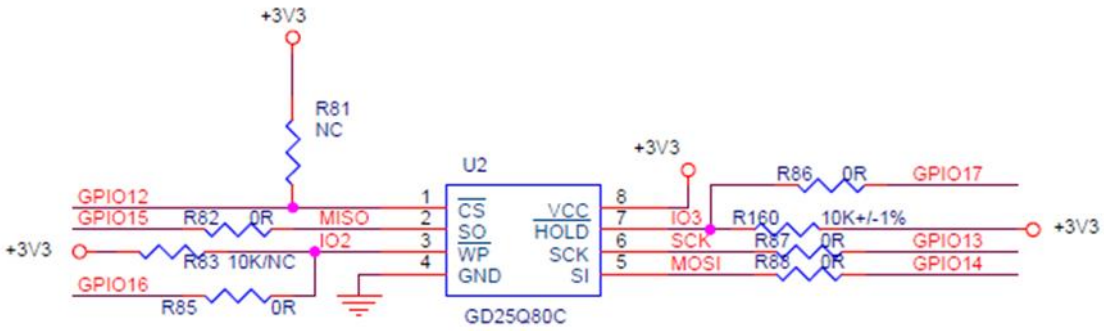
Illustration 4: Oscillator Circuit



7.2. External Flash

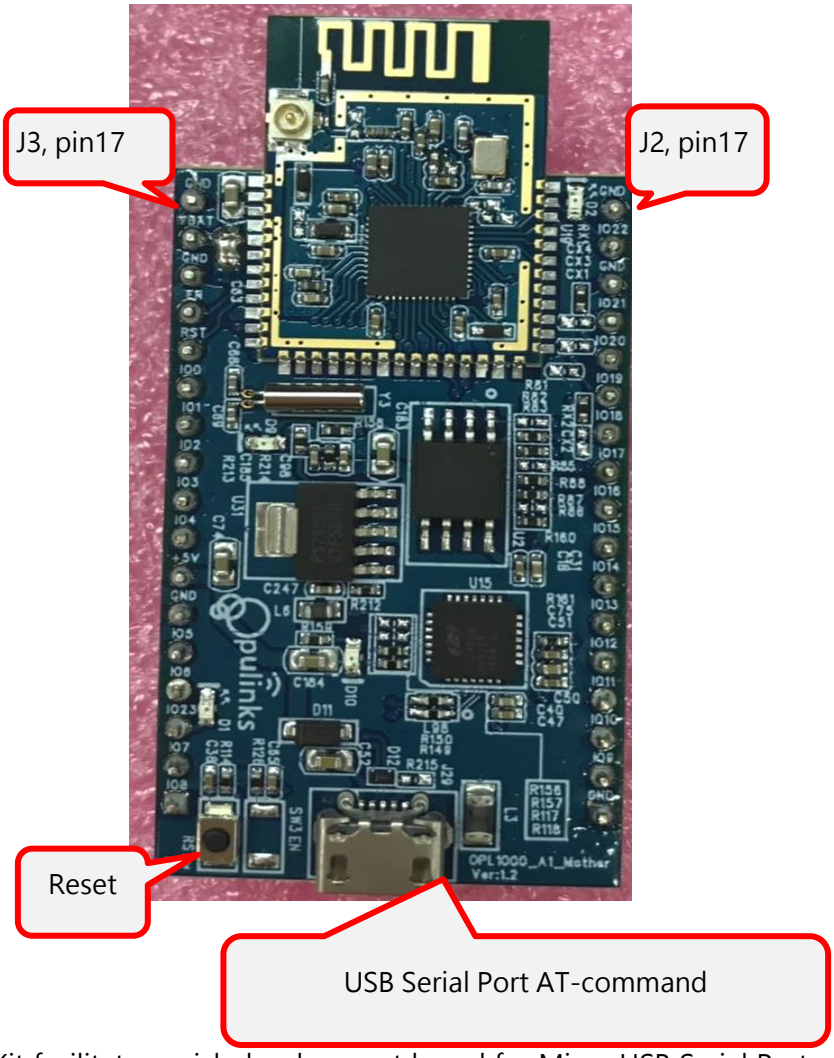
With 4-bit multiplexed I/O serial interface adopted, it is both adopted by GPIO12/13/14 and Mode_strap, and please pay attention to the usage layout for common PINs.

Illustration 5: Common PIN Circuit of External Flash of RF and Mode_strap



8. DEVELOPMENT SETUP

Illustration 6: Actual photo of IoT Motherboard and (module board)



OPL1000 IoT DevKit facilitates quick development board for Micro USB Serial Port, as customers can easily use USB to quickly evaluate and complete product development, while providing full-set development service which includes, useable GPIO PINs. Normal Function Mode, as default mode, can quickly switch to ICE mode, and in addition, functions such as flash software upgrade, GPIO, ADC, SPI and I2C, etc., are facilitated as (Bottom View) table shown below

J2						ANT		J3				
ICE Mode	PWM	I2C	ADC	Pin Name	Pin No		Pin No	Pin Name	ADC	SPI	UART	Flash Prg
				GND	pin 17		pin 17	GND				
	Yes			GPIO22	pin 16		pin 16	+3V				
				GND	pin 15		pin 15	GND				
M3_CLK				GPIO21	pin 14		pin 14	CHIP_EN				
M3_DAT				GPIO20	pin 13		pin 13	RST_N				
M0_DAT				GPIO19	pin 12		pin 12	GPIO0(REV)				UART_Prg_Tx
M0_CLK				GPIO18	pin 11	Bottom	pin 11	GPIO1(REV)				UART_Prg_Rx
		SDA	Yes	GPIO17	pin 10	View	pin 10	GPIO2	Yes	MOSI	TxD	
		SCLK	Yes	GPIO16	pin 9		pin 9	GPIO3	Yes	MISO	RxD	
				GPIO15	pin 8		pin 8	GPIO4	Yes	CLK		
				GPIO14	pin 7		pin 7	Ex_5V				
				GPIO13	pin 6		pin 6	GND				
	Yes			GPIO12	pin 5		pin 5	GPIO5	Yes	CS		
				GPIO11	pin 4		pin 4	GPIO6	Yes			
				GPIO10	pin 3		pin 3	GPIO23				
	Yes			GPIO9	pin 2		pin 2	GPIO7	Yes	CS		
				GND	pin 1	USB	pin 1	GPIO8	Yes			

Note 1: Flash burn UART_Prg Serial Port Baud rate: 115200 bps, n, 8,1

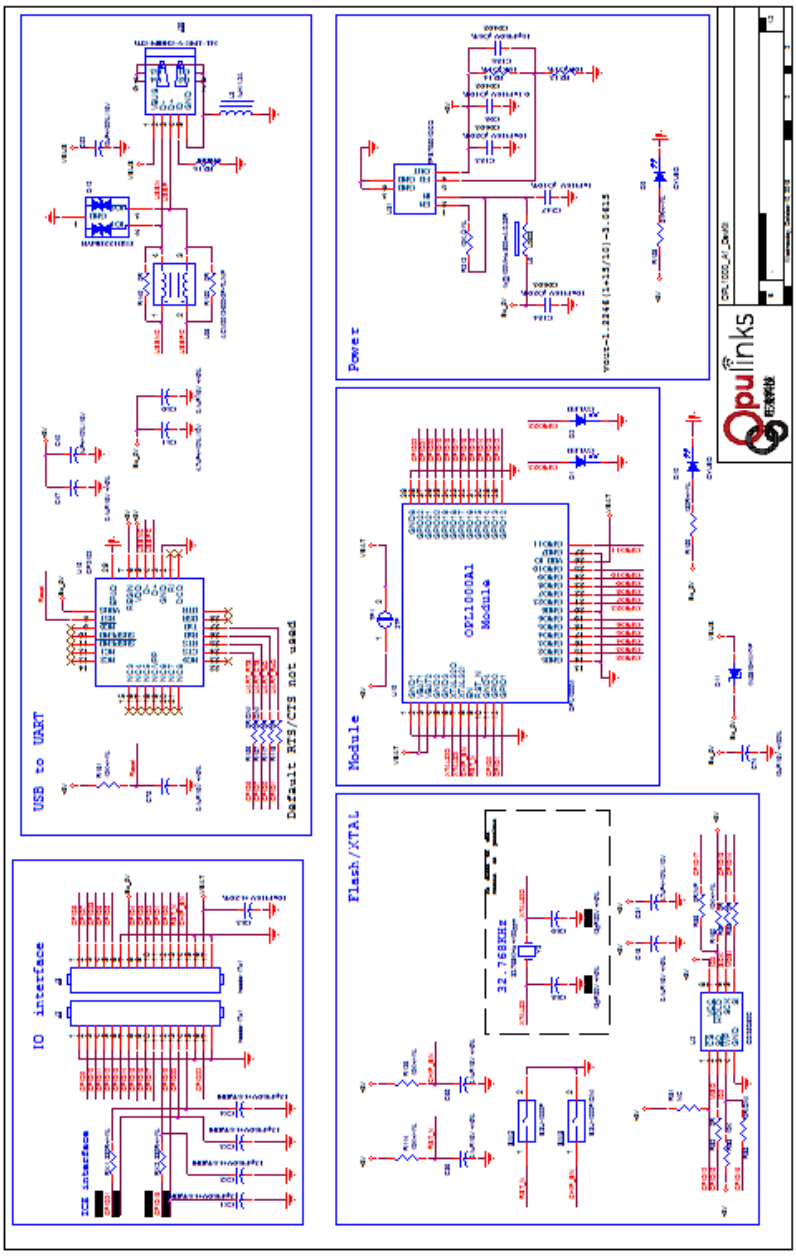
Note 2: Some PINs are multi-functional, e.g. GPIO2 can be set as general GPIO or ADC, SPI or UART

Note 3: GPIO18~23 can support high drive current 12mA/16mA.

Note 4: Chip Enable (CHIP_EN) and Reset (RST_N) can be regarded as “Reset” function.

9. ELECTRICAL SCHEMATICS AND PCB LAYOUT

Illustration 7: Reference Circuit of IoT Motherboard



The antenna of Module Board must be exposed on motherboard, in order to achieve optimal transmission range.

Illustration 8: IoT Motherboard Design Layout

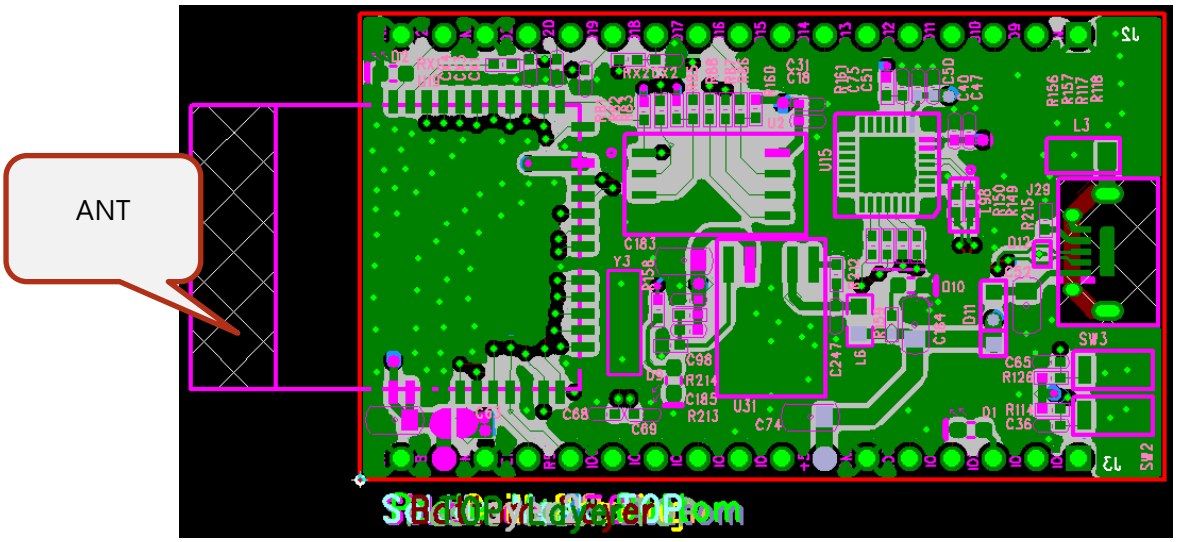


Illustration 9: Reference Circuit of Module Board

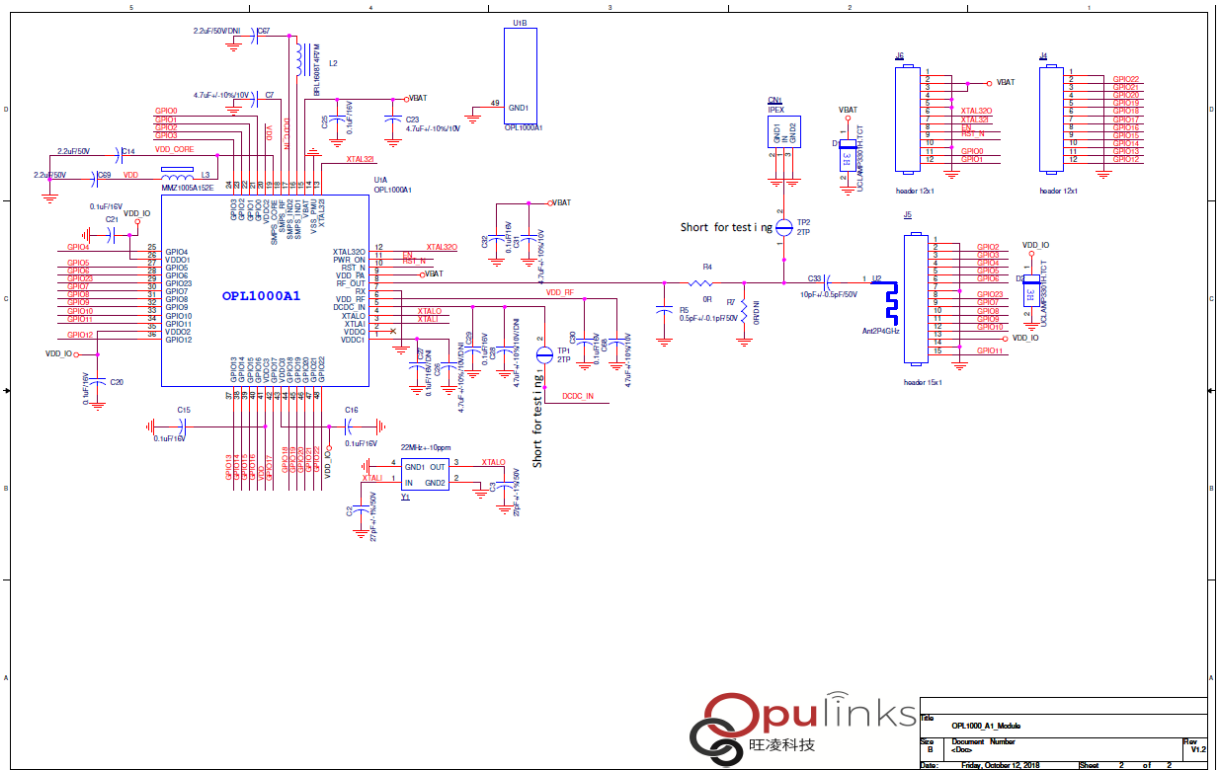
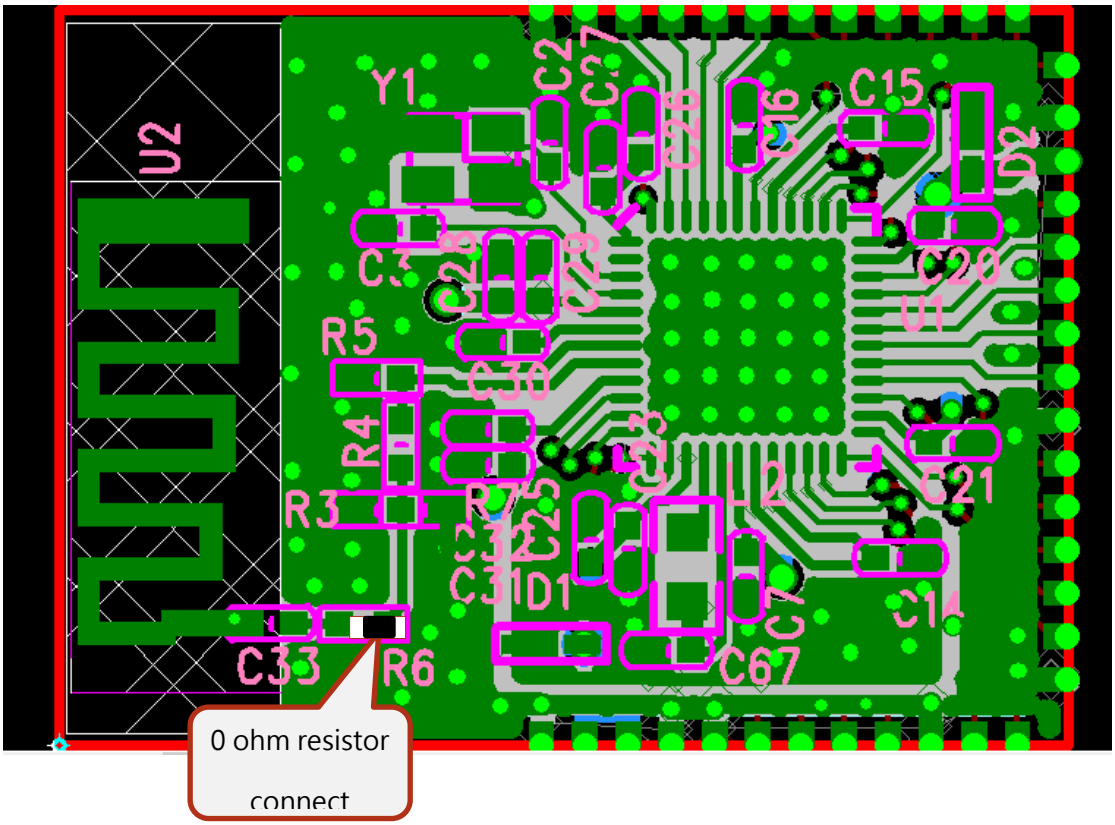


Illustration 10: IoT ModuleBoard Design Layout



Note: After the testing of IoT ModuleBoard is completed, low-cost PCB antenna can be used by zero-ohm resistor on TP1 , to transmit and receive over-the-air electromagnetic radiation.

10. PCB LAYER STACK-UP

For compliance to EMI Standard, and optimal system performance, 4-layer design is adopted, with stacking shown in the table below:

PCB Layer	Signal Type	Design Keys
Layer 1 (Top Layer)	Placed in components and RF signal wiring, as well as other signal wiring	• 50 (ohm) resistance need with the grounding of Layer 2 =>RF trace need 50 ohm impedence control reference to L2 • Large number of Ground Via are designated in RF area until Layer 4 • Large number of Via are designated in decoupled capacitor in power supply • The location of VSS (E-PAD) on chip should have exposed unpainted Cu, with large number of VIA to Layer 4.
Layer 2	Main grounding circuit does not go with other signal lines circuit	
Layer 3	Mainly of power supply that can go with other signal lines	
Layer 4 (Bottom layer)	Power supply and other signal lines	

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