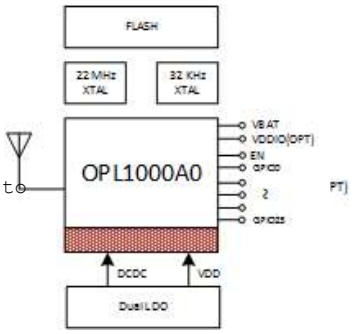
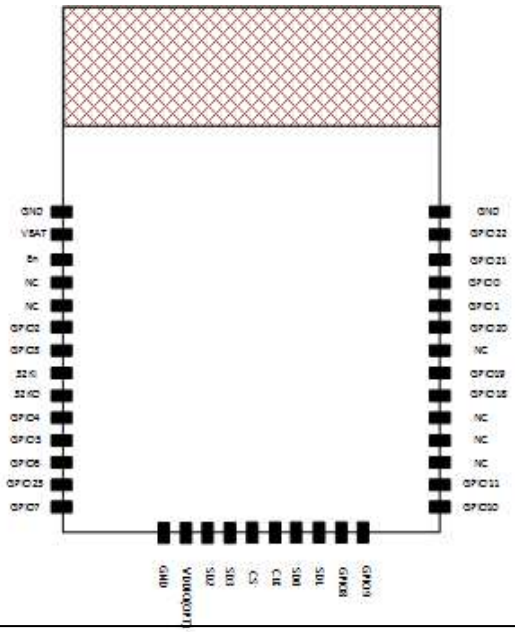
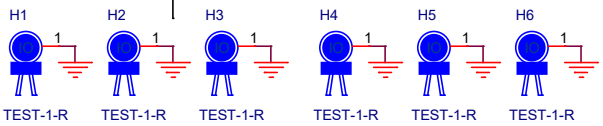
OPL1000 A1 Module

Date	Description
2018/01/23	Initial
2018/02/07	1. move out flash, 32K XTAL, C24
2018/06/15	1. Change to A1 version
2018/09/10	1. C26,C27 C28 DNI 2. Add C68, C69 L3 CN1 3. remove R3 R6 4. C14 change to 4.7uF 5. Add pi circuit on pin19,pin20
2018/10/29	1. Add Flash, 32K XTAL, RST, EN circuit
2018/11/08	1. remove C18,R82,R87,R88 (Flash part) 2. remove C20,C16, change C21 to 4,7uF 3. remove C18, change C72 to 10uF 4. remove D1,D2,C28,C26,C27 5. Change 32.768 XTAl 6. Change C70,C71 to 5.1pF
2018/12/03	1. remove C67 (Buck FB)
2018/12/22	1. Add U6/U7 LDO device 2. Remove TP2 and change TP3 circuit
2019/01/04	1. Reserve C82,C83
2019/02/14	1. R4 change to 1.2nH 2. R5 change to 1.2pF 3. L2,C14, C7 DNI
2019/03/07	1. Remove C78, R168, U7 2. R171 change to 6.2K 3. R167 change to 0 ohm
2019/03/21	1. Reserve L3 component
2019/03/22	1. Reserve L4 component for VDD connection with VDD_RF 2. Add R172 for SMFS_IND1 trace to connect with LDO enable pin 3. Remove C82, c83
2019/04/01	1. Remove L2, L3, C7, C14, C69
2019/05/16	1. C1,C65,R172 DNI 2. Change R126 51K ohm 3. R4 change 0 ohm
2019/05/22	1. Change C70,C71 to 9pf
2019/05/29	1. Change R114 to 44.2k ohm
2019/06/13	1. Midify A1 pin definition
2019/06/25	1. Point(TP4&TP5) is short

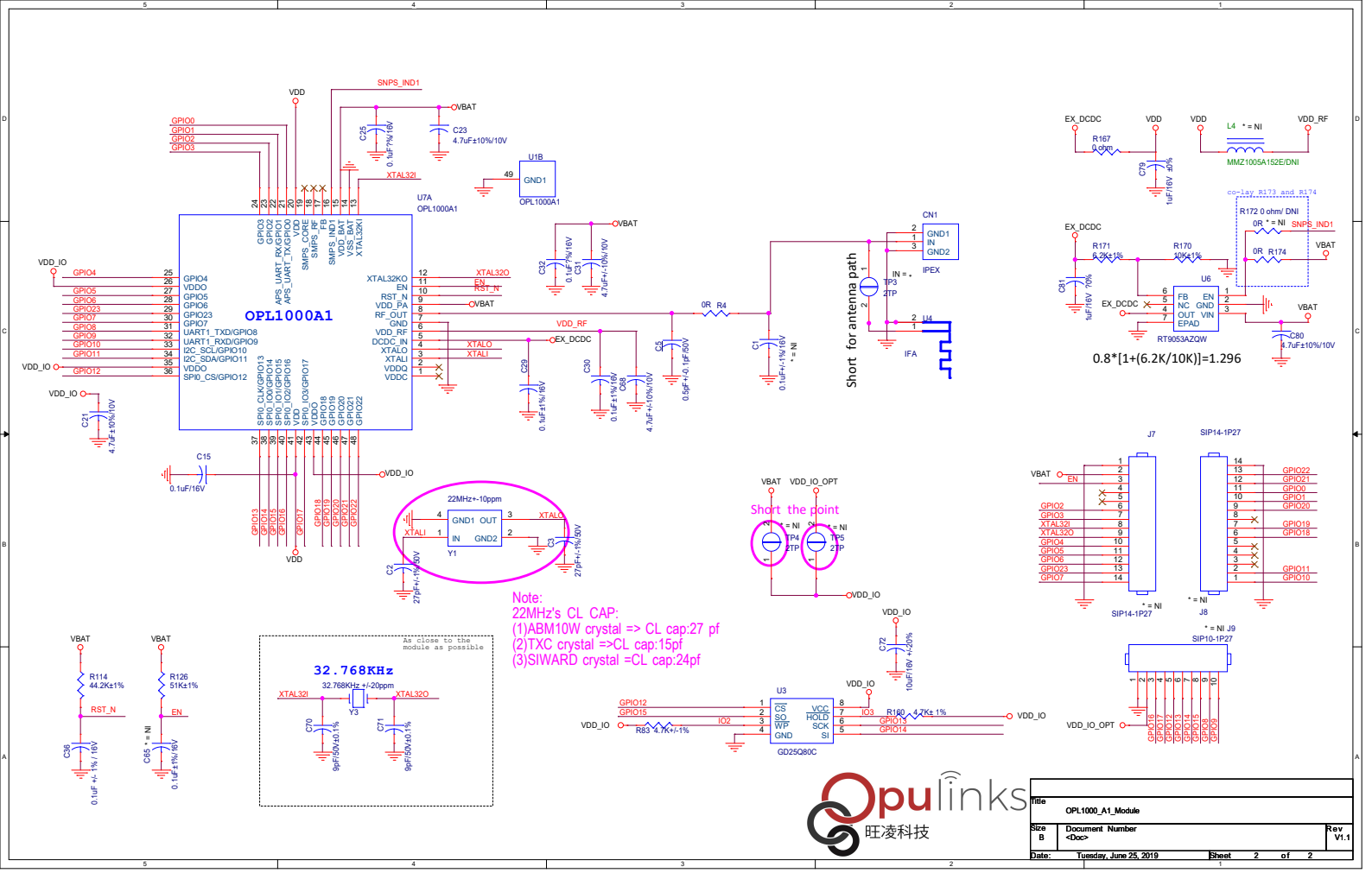






Opulinks 旺凌科技

Title	History		
Size A	Document Number <Doc>		Rev V1.1
Date: Tuesday, June 25, 2019		Sheet 1 of 2	


OPL1000A1
U7A
OPL1000A1
U1B
GND1
OPL1000A1
VDD
SNPS_IND1
VBAT
C25
0.1uF±1%/16V
C23
4.7uF±10%/10V
XTAL32I
GPIO0
GPIO1
GPIO2
GPIO3
VDD_IO
GPIO4
GPIO5
GPIO6
GPIO23
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
C21
4.7uF±10%/10V
C15
0.1uF/16V
XTAL32KO
EN
RST_N
VDD_PA
RF_OUT
GND
VDD_RF
DCDC_IN
XTALO
XTALI
VDDQ
VDDC
XTAL32O
VDD_RF
EX_DCDC
C32
0.1uF±1%/16V
C31
4.7uF+/-10%/10V
C29
0.1uF±1%/16V
C30
0.1uF±1%/16V
C68
4.7uF+/-10%/10V
C55
0.5pF+/-0.1pF/50V
0R R4
C1
0.1uF+/-1%/16V
* = NI
CN1
GND1
IN
GND2
IPEX
Short for antenna path
TP3
2TP
U4
IFA
22MHz+-10ppm
GND1 OUT
IN GND2
Y1
C2
27pF+/-1%/50V
C3
27pF+/-1%/50V
Note:
22MHz's CL CAP:
(1)ABM10W crystal => CL cap:27 pf
(2)TXC crystal =>CL cap:15pf
(3)SIWARD crystal =CL cap:24pf
VBAT
VDD_IO_OPT
Short the point
TP4
2TP
TP5
2TP
R114
44.2K±1%
RST_N
C36
0.1uF +/-1% / 16V
R126
51K±1%
EN
C65 * = NI
0.1uF±1%/16V
As close to the module as possible
32.768KHz
32.768KHz +/-20ppm
Y3
C70
9pF/50V±0.1%
C71
9pF/50V±0.1%
U3
GD25Q80C
CS
SO
WP
GND
VCC
HOLD
SCK
SI
GPIO12
GPIO15
IO2
IO3
R83 4.7K+/-1%
R160 4.7K± 1%
GPIO13
GPIO14
C72
10uF/16V +/-20%
EX_DCDC
R167
0 ohm
C79
1uF/16V ±5%
VDD
L4 * = NI
MMZ1005A152E/DNI
VDD_RF
co-lay R173 and R174
R172 0 ohm/ DNI
0R * = NI
SNPS_IND1
0R R174
VBAT
R171
8.2K±1%
R170
40K±1%
C31
1uF/16V /10%
U6
FB
NC
OUT
EPAD
EN
GND
VIN
RT9053AZQW
C80
4.7uF±10%/10V
0.8*[1+(6.2K/10K)]=1.296
J7
SIP14-1P27
J8
SIP14-1P27
GPIO22
GPIO21
GPIO0
GPIO1
GPIO20
GPIO19
GPIO18
GPIO11
GPIO10
* = NI J9
SIP10-1P27
GPIO16
GPIO17
GPIO12
GPIO13
GPIO14
GPIO15
GPIO28
GPIO29
Opulinks
旺凌科技
Title
OPL1000_A1_Module
Size B
Document Number
<Doc>
Rev V1.1
Date: Tuesday, June 25, 2019
Sheet 2 of 2