

Date	Description
2018/01/23	Initial
2018/02/07	1. move out flash, 32K XTAL, C24
2018/06/15	1. Change to A1 version
2018/09/10	1. C26,C27 C28 DNI 2. Add C68, C69 L3 CN1 3. remove R3 R6 4. C14 change to 4.7uF 5. Add pi circuit on pin19,pin20
2018/10/29	1. Add Flash, 32K XTAL, RST, EN circuit
2018/11/08	1. remove C18,R82,R87,R88 (Flash part) 2. remove C20,C16, change C21 to 4,7uF 3. remove C18, change C72 to 10uF 4. remove D1,D2,C28,C26,C27 5. Change 32.768 XTAL 6. Change C70,C71 to 5.1pF
2018/12/03	1. remove C67 (Buck FB)
2018/12/22	1. remove TP2 and change TP3 circuit
2019/05/16	1. C65 DNI 2. Change R126 51K ohm
2019/05/22	1. Change C70,C71 to 9pf
2019/05/29	1. Change R114 to 44.2K ohm
2019/06/13	1. Midify A1 pin definition
2019/06/25	1. Point(TP1&TP4&TP5) is short

OPL1000 A1 Module

The block diagram shows the OPL1000A0 module with its internal components and external connections. It includes a FLASH memory, two crystal oscillators (32 MHz XTAL and 32 KHz XTAL), and a variety of pins for power, control, and data transfer.

H1
TEST-1-R

H2
TEST-1-R

H3
TEST-1-R

H4
TEST-1-R

H5
TEST-1-R

H6
TEST-1-R

OpuLinks
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Title History		
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