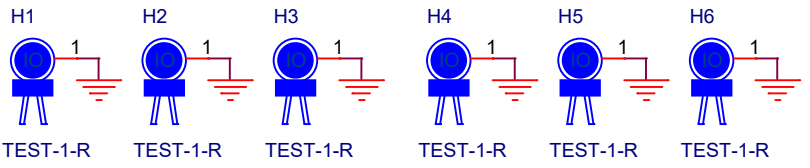
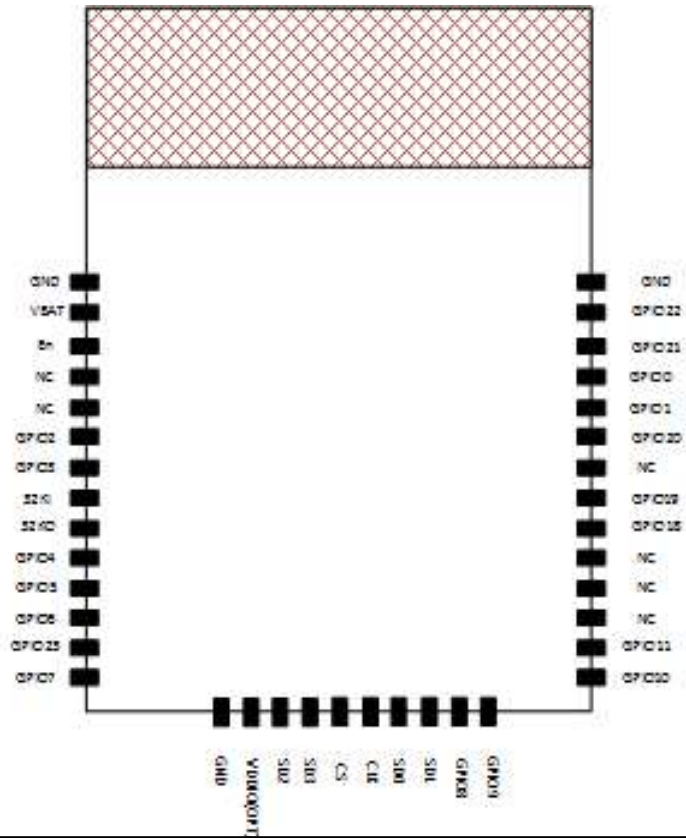
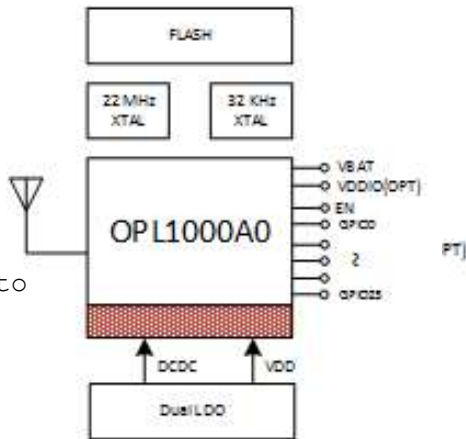
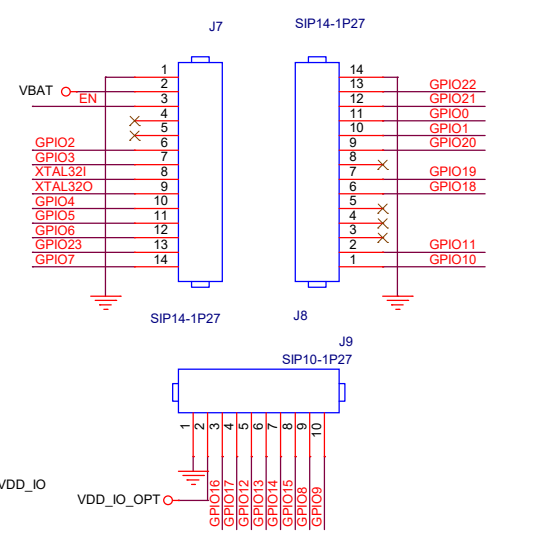
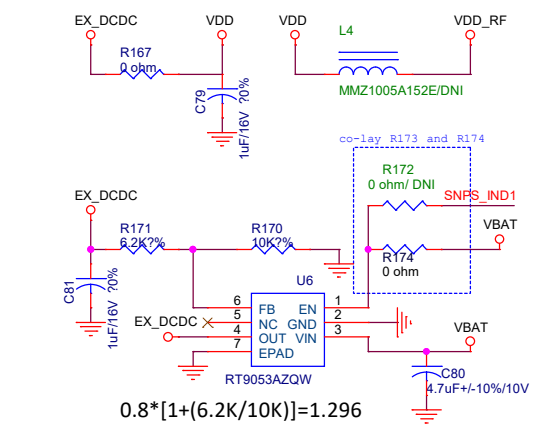
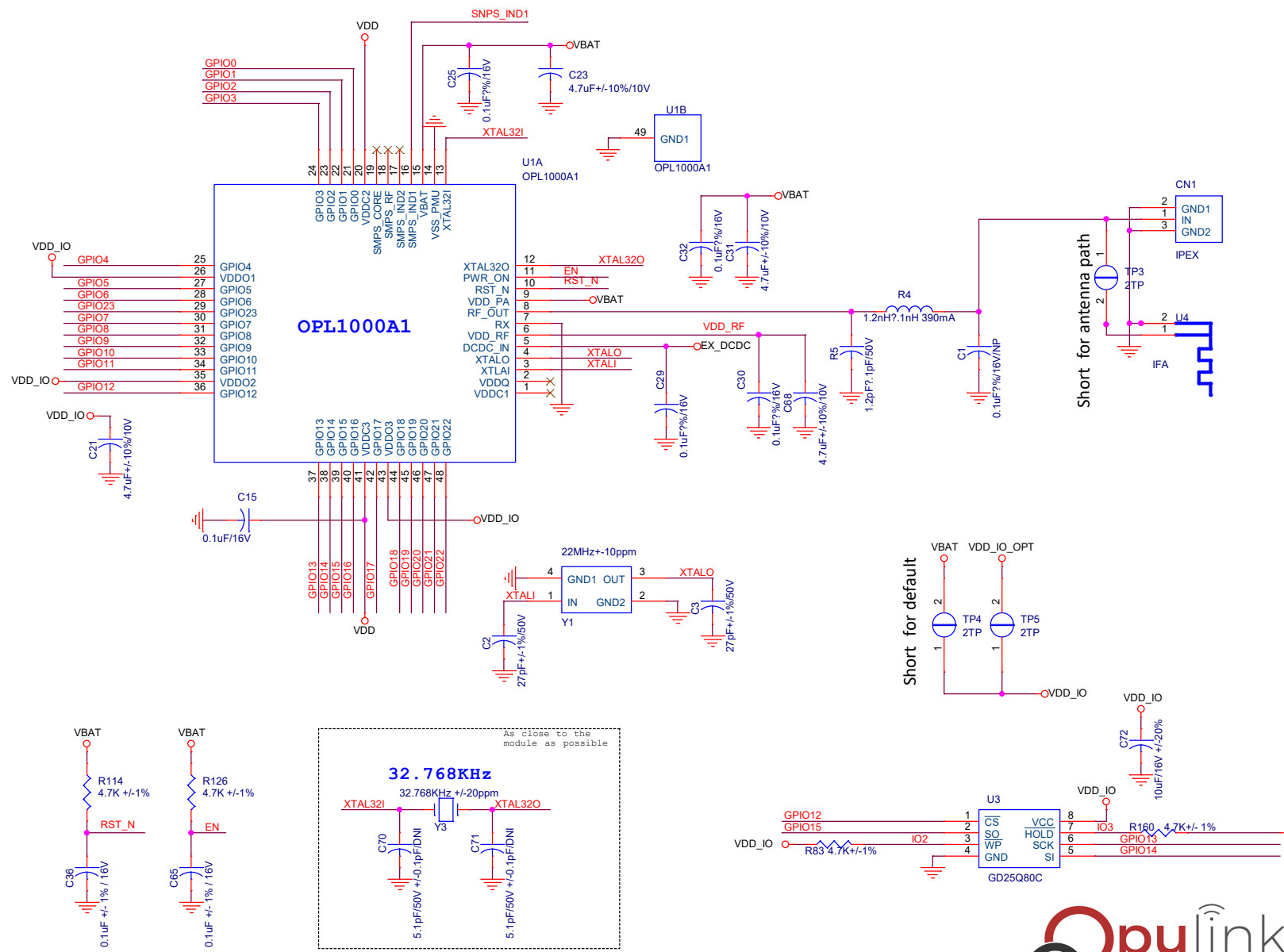


Date	Description
2018/01/23	Initial
2018/02/07	1. move out flash, 32K XTAL, C24
2018/06/15	1. Change to A1 version
2018/09/10	1. C26,C27 C28 DNI 2. Add C68, C69 L3 CN1 3. remove R3 R6 4. C14 change to 4.7uF 5. Add pi circuit on pin19,pin20
2018/10/29	1. Add Flash, 32K XTAL, RST, EN circuit
2018/11/08	1. remove C18,R82,R87,R88 (Flash part) 2. remove C20,C16, change C21 to 4,7uF 3. remove C18, change C72 to 10uF 4. remove D1,D2,C28,C26,C27 5. Change 32.768 XTAL 6. Change C70,C71 to 5.1pF
2018/12/03	1. remove C67 (Buck FB)
2018/12/22	1. Add U6/U7 LDO device 2. Remove TP2 and change TP3 circuit
2019/01/04	1. Reserve C82,C83
2019/02/14	1. R4 change to 1.2nH 2. R5 change to 1.2pF 3. L2,C14, C7 DNI
2019/03/07	1. Remove C78, R168, U7 2. R171 change to 6.2K 3. R167 change to 0 ohm
2019/03/21	1. Reserve L3 component
2019/03/22	1. Reserve L4 component for VDD connection with VDD_RF 2. Add R172 for SMPS_IND1 trace to connect with LDO enable pin 3. Remove C82, c83
2019/04/01	1. Remove L2, L3, C7, C14, C69

OPL1000 A1 Module



Title		
History		
Size A	Document Number <Doc>	Rev V1.1
Date:	Monday, April 01, 2019	Sheet 1 of 2



Title			
OPL1000_A1_Module			
Size	Document Number		Rev
B	<Doc>		V1.1
Date:	Monday, April 01, 2019	Sheet	2 of 2