SSW101B
Single-chip IEEE 802.11b/g/n 1T1R Wireless Network Controller with USB Interface

Data Sheet Version 1.3

REVISION HISTORY

Revision No.	Description	Date
1.0	• Initial release	12/21/2018
1.1	• Updated GPIO maximum current in DC Electrical Characteristics	05/05/2019
1.2	• Updated Block Diagram	10/14/2019
1.3	• Updated for clarity	11/20/2019

1. OVERVIEW

1.1. General Description

The SSW101B is a highly integrated Wi-Fi single chip which includes one spatial stream transmission, short guard interval (400ns GI), and transmission over 20MHz and 40MHz bandwidth. SSW101B fully supports all data rates of IEEE 802.11b, 802.11g, and 802.11n. SSW101B WLAN MAC supports 802.11e for multimedia applications, 802.11i security, and 802.11n for enhanced MAC protocol efficiency. Frame aggregation techniques such as A-MPDU are also supported for improving throughput performance. The SSW101B is designed to support standard based features in the areas of security, being fully compatible with WiFi- Alliance, WMM, WPS and P2P specifications, giving end users the greatest performance any time and in any circumstance.

1.2. Block Diagram

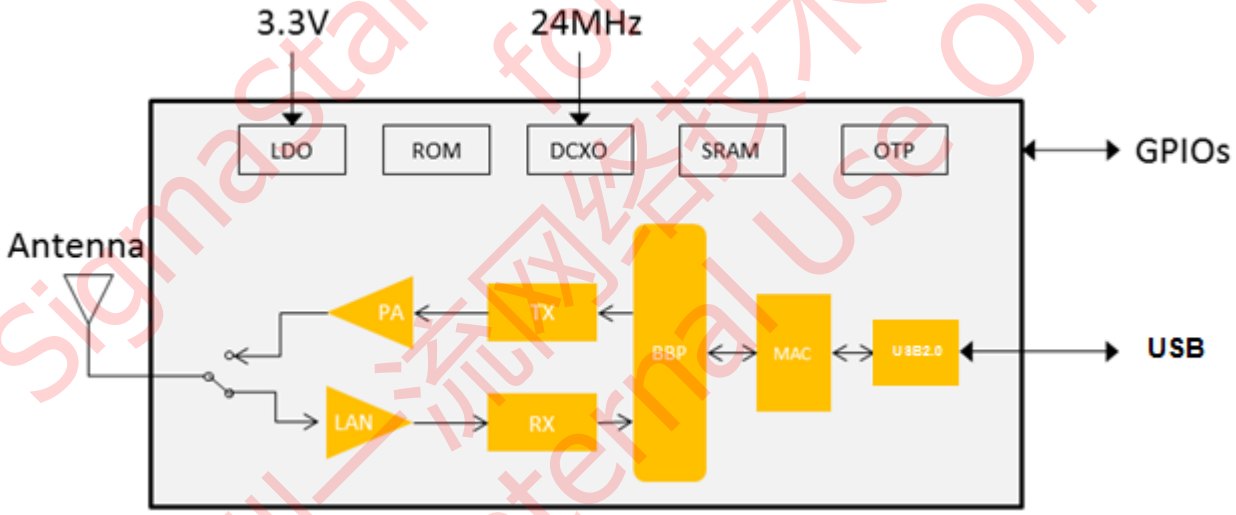

Figure 1: SSW101B Block Diagram

1.3. SSW101B Feature List

- IEEE 802.11 b/g/n/e/i/n/w client
- Embedded high-performance 32-bit RISC microprocessor speed up to 150MHz
- Highly integrated RF with 40nm CMOS technology
- WLAM MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip
- Integrated PA, LNA, Balun and T/R switch
- Support A-MPDU transmit and receive for throughput improvement
- Support A-MSDU reception
- Support STBC stream reception
- Support Short-GI of 802.11n
- Supports both 20MHz and 40MHz bandwidth transmission
- 4x4mm^2, 28pin QFN package
- Security support Hardware Crypto Engine for Advanced Fast Security, Including WEP, TKIP, AES and 802.11w
- USB device interface speed up to 480Mbps
- Supports STA and AP mode
- Support 24.0MHz crystal as default with internal oscillator
- Auto-calibration

2. PIN INFORMATION

2.1. Pin Map

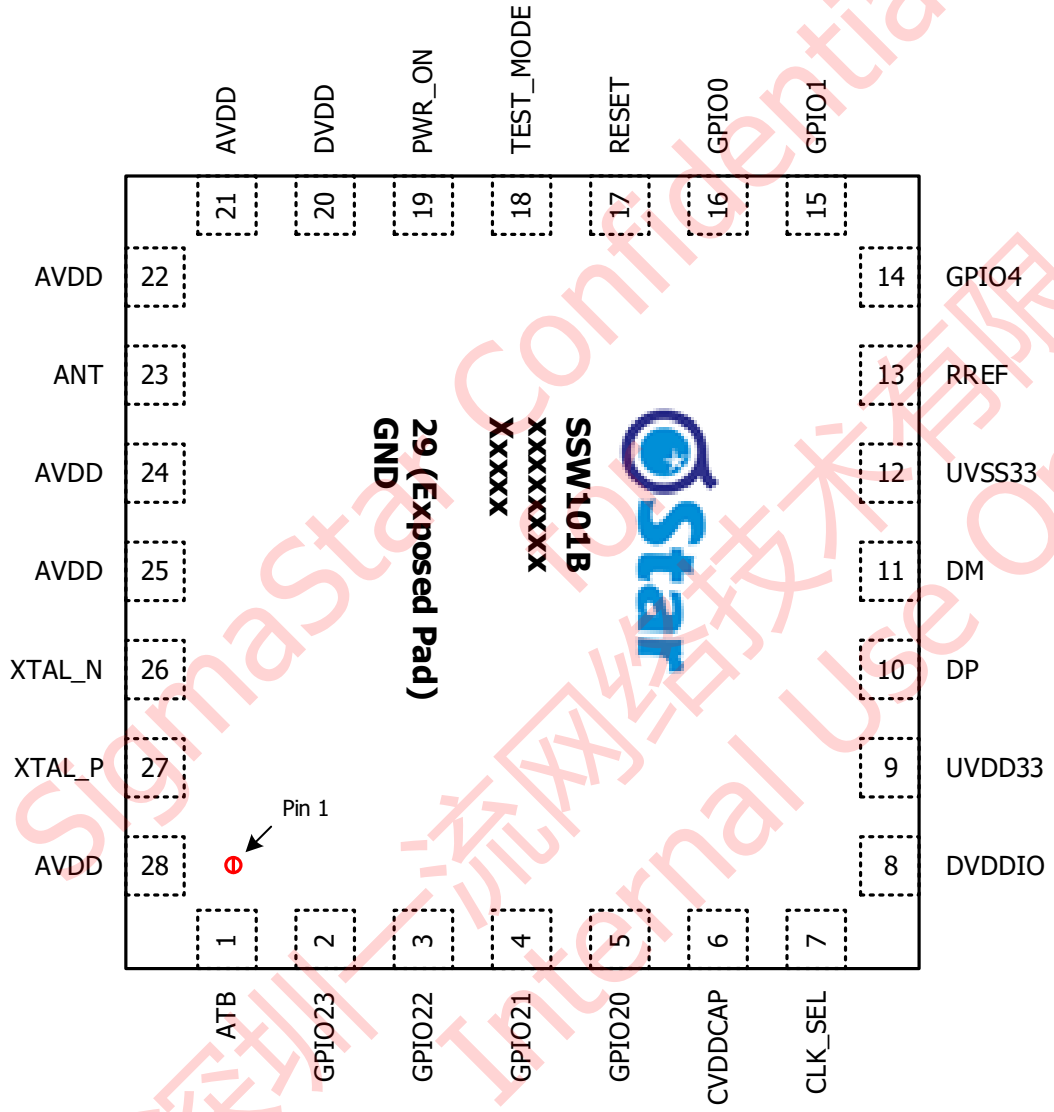

Figure 2: SSW101B Pin Map (Top View)

2.2. Pin Table

Pin Number	Pin Name	Type	Pin Description
Test			
1	ATB	Output	test pin
18	TEST_MODE	Input	Test mode selection, let it floating in normal mode.
USB interface			
10	DP	I/O	USB2.0 DP
11	DM	I/O	USB2.0 DM
13	RREF	Output	Bias resistor for USB block Requirement: 12kohm (±1%)
Power supply			
6	CVDDCAP	PWR	VDD1.1V for digital core. It is only connected with decouple capacitance. Digital core power is supplied by LDO on chip to reduce power source for BOM cost reduction.
8	DVDDIO	PWR	VDD 3.3V for digital IO
9	UVDD33	PWR	VDD 3.3V for USB transceiver
20	DVDD	PWR	VDD 3.3V for digital
21	AVDD	PWR	VDD 3.3V for analog
22	AVDD	PWR	VDD 3.3V for analog
24	AVDD	PWR	VDD 3.3V for analog
25	AVDD	PWR	VDD 3.3V for analog
28	AVDD	PWR	VDD 3.3V for analog
GPIO			
2	GPIO23	I/O	UART[2] RTS/; SPI[2] CS; I2C[2] SCL; GPIO; PWM
3	GPIO22	I/O	UART[2] CTS/;SPI[2] MOSI; I2C[2] SDA; GPIO; PWM
4	GPIO21	I/O	UART[2] TXD; SPI[2] MISO; GPIO; PWM
5	GPIO20	I/O	UART[2] RXD; SPI[2] CLK; GPIO; PWM
14	GPIO4	I/O	GPIO
15	GPIO1	I/O	UART[1] TXD; GPIO; PWM； I2C SCL;
16	GPIO0	I/O	UART[1] RXD; GPIO; PWM; I2C SDA;
Power control			
17	RESET	Input	Hardware reset pin, low active
19	PWR_ON	Input	Power enable pin, low level is chip power down

Pin Number	Pin Name	Type	Pin Description
Clock			
7	CLK_SEL	Input	If uses 24MHz crystal, let it floating
26	XTAL_N	Output	Oscillator output
27	XTAL_P	Input	Oscillator input
Antenna interface			
23	ANT	I/O	2.4GHz radio signal input/output from/to antenna
GND			
12	UVSS33	GND	Ground for USB transceiver
29 (Exposed Pad)	GND	GND	Ground for power supplies

3. ELECTRICAL CHARACTERISTICS

3.1. Recommended Operating conditions

Parameter	Description	Min	Max	Unit
DVDDIO UVDD33 DVDD	Digital 3.3V power supplies voltage	-0.2	5.0	V
AVDD	Analog 3.3V power supplies voltage	-0.2	5.0	V
T_{stg}	Storage temperature	-60	150	°C
T_j	Junction temperature		125	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded.

3.2. Thermal Data

Parameter	Description	Value	Unit
T_{oper}	Operating ambient temperature range	-40 ~ +85	°C
R_{thjc}	Junction-case thermal resistance	15.5	°C/W
R_{thja}	Junction-ambient thermal resistance	30.8	°C/W

3.3. DC Electrical Specifications

Parameter	Description	Min	Typical	Max	Unit
UVDD33	USB transceiver operating voltage	2.98	3.3	3.63	V
AVDD	Analog module 3.3V operating voltage	2.98	3.3	3.63	V
DVDDIO DVDD	Digital module 3.3V operation voltage	2.98	3.3	3.63	V
V_{IL} V_{IH}	Low level input voltage (I, I/O) High level input voltage (I, I/O)	-02 2.0		0.8 3.6	V V
V_{T+} V_{T-}	Schmitt trig Low to High threshold (I, I/O) Schmitt trig High to Low threshold (I, I/O)	1.54 0.95	1.65 1.02	1.74 1.09	V V
V_{OL} V_{OH}	Low level output voltage (O, I/O) High level output voltage (O, I/O)	 2.4		0.4	V V
I_{GPO}	GPOs, STATUS			9.5	mA

Note: Exposure beyond recommended operating conditions may affect device reliability.

3.4. Requirements to Peripheral Circuits

3.4.1 Power Supply Recommendation

Power Module	Parameter	Requirement	Unit
3.3V power supply	Rated voltage	3.3	V
	Voltage tolerance	≤10	%
	Rated current	≥400	mA
	Ripple	<115	mV

3.4.2 External Crystal

Note: If a 24MHz external crystal is used, the specification of the crystal should be as below:

Parameter	Description	Min	Typ	Max	Unit
Frequency	Nominal frequency		24.0000		MHz
Tolerance	Frequency measured at 25°C±3°C		±10	±20	ppm
ESR	Equivalent series resistance			40	Ω
C_{Load}	Load capacitance	8	15	16	pF
C_{Shunt}	Shunt capacitance		5		pF
DL	Drive level		120		μW
Aging	Aging per year in 10 years		±5		ppm
Temp Drift	Drift of frequency over the operating temperature range			±20	ppm

Note: If a 40MHz external crystal is used, the specification of the crystal should be as below:

Parameter	Description	Min	Typ	Max	Unit
Frequency	Nominal frequency		40.0000		MHz
Tolerance	Frequency measured at 25°C±3°C		±10	±20	ppm
ESR	Equivalent series resistance			40	Ω
C_{Load}	Load capacitance	8	15	16	pF
C_{Shunt}	Shunt capacitance		5		pF
DL	Drive level		120		μW
Aging	Aging per year in 10 years		±5		ppm
Temp Drift	Drift of frequency over the operating temperature range			±20	ppm

4. PERIPHERAL INTERFACE

4.1. GPIO interface

SSW101B has seven GPIO pins, which can be assigned as different functions by registers setting. When these pins are used as GPIO, they may be assigned as High/Low voltage level input/output. When these GPIO pins are used as GPIO input, High/Low input voltage level on GPIOs can be read by registers to trigger CPU interruption. The GPIO pin's map is shown in Table 1.

Table 1: GPIO Interface Definition

Pin Number	Pin Name	I2C	UART	SPI	GPIO	PWM
2	GPIO23	I2C[2] SCL	UART[2] RTS/	SPI[2] CS/	Available	Available
3	GPIO22	I2C[2] SDA	UART[2] CTS/	SPI[2] MOSI	Available	Available
4	GPIO21		UART[2] TXD	SPI[2] MISO	Available	Available
5	GPIO20		UART[2] RXD	SPI[2] CLK	Available	Available
14	GPIO4				Available	
15	GPIO1	I2C[1] SCL	UART[1] TXD		Available	Available
16	GPIO0	I2C[1] SDA	UART[1] RXD		Available	Available

4.2. USB interface

SSW101B provides one USB interface as shown in Table 2. Pin[13] RREF should connect to a 12kohm (±1%) bias resister for USB block.

Table 2: USB Interface Definition

Pin Number	Pin Name	Function
9	UVDD33	3.3V VCC
10	DP	USB DP (D+)
11	DM	USB DM (D-)
12	UVSS33	GND

4.3. Clock frequency selection

SSW101B uses external 24MHz crystal as default. On the other hand, SSW101B can also use 40MHz crystal and external clock or oscillator clock input from XTAL_P pin, controlled by strapping pin as shown in Table 3. These strapping pins could connect to GND or I/O power supply directly without resistors.

Table 3: Clock Frequency Selection

Clock type	CLK_SEL Pin [7]	GPIO22 Pin [3]	GPIO23 Pin [2]
24MHz crystal (default)	NC (pull-up internally)	Optional	Optional
40MHz crystal	Low	Low	High
24MHz crystal	Low	Low	Low
40MHz external clock or oscillator	Low	High	High
24MHz external clock or oscillator	Low	High	Low

4.4. I2C interface

SSW101B provides two groups of I2C interface, please refer to the following Table 4 for detailed information.

Table 4: I2C interface definition

Pin Number	Pin Name	Group	Function
2	GPIO23	#2	I2C SCL
3	GPIO22	#2	I2C SDA
15	GPIO1	#1	I2C SCL
16	GPIO0	#1	I2C SDA

4.5. UART interface

SSW101B provides two groups of UART interface, the interface definition is shown in Table 5.

Table 5: UART interface definition

Pin Number	Pin Name	Group	Function
2	GPIO23	#2	UART RTS/
3	GPIO22	#2	UART CTS/
4	GPIO21	#2	UART TXD
5	GPIO20	#2	UART RXD
15	GPIO1	#1	UART TXD
16	GPIO0	#1	UART RXD

Both two groups of UART interfaces support 2.5Mbps or higher data rate. It is recommended that UART group #1 is used to print debug information and UART group #2 is used for data transmission.

4.6. PWM interface

All GPIOs except Pin[14] GPIO4 can be used as PWM output interface, please refer to Table 4-1 for detailed information.

5. INTERFACE TIMING SPECIFICATION

5.1. USB Attach and HS Handshake Behaviors

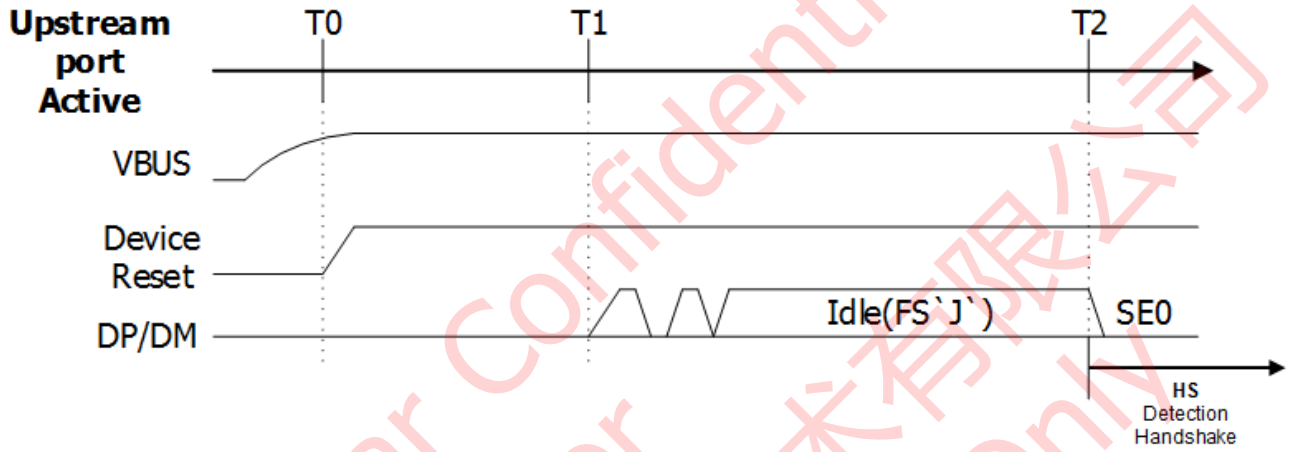

Figure 3: USB Attach Behavior

USB reset timing values is shown as below.

Timing Parameter	Description	Value
T0	VBUS valid	0(Reference)
T1	Maximum time from the VBUS valid(>4.01V) to when the device signals the attachment.	T0+100ms{Tsigatt}>T1
T2(HS Reset T0)	De-bounce interval The device enters the HS detection handshake protocol	T1+100ms{Tattdb}<T2

5.2. HS Handshake Detection

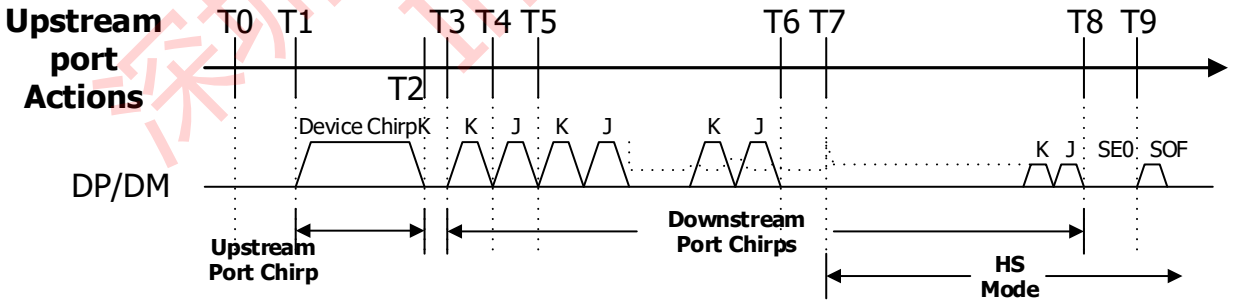

Figure 4: HS Detection Handshake Timing Behavior

Reset timing values are shown as below.

Timing Parameter	Description	Value
T0	HS handshake begins. D+ pull-up is enabled; HS termination is disabled.	0(Reference)
T1	Device asserts Chirp-K on the bus.	T0<T1<HS Reset T0+6ms {Tuchend-Tuch}
T2	Device removes Chirp-K from the bus. Minimum width:1.0ms	T0+1.0ms{Tuch}<T2<HS Reset T0+7.0ms{Tuchend}
T3	The downstream port asserts Chirp-K on the bus.	T2<T3<T2+100us{Twtdch}
T4	The downstream port toggles Chirp-K to Chirp-J on the bus.	T3+40us{Tdchbit(Min.)}<T4<T3+60us{Tdchbit(Max.)}
T5	The downstream port toggles Chirp-J to Chirp-K on the bus.	T4+40us{Tdchbit(Min.)}<T5<T6+60us{Tdchbit(Max.)}
T6	Device detects the downstream port chirp.	T6
T7	Downstream port chirp detected by the device Device removes D+ pull-up, asserts HS terminations, reverts to the HS default state, and waits for the end of a reset.	T6<T7<T6+500us{T{wths}}
T8	Terminate downstream port Chirp K-J sequence (Repeating T4 and T5)	T9-500us{Tdchse0(Max.)}<T8<T9-100us{Tdchse0(Min.)}
T9	The earliest time that the downstream port may end the reset; and the latest time at which the device may remove the D+ pull-up, assert the HS terminations, and revert to the HS default state.	HS resets T0+10ms{Tdrst(Min.)}

6. MECHANICAL DIMENSIONS

6.1. Chip Package Drawing

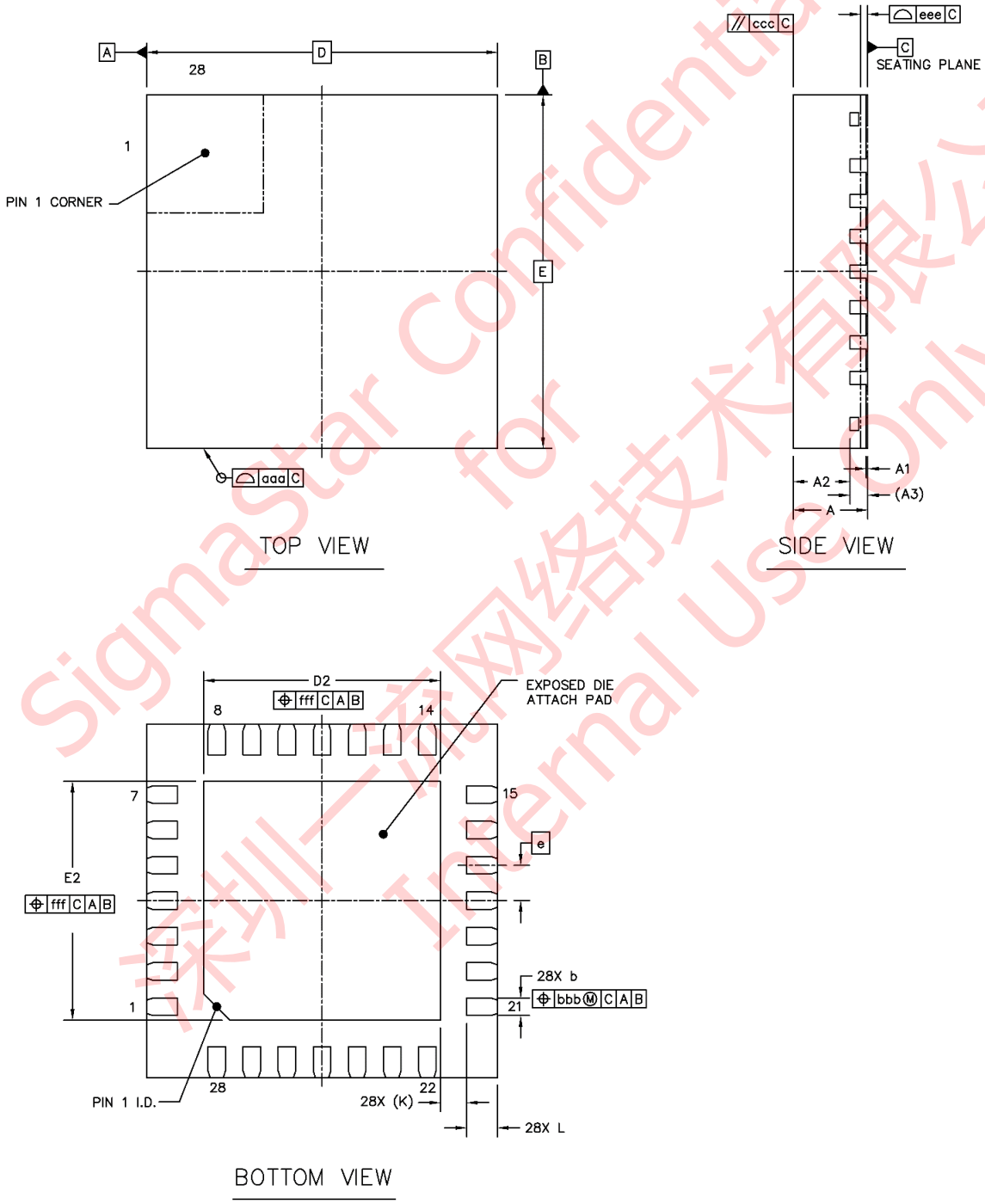

Figure 5: SSW101B Package Drawing

6.2. Dimensions of Packaging Parameters

		SYMBOL	MIM	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.647	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.6	2.7	EP SIZE
	Y	E2	2.6	2.7	
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSE PAD OFFSET		fff		0.1	

UNIT: mm

7. SOLDER REFLOW PROFILE

7.1. Package Peak Reflow Temperature

SSW101B is assembled in a lead-free QFN28 package. Since its size is 4×4×0.85mm3, the volume and thickness is in the category of volume<350mm3 and thickness<1.6mm in Table 4-2 of IPC/JEDEC J-STD-020C. Accordingly, the peak reflow temperature (Tp) is 260°C.

7.2. Classification Reflow Profile

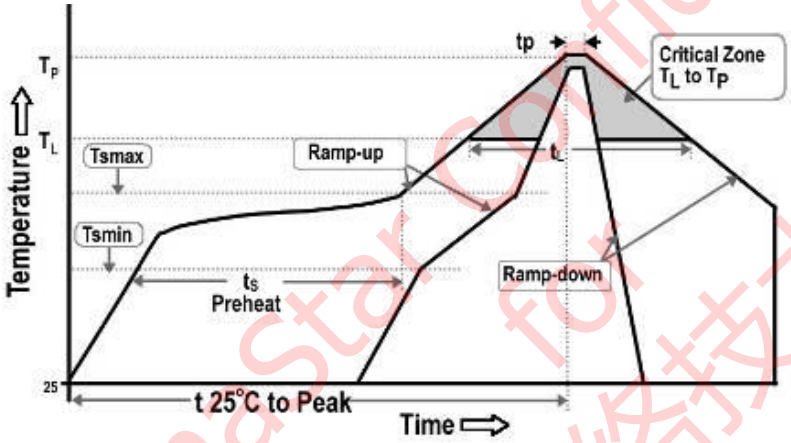

Figure 6: SSW101B Reflow Profile

Profile Feature		Specification*
Average ramp-up rate (t_{smax} to t_P)		3°C/second max.
Pre-heat	Minimal temperature (T_{smin})	150°C
	Maximal temperature (T_{smax})	200°C
	Time (t_s)	60~180 seconds
Time maintained above	Temperature (T_L)	217°C
	Time (t_L)	60~150 seconds
Peak/Classification temperature (T_P)		260°C
Time within 5°C of actual peak temperature (t_P)		20~40 seconds
Ramp-down rate		6°C/second max.
Time 25°C to peak temperature		8 minutes max.

*** Note: all temperatures are measured on the top surface of the package.**

7.3. Maximum Reflow Times

All package reliability tests are performed, and they pass the tests with a pre-condition procedure that repeats the above reflow profile, **three (3)** times.