DIGITAL LOGIC & DESIGN (EE-1005)
ASSIGNMENT #4

ID: _____
NAME: _____
SECTION: ____
Read the Instructions Carefully NO Marks will be given if you failed to follow instructions

❖ Your assigned number is given to you in excel sheet provided with the assignment **FOR**

EXAMPLE: Assigned Number if your assigned number is **9846**

	Assign Digit 0	Assign Digit 1	Assign Digit 2	Assign Digit 3
Short for Assigned Digit	**A0**	**A1**	**A2**	**A3**
Write Assigned Number Digit By Digit	9	8	4	6

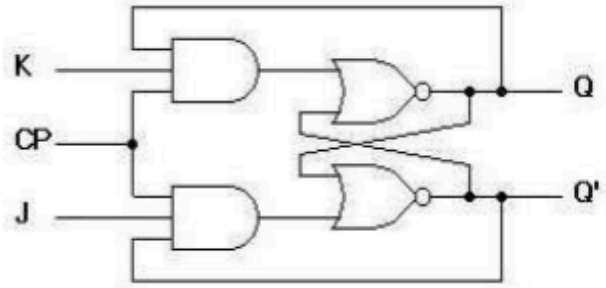
FOR EXAMPLE: Name is **HAMZA DAUD**

	ZERO CHARACTER OF YOUR NAME	FIRST CHARACTER OF YOUR NAME	SECOND CHARACTER OF YOUR NAME	THIRD CHARACTER OF YOUR NAME	FOURTH CHARACTER OF YOUR NAME
Short for CHARACTER	**F0**	**F1**	**F2**	**F3**	**F4**
YOUR NAME CHARACTER BY CHARACTER	H	A	M	Z	a
	ZERO CHARACTER OF YOURS SECOND NAME	**FIRST CHARACTER OF YOUR SECOND NAME**	**SECOND CHARACTER OF YOUR SECOND NAME**	**THIRD CHARACTER OF YOUR SECOND NAME**	**FOURTH CHARACTER OF YOUR SECOND NAME**
Short for CHARACTER	**S0**	**S1**	**S2**	**S3**	**S4**
YOUR NAME CHARACTER BY CHARACTER	D	@	U	d	z

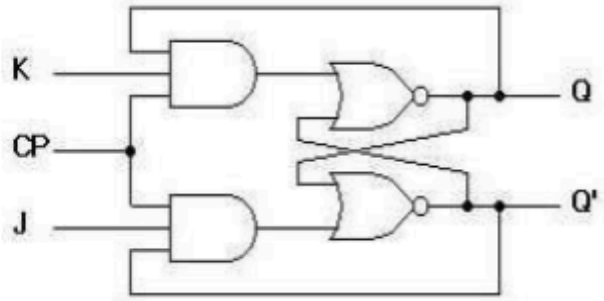
1. Process the POSITVE CLOCK EDGE **JK FLIP FLOP** circuit given below for all possible cases and fill the table accordingly?

CIRCUIT:

CLK=0

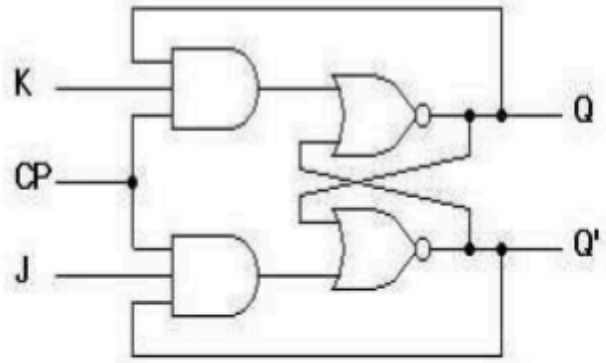


CLK=1

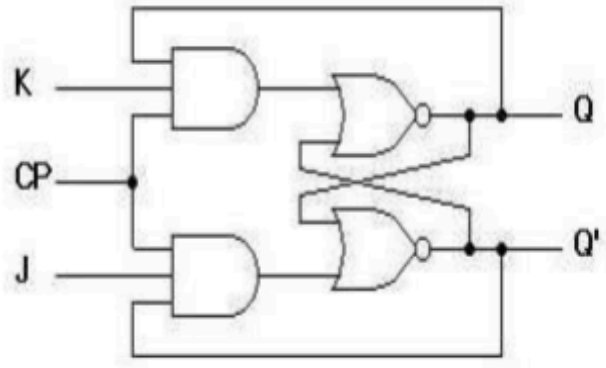


CASE I

J=0,K=0,Q=0

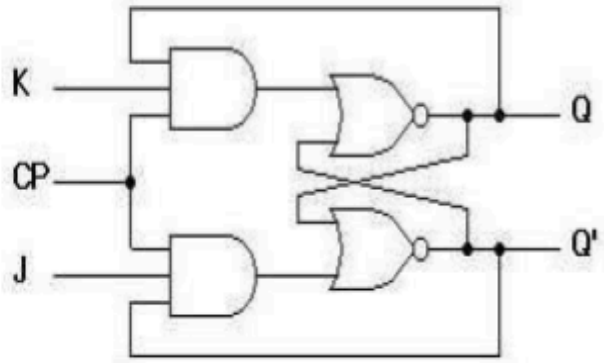


J=0,K=1,Q=0

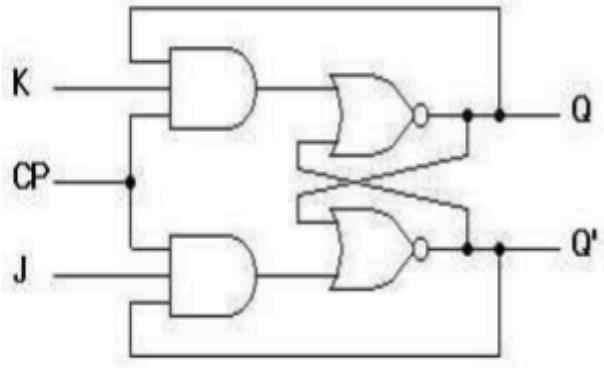


CASE-II

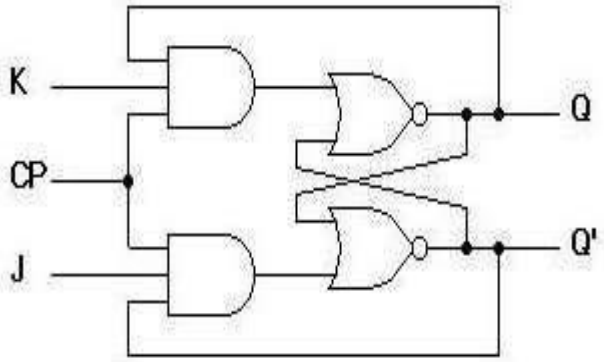
J=0,K=0,Q=1



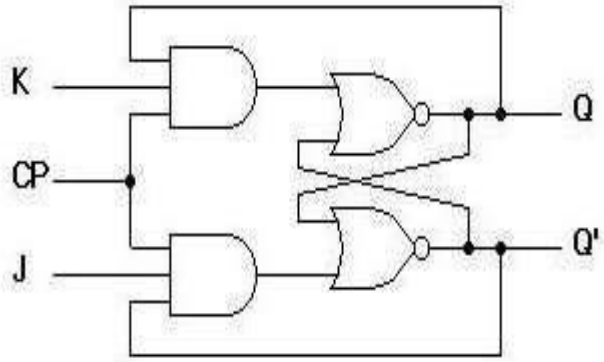
J=0,K=1,Q=1



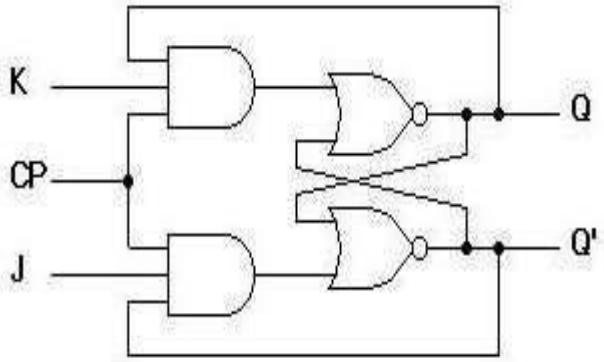
J=1,K=0,Q=0



J=1,K=0,Q=1



J=1,K=1,Q=0



J=1,K=1,Q=1

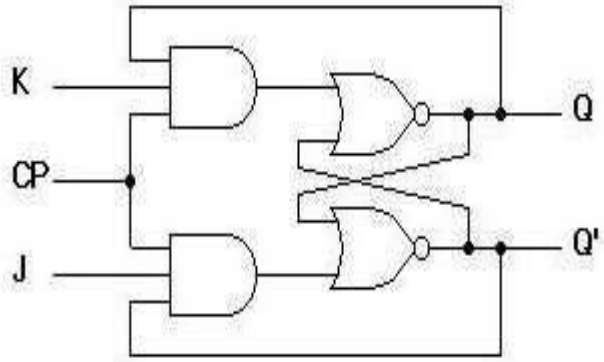


TABLE:

CLK	J	K	Q_{t+1}	$\bar{\bar{Q}}_{t+1}$
0	X	X		
1	X	X		
↑	0	0		
↑	0	1		
↑	1	0		
↑	1	1		

2. Modify given circuit to introduce Asynchronous **CLEAR** and **SET** inputs fill table?

HINT: For reference kindly read Section **7-2** of DIGITAL FUNDAMENTAL by Thomas Floyd, 10th Edition

CIRCUIT:

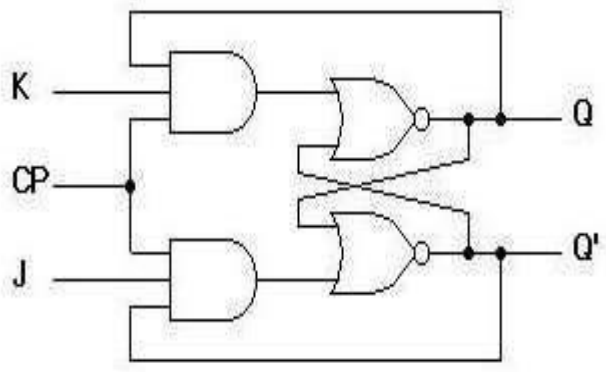


TABLE:

SET	CLEAR	Q_{t+1}	Q_{t+1}
0	0		
0	1		
1	0		
1	1		

3. For the given state table perform all of the following.

NOTE: *Rename states in the table given below as a= **F0**, b= **S0**, c=**F1**, d= **S1**, e=**F2**, f= **S2**, g=**F3**, h= **S3** and then perform following operations*

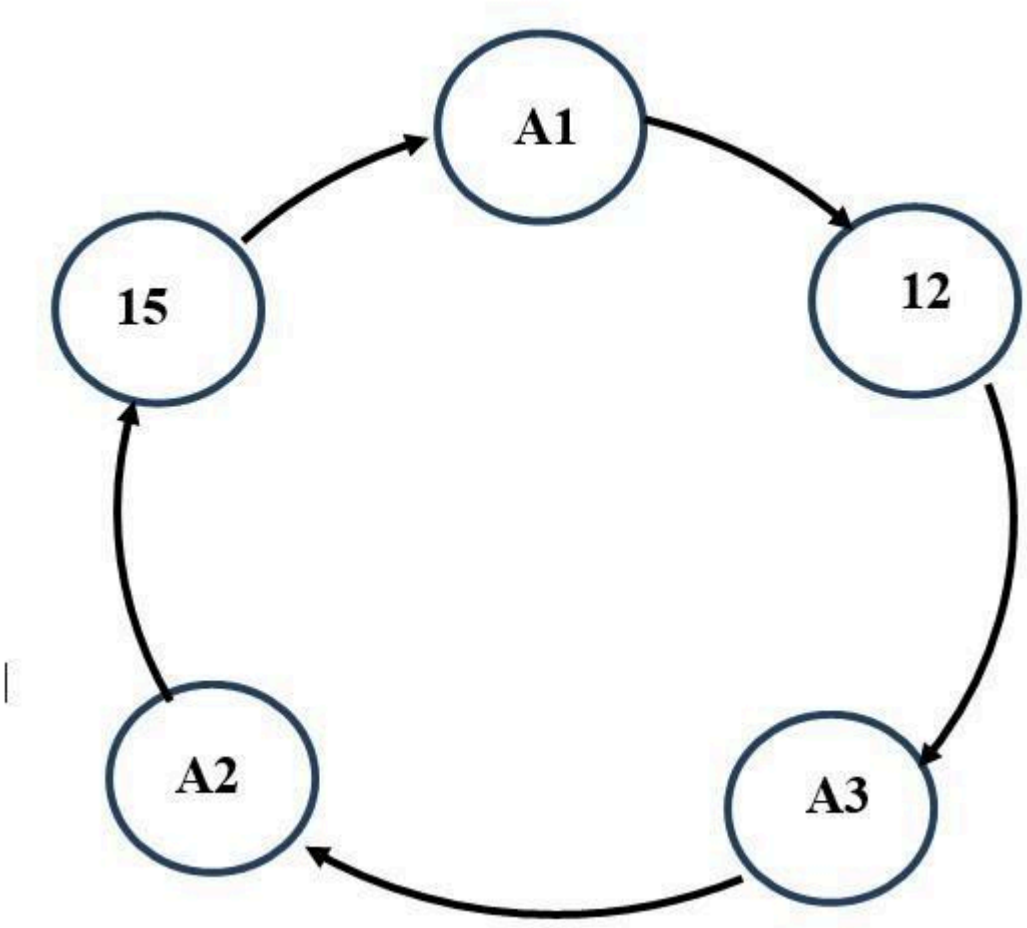
✔ Draw the corresponding state diagram

TABLE:

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

STATE TRANSITION DIAGRAM:

4. Design circuit for given state diagram using **T Flip-Flop**?



TABLE, SIMPLIFICATION & EXPRESSIONS

5. Draw a three bit UP-DOWN Counter. For each bit you will have to use a different flip flop (JK, T, D). Follow the steps properly.

- State Diagram
- Next State Table
- State Reduction And Assignment
- Flip Flop Transition Table (FLIP FLOP Selection)
- Simplification
- Input/output Equations
- Implementations of Equation(Logic Diagram)

To decide which flip flop to use for your counter is based on your assigned number. Assume that JK<T<D. This means JK is the smallest, T flip flop is middle one and D flip flop is biggest one. Now based on the first 3 digits of your assigned number you will decide the pattern. For example, the id assigned number is **948**6, then pick the first three digits like 948. Since the first digit is the biggest so D flip flop should be used first. 4 is the smallest, so JK should be used in the middle and T flip flop should be used in the end.

6. A sequential circuit shown in the given figure has three D flip-flops Do, D_1 and D_2 , two inputs X and Y, and outputs Z_1 and Z_2.

- ✔ Derive the STATE EQUATIONS
- ✔ Tabulate the STATE TABLE.
- ✔ Draw the **STATE DIAGRAM** of the circuit