DIGITAL LOGIC & DESIGN (EE-1005)
ASSIGNMENT #4

ID: 23i-2623
NAME: Muneeb Lone
SECTION: B
Read the Instructions Carefully NO Marks will be given if you failed to follow instructions

❖ Your assigned number is given to you in excel sheet provided with the assignment **FOR**

EXAMPLE: Assigned Number if your assigned number is **9846**

	Assign Digit 0	Assign Digit 1	Assign Digit 2	Assign Digit 3
Short for Assigned Digit	A0	A1	A2	A3
Write Assigned Number Digit By Digit	7	6	5	0

FOR EXAMPLE: Name is **HAMZA DAUD**

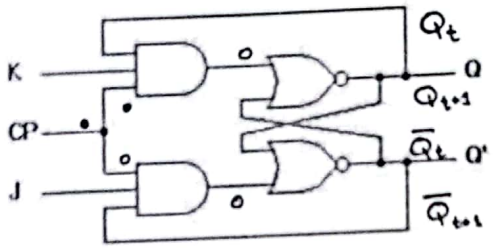
	ZERO CHARACTER OF YOUR NAME	FIRST CHARACTER OF YOUR NAME	SECOND CHARACTER OF YOUR NAME	THIRD CHARACTER OF YOUR NAME	FOURTH CHARACTER OF YOUR NAME
Short for CHARACTER	F0	F1	F2	F3	F4
YOUR NAME CHARACTER BY CHARACTER	M	U	N	E	e
	ZERO CHARACTER OF YOURS SECOND NAME	FIRST CHARACTER OF YOUR SECOND NAME	SECOND CHARACTER OF YOUR SECOND NAME	THIRD CHARACTER OF YOUR SECOND NAME	FOURTH CHARACTER OF YOUR SECOND NAME
Short for CHARACTER	S0	S1	S2	S3	S4
YOUR NAME CHARACTER BY CHARACTER	L	O	n	E	

ID: ASSIGNMENT # 4 [EE-227] Assigned Number:

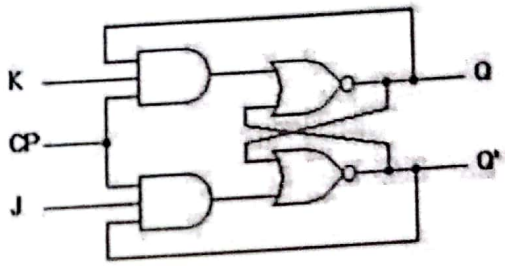
1. Process the POSITVE CLOCK EDGE **JK FLIP FLOP** circuit given below for all possible cases and fill the table accordingly?

CIRCUIT:

CLK=0

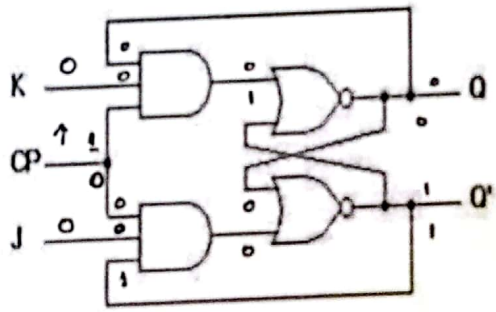


CLK=1

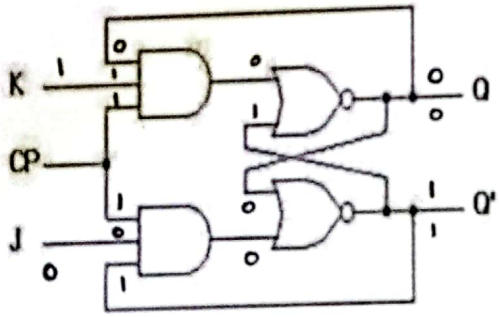


CASE I

J=0,K=0,Q=0

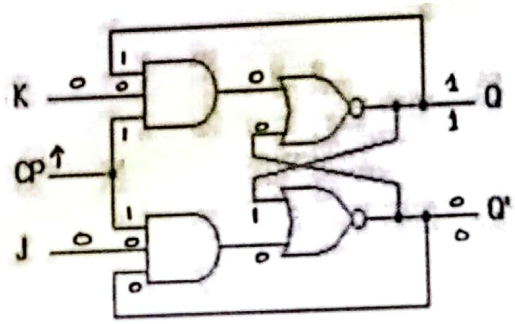


J=0,K=1,Q=0

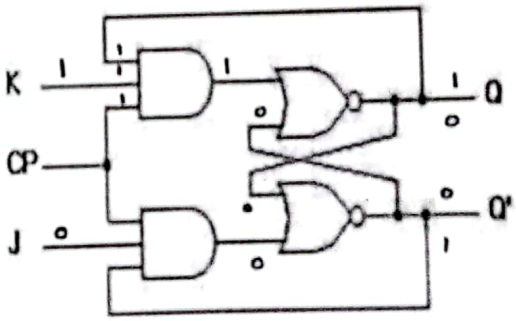


CASE-II

J=0,K=0,Q=1



J=0,K=1,Q=1



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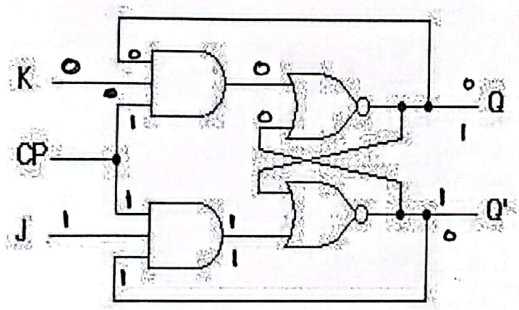
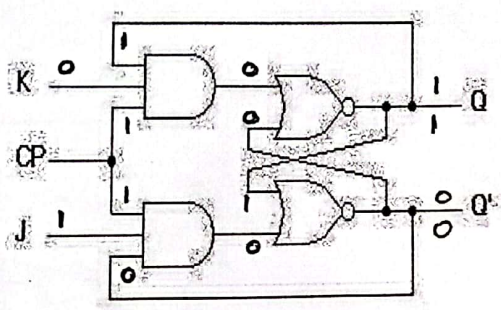
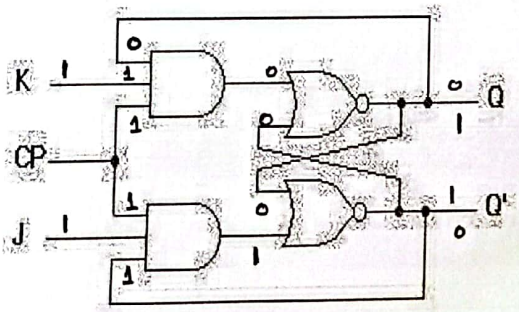
J=1,K=0,Q=0



J=1,K=0,Q=1



J=1,K=1,Q=0



J=1,K=1,Q=1

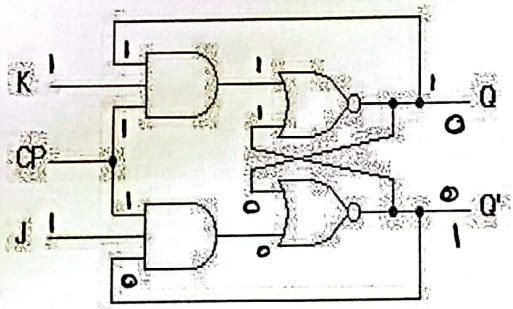


TABLE:

CLK	J	K	Q_{t+1}	$\bar{Q}_{t+1}$
0	X	X	Q_t	$\overline{Q_t}$
1	X	X	Q_t	$\overline{Q_t}$
↑	0	0	Q_t	$\overline{Q_t}$
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	$\overline{Q_t}$	Q_t

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2. Modify given circuit to introduce Asynchronous **CLEAR** and **SET** inputs fill table?
HINT: For reference kindly read Section **7-2** of DIGITAL FUNDAMENTAL by Thomas Floyd, 10th Edition

CIRCUIT:

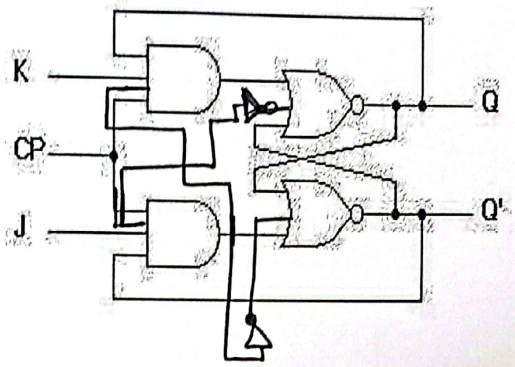

TABLE:

SET	CLEAR	Q_{t+1}	$\bar{Q}_{t+1}$
0	0	invalid	invalid
0	1	0	1
1	0	1	0
1	1	Depends on JK Inputs	

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3. For the given state table perform all of the following.

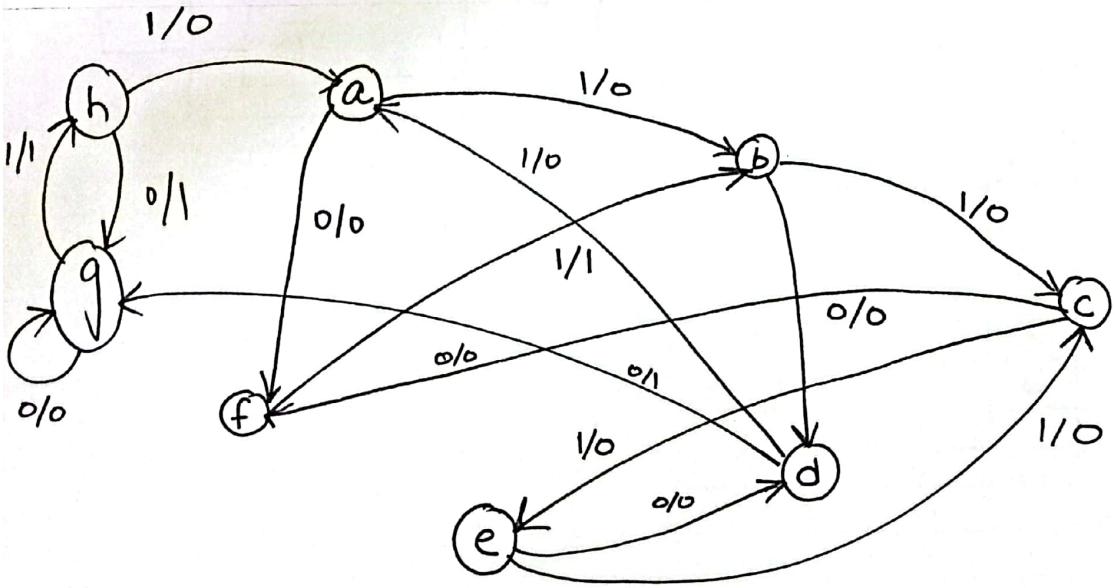
NOTE: *Rename states in the table given below as a= **F0**, b= **S0**, c=**F1**, d= **S1**, e=**F2**, f= **S2**, g=**F3**, h= **S3** and then perform following operations*

✔ Draw the corresponding state diagram

TABLE:

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
$a \rightarrow$M	f	b	0	0
$b \rightarrow$L	d	c	0	0
$c \rightarrow$U	f	e	0	0
$d \rightarrow$O	g	a	1	0
$e \rightarrow$N	d	c	0	0
$f \rightarrow$∩	f	b	1	1
$g \rightarrow$E	g	h	0	1
$h \rightarrow$∃	g	a	1	0

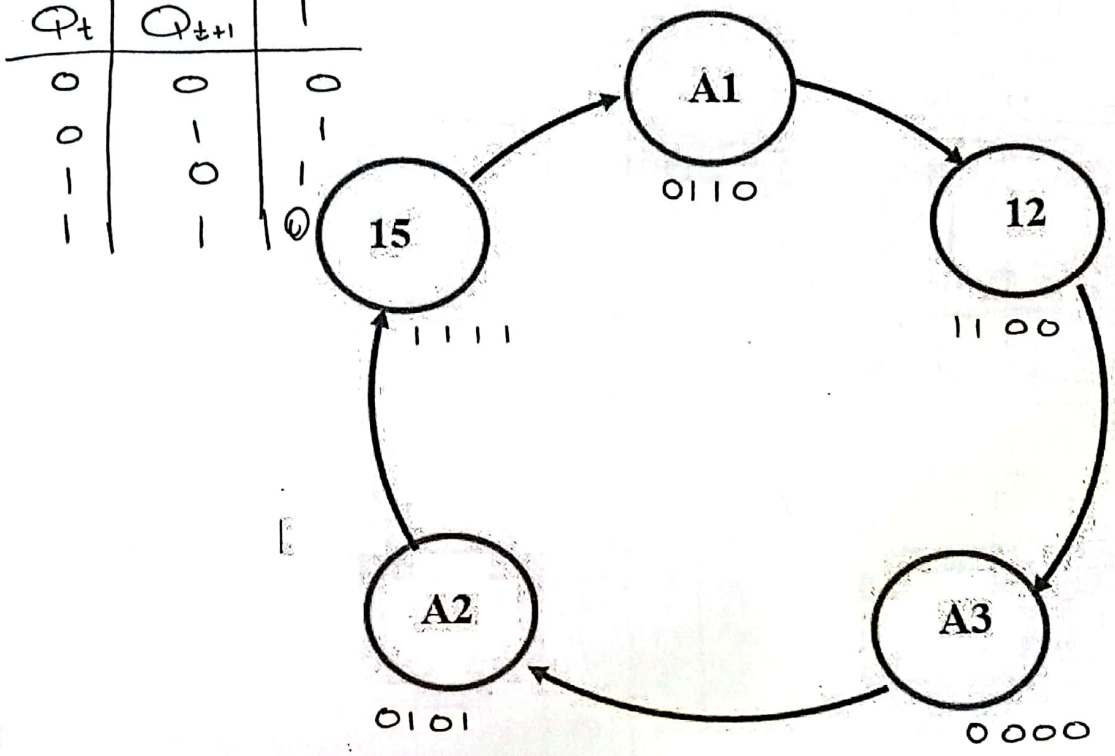
STATE TRANSITION DIAGRAM:



ID: ASSIGNMENT # 4 [FF-1005] Assigned Number:

4. Design circuit for given state diagram using **T Flip-Flop**?

Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



TABLE, SIMPLIFICATION & EXPRESSIONS

Current Stage Next Stage Inputs

	A_o	B_o	C_o	D_o	A	B	C	D	I_A	I_B	I_C	I_D
0	0	0	0	0	0	1	0	1	0	1	0	1
1	0	0	0	1	x	x	x	x	x	x	x	x
2	0	0	1	0	x	x	x	x	x	x	x	x
3	0	0	1	1	x	x	x	x	x	x	x	x
4	0	1	0	0	x	x	x	x	x	x	x	x
5	0	1	0	1	1	1	1	1	1	0	1	0
6	0	1	1	0	1	1	0	0	1	0	1	0
7	0	1	1	1	x	x	x	x	x	x	x	x
8	1	0	0	0	x	x	x	x	x	x	x	x
9	1	0	0	1	x	x	x	x	x	x	x	x
10	1	0	1	0	x	x	x	x	x	x	x	x
11	1	0	1	1	x	x	x	x	x	x	x	x
12	1	1	0	0	0	0	0	0	1	1	0	0
13	1	1	0	1	x	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x	x
15	1	1	1	1	0	1	1	0	1	0	0	1

I_A

AB \ CD	00	01	11	10
00	0	x	x	x
01	x	1	x	1
11	1	x	1	x
10	x	x	x	x

$I_A = B$

I_B

AB \ CD	00	01	11	10
00	1	x	x	x
01	x	0	x	0
11	1	x	0	x
10	x	x	1	x

$I_B = \bar{B} + B\bar{C}\bar{D}$

I_C

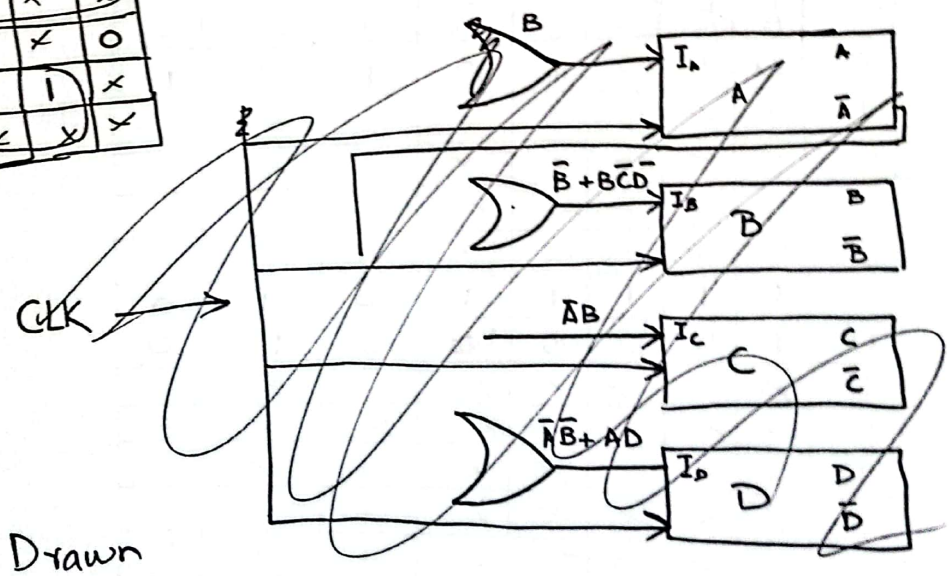
AB \ CD	00	01	11	10
00	0	x	x	x
01	x	1	x	1
11	0	x	0	x
10	x	x	x	x

$I_C = \bar{A}B$

I_D

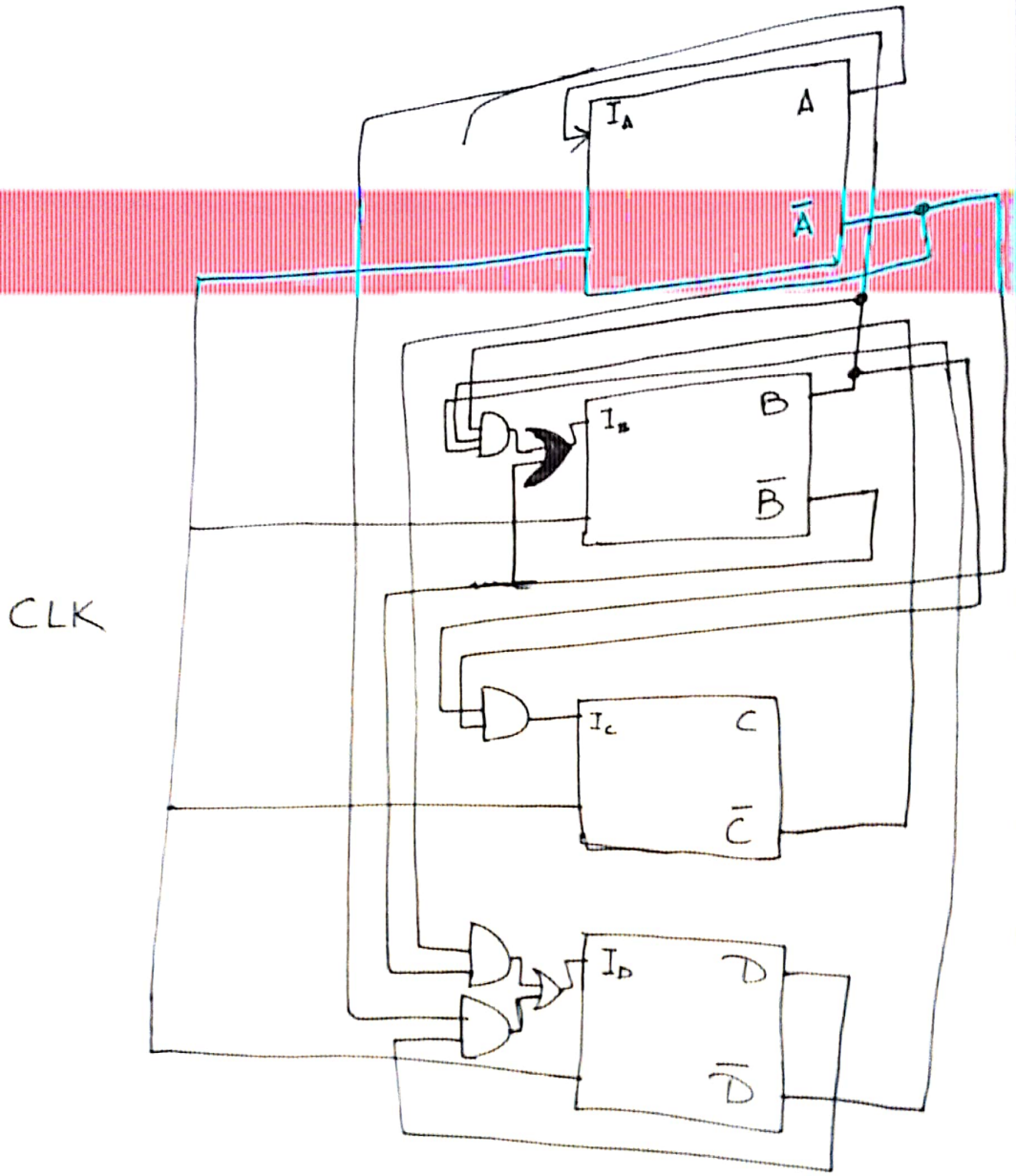
AB \ CD	00	01	11	10
00	1	x	x	x
01	x	0	x	0
11	0	x	1	x
10	x	x	x	x

$I_D = \bar{A}\bar{B} + AD$



Drawn on previous page

$I_A = B$, $I_B = \bar{B} + B\bar{C}\bar{D}$, $I_C = \bar{A}B$, $I_D = \bar{A}\bar{B} + AD$



ASSIGNMENT # 4 [EE-1005] Assigned Number:

raw a three bit UP-DOWN Counter. For each bit you will have to use a different flip flop (JK, T, D). Follow the steps roperly.

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D→T→JK

- State Diagram
- Next State Table
- State Reduction And Assignment
- Flip Flop Transition Table (FLIP FLOP Selection)
- Simplification
- Input/output Equations
- Implementations of Equation(Logic Diagram)

To decide which flip flop to use for your counter is based on your assigned number. Assume that JK<T<D. This means JK is the smallest, T flip flop is middle one and D flip flop is biggest one. Now based on the first 3 digits of your assigned number you will decide the pattern. For example, the id assigned number is 9486, then pick the first three digits like 948. Since the first digit is the biggest so D flip flop should be used first. 4 is the smallest, so JK should be used in the middle and T flip flop should be used in the end.

Excitation Tables

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Tables

J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$\overline{Q_t}$

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D	Q_{t+1}	$\overline{Q_{t+1}}$
0	0	1
1	1	0

Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T	Q_{t+1}
0	Q_t
1	$\overline{Q_t}$

ASSIGNMENT # 4 [EE-1005] **Assigned Number:**

A sequential circuit shown in the given figure has three D flip-flops Do, D_1 and D_2, two inputs X and Y, and outputs Z_1 and Z_2.

- ✔ Derive the STATE EQUATIONS
- ✔ Tabulate the STATE TABLE.
- ✔ Draw the **STATE DIAGRAM** of the circuit