Comparison of Vivado IP Integrator and Quartus Platform Designer

Background

When designing embedded systems on FPGAs, engineers often use graphical tools provided by FPGA vendors to build custom hardware platforms. These tools allow developers to connect processors, memory, and peripheral IP blocks into a coherent system-on-chip (SoC) architecture. Two commonly used tools for this purpose are **Vivado IP Integrator** (by AMD/Xilinx) and **Platform Designer** (by Intel, formerly Altera).

Vivado IP Integrator is a part of the Vivado Design Suite and is primarily used for designing systems with **MicroBlaze processors** or **Zynq SoCs**. It is based on the **AXI bus architecture**, which is a part of the ARM AMBA standard. Platform Designer, on the other hand, is integrated into the Quartus Prime software and is used for building systems with **Nios II processors**, based on Intel's **Avalon bus architecture**.

Although both tools serve a similar purpose, their interfaces, workflows, and technical foundations differ significantly. The comparison below outlines the key differences between the two tools, focusing on user interface, system integration, and design flow.

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1. Overview – Purpose and Function

Aspect	Vivado IP Integrator	Quartus Platform Designer
Purpose	System design using MicroBlaze or Zynq, AXI bus, IP integration	System design using Nios II, Avalon bus, IP integration
Bus System	AXI4, AXI4-Lite, AXI4-Stream	Avalon-MM, Avalon-ST
Processor Support	MicroBlaze (softcore), Zynq (ARM Cortex-A)	Nios II (softcore only)

2. User Interface

Aspect	Vivado	Platform Designer
GUI Layout	Modern and visual, with a canvas-based drag-and-drop interface	Classic, tabular interface integrated into Quartus
IP Connectivity	Visual block diagram with graphical connections	Component list with interface columns and manual/automatic connections
Navigation	Intuitive panning, zooming, and hierarchical block management	Simple tabs and lists, less visual flexibility
Integration in Toolchain	Embedded in Vivado as IP Integrator	Launched as a sub-tool inside Quartus Prime

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3. IP Integration and Configuration

Aspect	Vivado	Platform Designer
IP Configuration	Configure by clicking on a block in the diagram; opens a separate configuration dialog	Configure by selecting a component in the list; settings appear in a configuration pane
Auto-Connection	Yes, via “Run Connection Automation” to connect clocks, resets, and buses	Yes, via “Auto-Assign” to match master/slave interfaces
Custom IP Support	Supported through the IP Packager tool with GUI support	Supported using the Component Editor; process is more manual

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4. HDL Generation and Export

Aspect	Vivado	Platform Designer
HDL Output	Generates wrapper files and system HDL (VHDL/Verilog) from the block design	Generates HDL files and a TCL script for instantiation
Top-Level Integration	"Generate HDL Wrapper" allows easy inclusion in the top module	The Platform Designer system is instantiated manually or via auto-generated wrapper
Software Integration	Compatible with Vitis for software development targeting MicroBlaze or Zynq	Works with Nios II Software Build Tools (SBT) or Eclipse-based IDE

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5. User Experience

Aspect	Vivado	Platform Designer
Learning Curve	Moderate; visual interface helps beginners but system complexity may require time	Easier for small projects; more familiar to users with basic HDL knowledge
Interface Responsiveness	Fast and responsive (modern UI technologies)	Slightly slower, especially on large systems (older UI framework)
Documentation and Support	Extensive online documentation, tutorials, and community support	Good documentation, but some resources may be outdated

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Summary

Tool	Strengths	Limitations
Vivado IP Integrator	Modern, visual design flow; powerful automation; strong support for AXI and Zynq	Higher complexity; steeper learning curve for advanced configurations
Quartus Platform Designer	Simpler interface; fast for small/medium systems; well-suited for Nios II	Less visual feedback; Avalon bus is not as widely supported outside Intel tools