

Internal and External RAM in Vivado IP Integrator with MicroBlaze V

1. Background

MicroBlaze V is a configurable 32-bit RISC-V processor from AMD/Xilinx used in FPGA-based systems. In Vivado, MicroBlaze V can be integrated into a system using **IP Integrator**, a graphical tool that allows you to connect different IP blocks such as the processor, memory, buses, and I/O devices.

An important design decision when building an embedded system is the choice and placement of memory – whether to use **internal (on-chip)** or **external (off-chip)** RAM.

2. Internal RAM

2.1 What is Internal RAM?

Internal RAM (also known as Block RAM or BRAM) consists of memory blocks located inside the FPGA fabric. It is commonly used as:

- Instruction memory
- Data memory
- Cache

2.2 IP in Vivado

In IP Integrator, the "Block Memory Generator" IP is used to create internal RAM. It is connected to MicroBlaze V through an AXI BRAM Controller.

2.3 Advantages of Internal RAM

- **Fast:** Very low access time
- **Low latency:** Ideal for real-time applications
- **Easy to configure:** Directly generated and connected inside Vivado

2.4 Disadvantages

- **Limited size:** Capacity depends on the specific FPGA model
 - **Consumes logic resources:** Uses up block RAMs that could be used for other logic functions
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3. External RAM

3.1 What is External RAM?

External RAM refers to memory located **outside the FPGA**, such as DDR3 or DDR4 SDRAM. It is commonly used when more memory is needed than what BRAM can offer.

3.2 IP in Vivado

To use external RAM, the "**DDR4 SDRAM Controller**" IP (via **MIG – Memory Interface Generator**) is used. It connects to MicroBlaze via an **AXI Interconnect**.

3.3 Advantages of External RAM

- **Larger capacity:** From hundreds of megabytes to gigabytes
- **No consumption of FPGA resources:** Frees up logic and BRAM inside the FPGA

3.4 Disadvantages

- **Slower access** compared to BRAM (due to bus latency)
 - **Requires proper I/O pin configuration, layout, and timing constraints**
 - **More complex system integration**
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4. Practical Use in IP Integrator

Example: Internal RAM for Program Code

Steps:

1. Add **MicroBlaze V** in IP Integrator
2. Add the following IPs:
 - **Block Memory Generator** (e.g., 64 KB)
 - **AXI BRAM Controller**
 - **AXI Interconnect**
3. Connect the BRAM to MicroBlaze via the controller and interconnect

Example: External RAM using DDR4

Steps:

1. Add the **DDR4 SDRAM Controller (MIG)**
2. Configure it according to your board (e.g., Arty S7 uses DDR3)
3. Add an **AXI Interconnect** and connect it to MicroBlaze
4. Assign address ranges correctly in the **Address Editor**

5. Address Space and Memory Mapping

MicroBlaze uses a **32-bit address space**. In Vivado's **Address Editor**, you must define where each memory segment is mapped:

- 0x00000000 – 0x0000FFFF → Internal RAM (BRAM)
- 0x80000000 – 0xFFFFFFFF → External RAM (e.g., DDR)

In **Vitis**, you can also use the **linker script** to specify where program code and data segments should be placed in memory.

6. Recommendations

- For **simple or small systems** (e.g., lab work or test code): use **only internal BRAM**
 - For **complex systems with larger memory demands**: combine **internal and external RAM**
 - For **fast boot and startup**: use BRAM for the bootloader/instructions and stack/heap in DDR
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7. Summary: Comparison

Feature	Internal RAM (BRAM)	External RAM (DDR)
Access Speed	Very high	Low to medium
Size	Limited (KB)	Large (MB–GB)
Design Complexity	Simple	High
FPGA Resource Usage	Yes	No
Typical Usage	Boot, stack, instructions	Data buffers, large programs