AGSTU		**Technical report**	
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AGSTU

Time Verification

Comparison between Setup and Hold Timers from different designs

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Summary: In the current project, clock management will be improved to avoid timing problems that can occur when clock splitting via internal rockers. Clock splitting can lead to latency and race conditions between signals, affecting functionality. To solve this, three new projects were created based on the previous design.

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SDC files with comments and fastest frequency

Project 1

In project 1, the system clock of 50 MHz is divided down to 25 MHz through a clock division process in VHDL code. In the SDC file, the shared clock is imported using the command : `create_generated_clock.`

Project 2

- Synchronizes each frame (frame).
- Consists of the same four parts as the horizontal synchronization but relative to full frames.

Project 3

Time graphs in relation to horizontal and vertical counters (x_counter and y_counter):

1. **VGA_HS (Horizontal Sync)**
    - **Display Area** (x_counter: 0-639): RGB data is sent to draw pixels.
    - **Front porch** (x_counter: 640–655): No image data, a short pause.
    - **Sync heart rate** (x_counter: 656-751): VGA_HS set to **low** ('0').
    - **Rear porch** (x_counter: 752–799): No image data, a pause before the next line.
2. **VGA_VS (Vertical sync)**
    - **Display Area** (y_counter: 0-479): All rows in the frame are displayed.
    - **Front porch** (y_counter: 480–489): No image data, a pause.
    - **Sync heart rate** (y_counter: 490-491): VGA_VS set to **low** ('0').
    - **Rear porch** (y_counter: 492-524): No image data until the next frame.

Test log

- **Counter values**: Simulate up to the full range of both x_counter and y_counter.
- **Analysis tools**: Use ModelSim to observe **VGA_HS** and **VGA_VS** in relation to the values of the counters in the heart rate chart. See the next table.

Table 2. Test case for a test protocol being tested in Modilsim

Modelsim

ModelSim was used to simulate the VGA controller. During the simulation, the counters were analyzed **x_counter** and **y_counter** to ensure that they count correctly and reset according to VGA timing. The VGA_HS and **VGA_VS synchronization signals** were checked to confirm that they comply with the specified specifications. The RGB signals were tested by activating the respective buttons and observing the waveforms of the simulation.

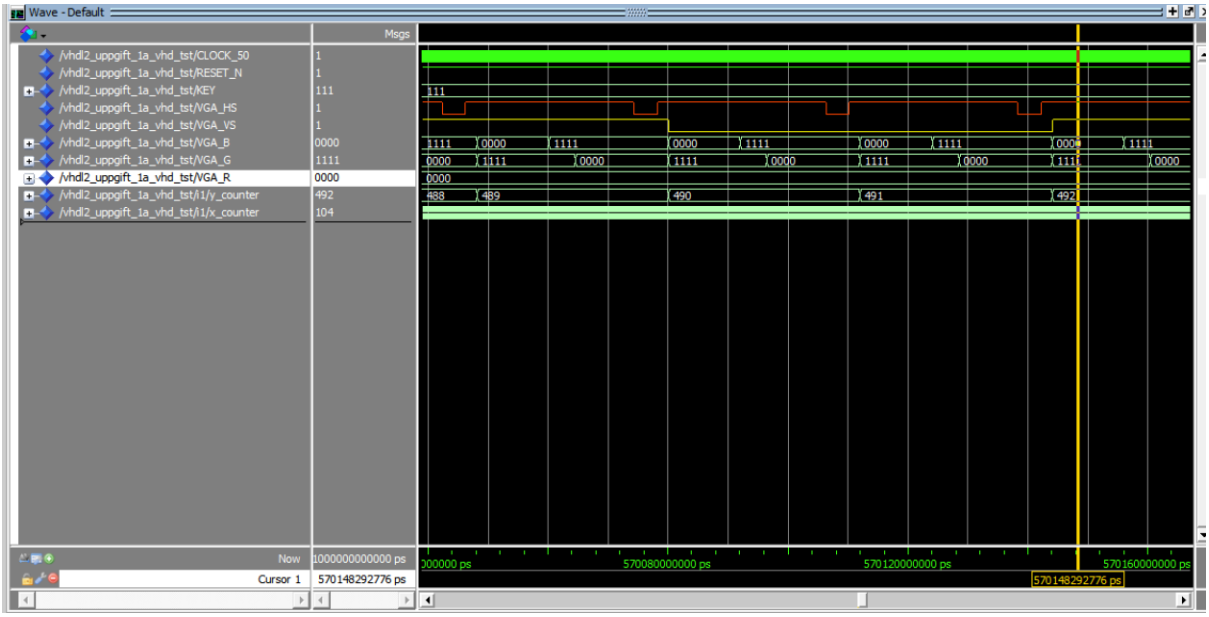

Figure 1. The plus chart shows HS and VS

SignalTap

SignalTap was used to analyze and verify the VGA controller directly on the FPGA board. The x_counter and y_counter counters were reviewed to ensure accurate counting and resetting according to VGA timing in the actual hardware. The synchronization signals VGA_HS and VGA_VS were monitored to verify that they are working according to specifications. The RGB signals were tested by activating the buttons on the board and analyzing the collected waveforms in SignalTap to ensure that they match the expected behavior. See the next figure.

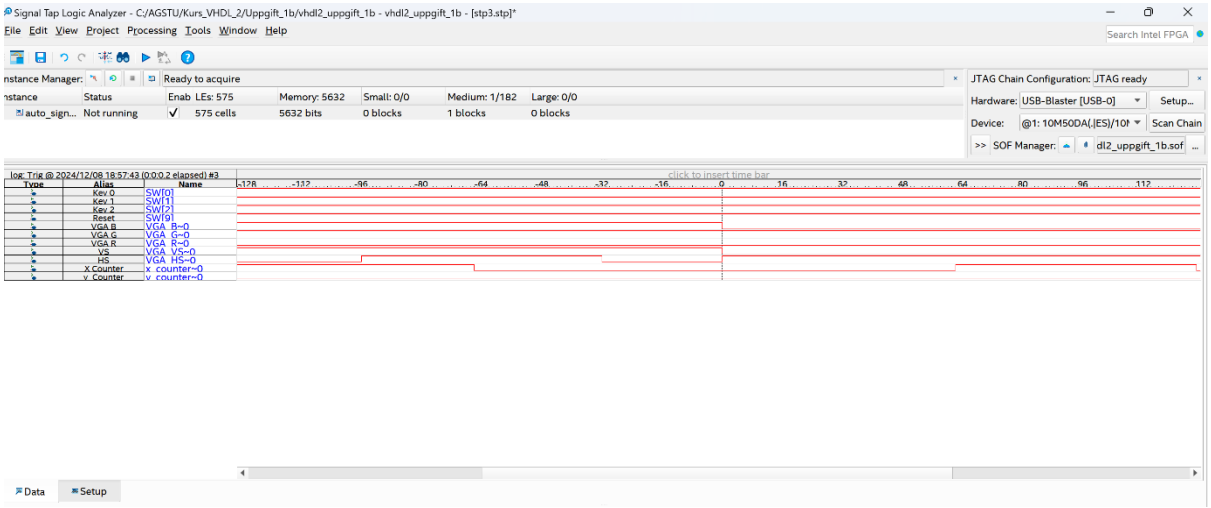

Figure 2. Plus chart from SignalTap