VLSI Design and Automation Project

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Basic Modules Comparison

Metric	Module	Synthesis Area	Synthesis Delay	Synthesis Utilization	Sy
Ripple Carry Adder	\ripple_carry_adder	2452.352000	2.55227	0.0105461	0.0001
Carry Select Adder	\carry_select_adder	2738.876800	2.503967	0.0117783	0.0001
Carry Bypass Adder	\carry_bypass_adder	2289.696000	2.458569	0.00984665	0.0001
Carry Lookahead Adder	\carry_lookahead_adder	1535.222400	2.424406	0.0066021	6.2243
Booth Multiplier	\booth_multiplier	157193.260800	3.038755	0.675997	0.0363
Sequential Multiplier	\sequential_multiplier	23951.721600	2.223281	0.103002	0.0013
Tree Multiplier	\tree_multiplier	109565.081600	2.97044	0.471176	0.0242
Verilog Multiplier	\verilog_multiplier	100475.113600	3.052082	0.432085	0.0131

Notes:

- **Clock Period**: Fixed at **20** for all modules.

Main RTL Comparison

Metric	Module	Synthesis Area	Synthesis Delay	Synthesis Utilization	Synth
Floating Point ALU	\floating_point_alu	54309.587200	12.419388	0.233554	0.00743