Zewail City of Science and Technology C++ (NANENG 503)

Fall 2020

Final Project

Delivery:

Each group member must deliver a code to perform floorplanning on a circuit given its netlist and possible dimensions for each circuit element. The output is the floorplan displayed graphically, its aspect ratio and percentage of wasted area inside of the minimum bounding box. Any of the three algorithms mentioned in the book could be used.

Component	**NOT gate**	**AND gate**	**OR gate**	**XOR gate**	**Flipflop**	**NAND gate**	**NOR gate**	**XNOR gate**
Dimensions	2*1	(n+1)* (n+1)	(n+1)* (n+1)	2n * (n+2)	8 * 1	n*n	n*n	2n*n

Where n is the number of inputs for that specific gate.

- Each gate can be flipped 90 degrees (i.e: lengths and widths are interchangeable.)
- Floorplan aspect ratio should be between 40% and 60%
- You could use any graphics library of your choice (SFML is recommended)

- The code must be general and accept any input.
- Code must be original
- Late submission is not accepted.

Netlist format is as follows:

```
Flipflop F1 (in D1, clk Clk1, out Q1);
Flipflop F2 (in D2, clk Clk1, out Q2);
Flipflop F3 (in D3, clk Clk1, out Q3);
And A1 (in Q1, in Q2, out S1);
Or O1 (in Q2, in Q3, out S2);
Xor X1 (in S1, in S2, out S3);
Inv I1 (in S2, out S4);
And A2 (in Q3, in S3, out S5);
Flipflop F4 (in S1, clk Clk1, out Q4);
Flipflop F5 (in S3, clk Clk1, out Q5);
Flipflop F6 (in S4, clk Clk1, out Q6);
Flipflop F7 (in S5, clk Clk1, out Q7);
Inv I2 (in Q4, out S6);
Xor X2 (in Q4, in Q5, out S7);
Or O2 (in Q6, in S7, out S8);
Inv I3 (in Q7, out S9);
And A3 (in S9, in S8, out S10);
Or O3 (in S6, in S7, out S11);
Flipflop F8 (in S11, clk Clk1, out Q8);
Flipflop F9 (in S8, clk Clk1, out Q9);
Flipflop F10 (in S10, clk Clk1, out Q10);
```