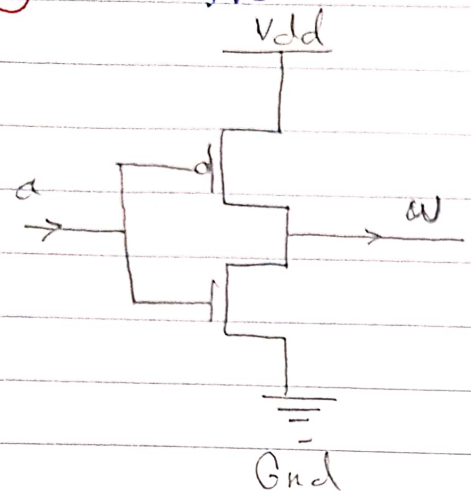
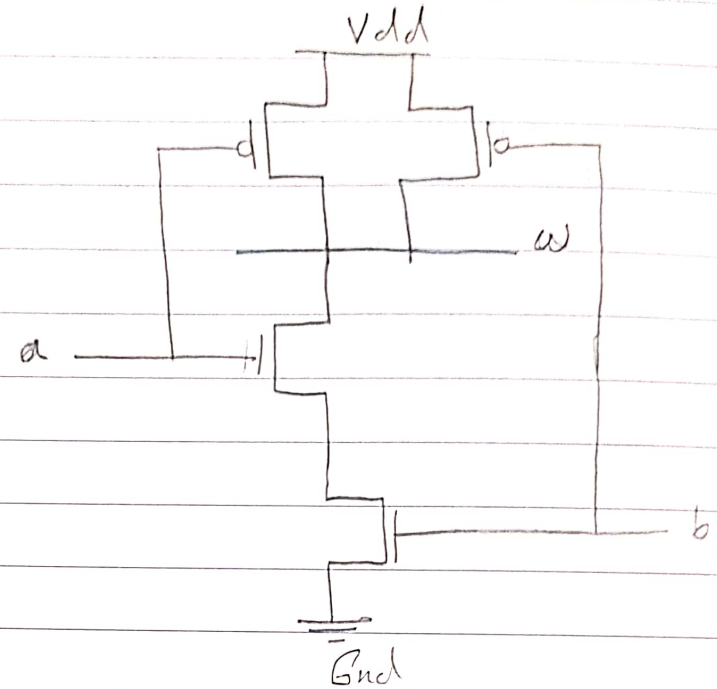
CA1 ۸۱۰۱۹۹۴۹۲ محمدامین پورزارع

Date: Subject:

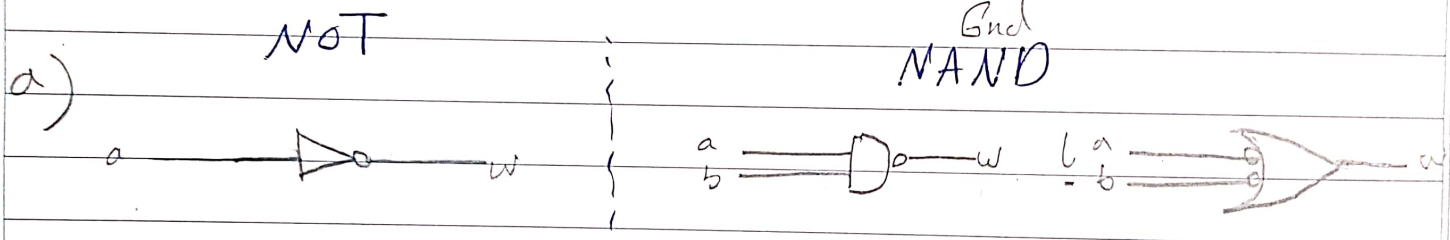
(1) NOT



NAND



a)



b) NOT

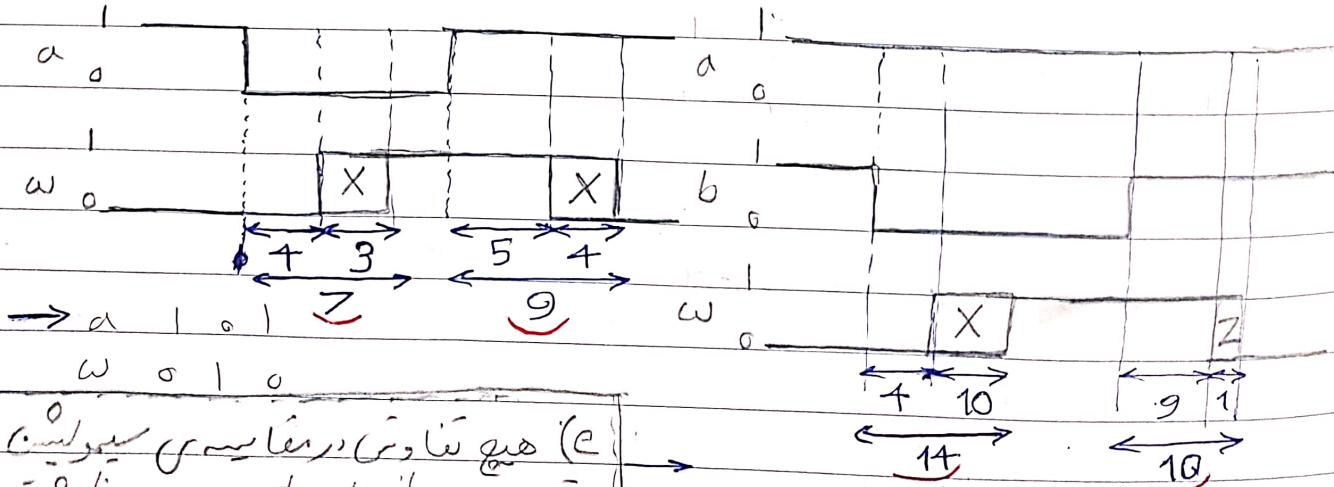
To 1: max(4, 7) = 7

To 0: max(5, 9) = 9

NAND

To 1: max(4, 2×7) = 14

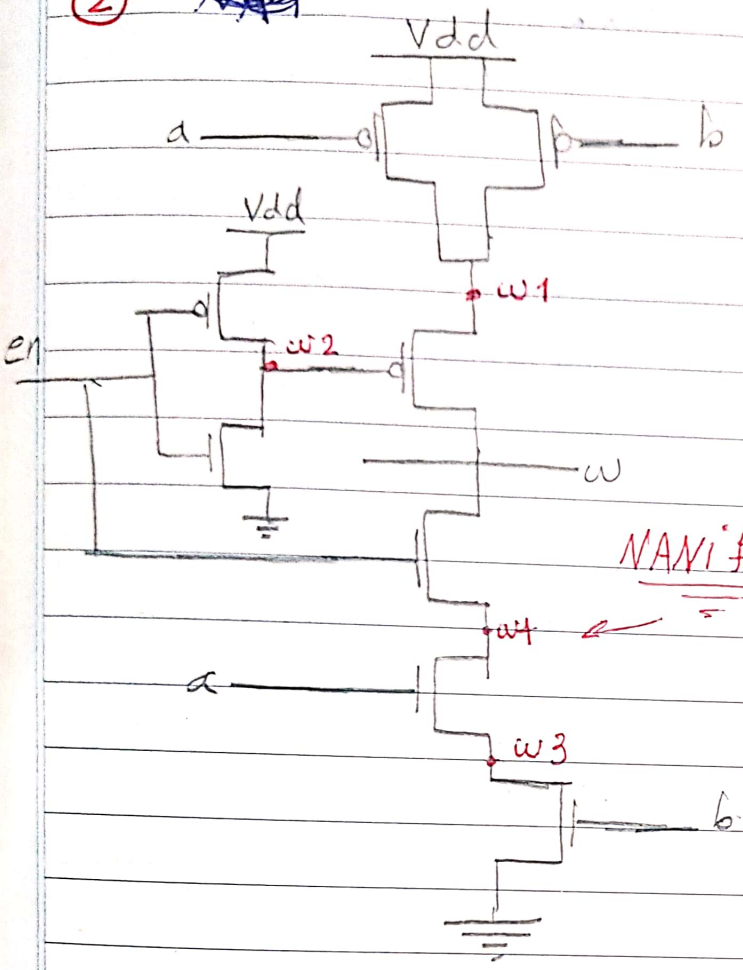
To 0: max(2×5, 9) = 10



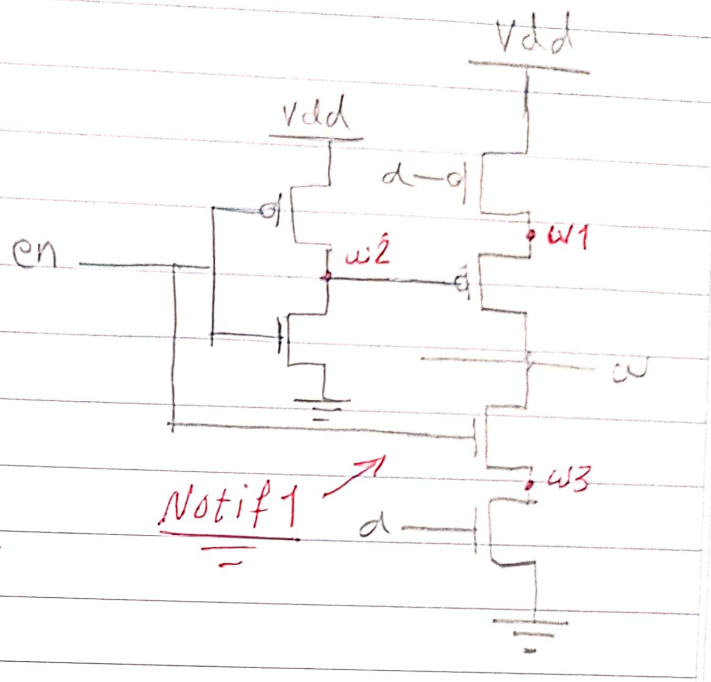
c) هیچ تفاوتی در مقایسه‌ی سیمولیشن دستی و System Verilog وجود نداشت و هر دو را از جمله زبان ها یکسان بودند.

Date: Subject:

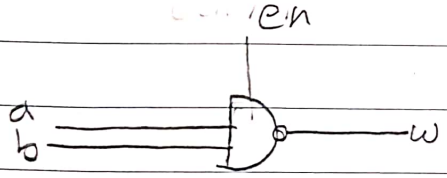
(2) ~~NOT~~ NAND Gate



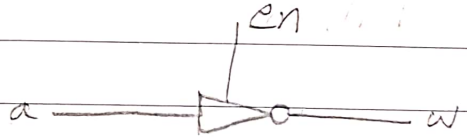
NOT Gate



a) NAND Gate



NOT Gate



b) To1: max(2×4, 3×7) = 21

To0: max(2×9, 3×3) = 18

To z: 9+7 = 16

Pmos Nmos a → 0 → 1 → 0

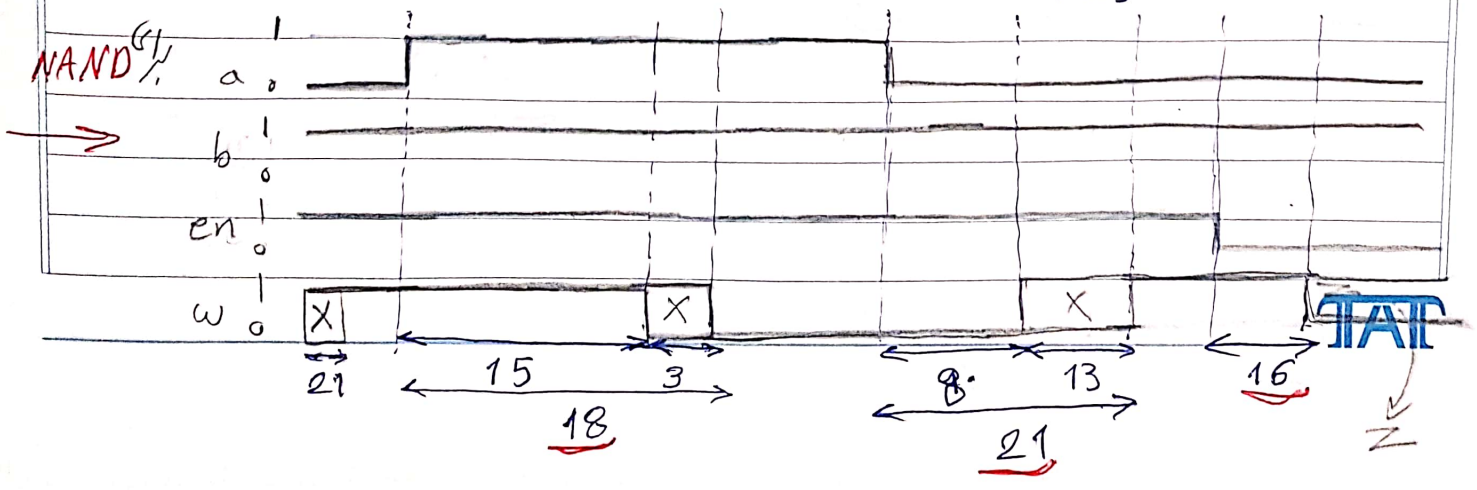
To1: max(2×4, 2×7) = 14

To0: max(2×9, 2×5) = 18

To z: 9+7 = 16

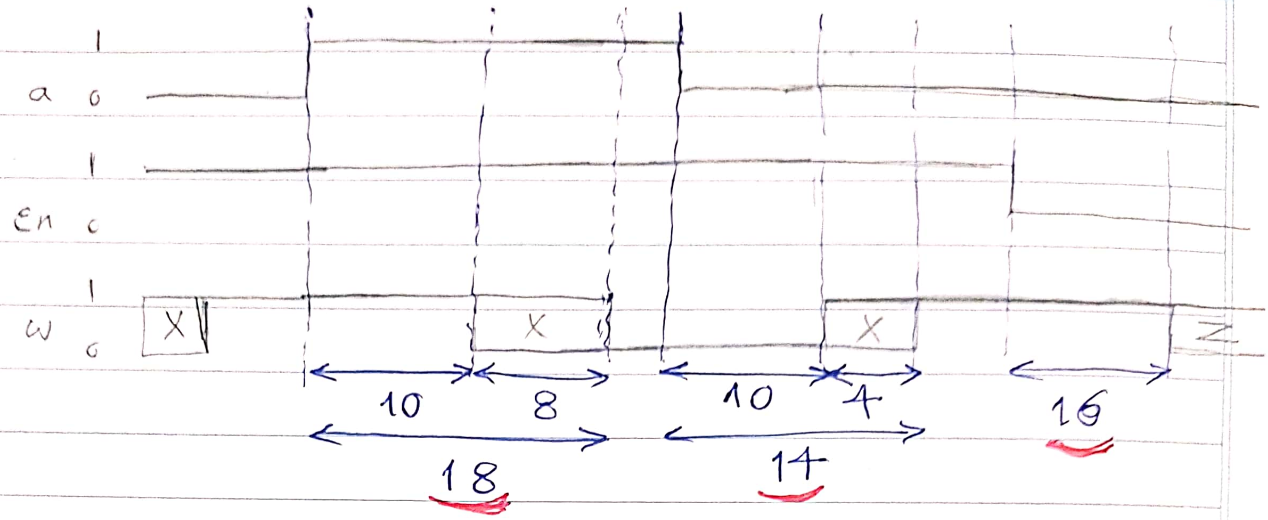
Pmos Nmos

NAND Gate



Date: Subject:

برای NOT

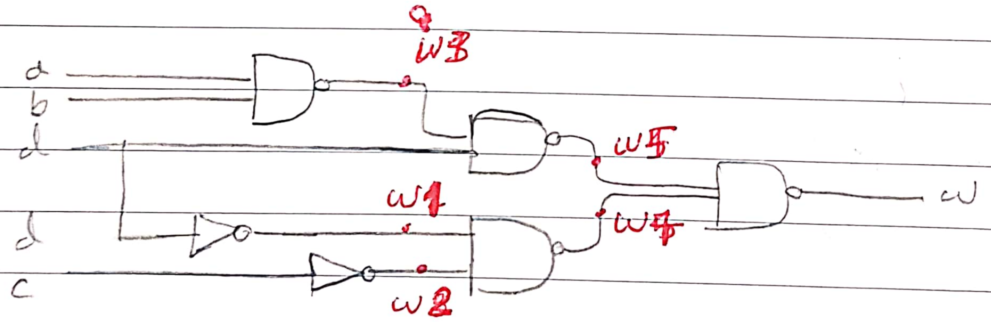


e) مانند سوال قبل هیچ تفاوتی دیده نمی شود.

③ $w = \bar{d} \cdot \bar{c} + d \cdot \overline{(a \cdot b)}$ $\xrightarrow[\text{NOT, NAND از}]{\text{برای استفاده}}$ $\overline{\overline{w}} = \overline{\overline{\bar{d} \cdot \bar{c} + d \cdot \overline{(a \cdot b)}}}$

$\longrightarrow w = \overline{\overline{(\bar{d} \cdot \bar{c})} \cdot \overline{d \cdot \overline{(a \cdot b)}}}$

a)



b) به دلیل اینکه Delay در NAND از NOT بیشتر است پس چون بالا سمت ما TNAND
پس مجموع قبل را استفاده می کنیم.

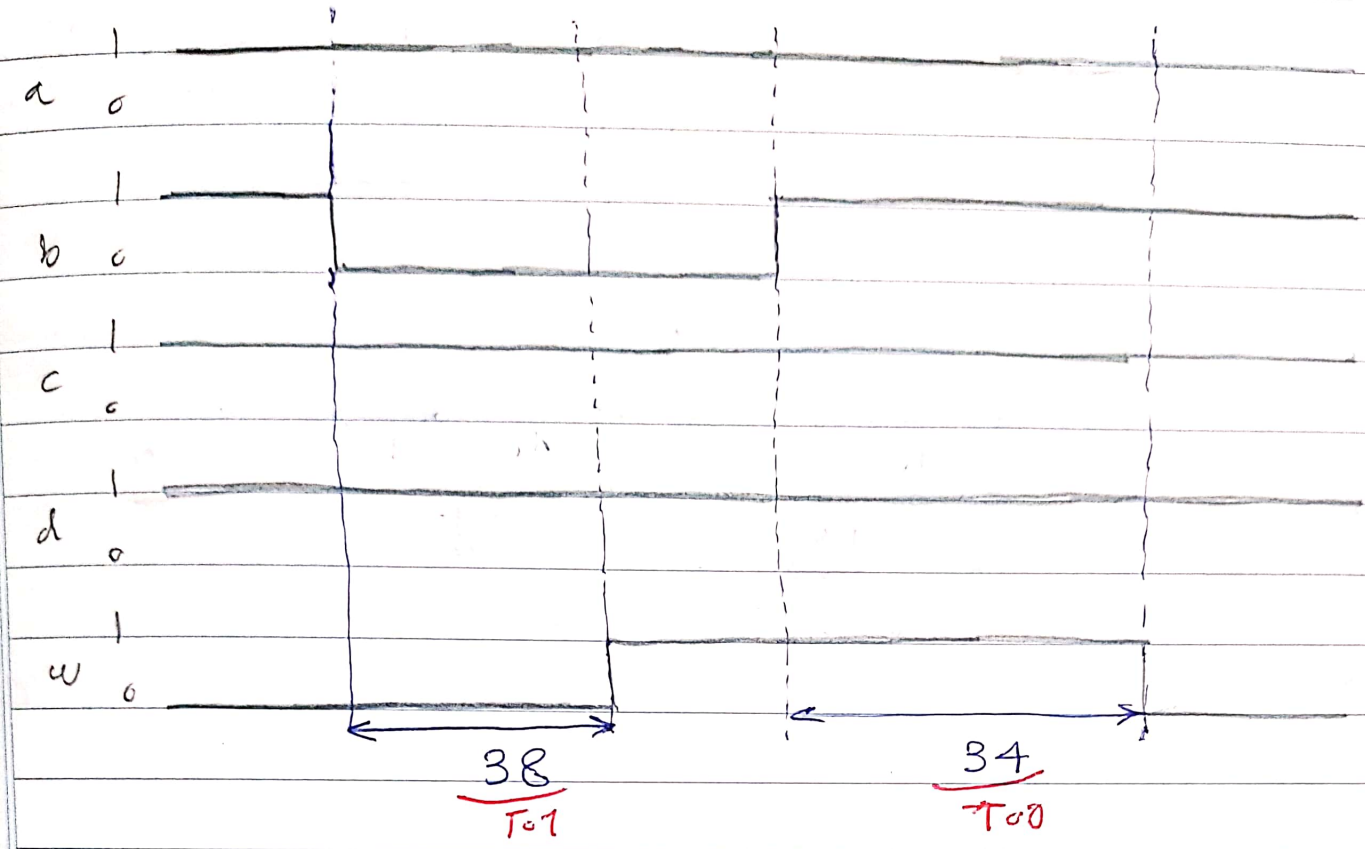
abcd → 1111 → 1011

To1: 14 + 14 + 10 = 38

abcd → 1011 → 1111

To0: 10 + 14 + 10 → 34

Date: Subject:



d) تغییر نمی‌کند.

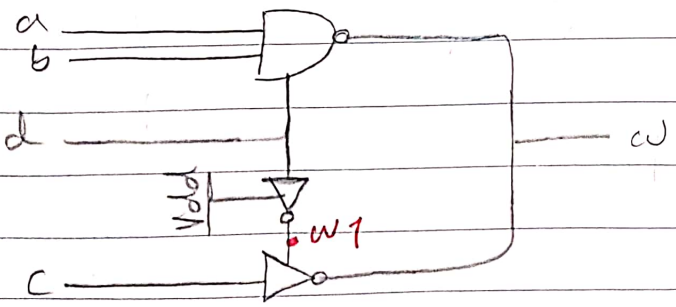
④ $w = \bar{d} \cdot \bar{c} + d \cdot (\overline{a \cdot b})$

Nandif1 # (21, 18, 16)

Notif1 # (14, 18, 16)

T=1 T=0 T=Z

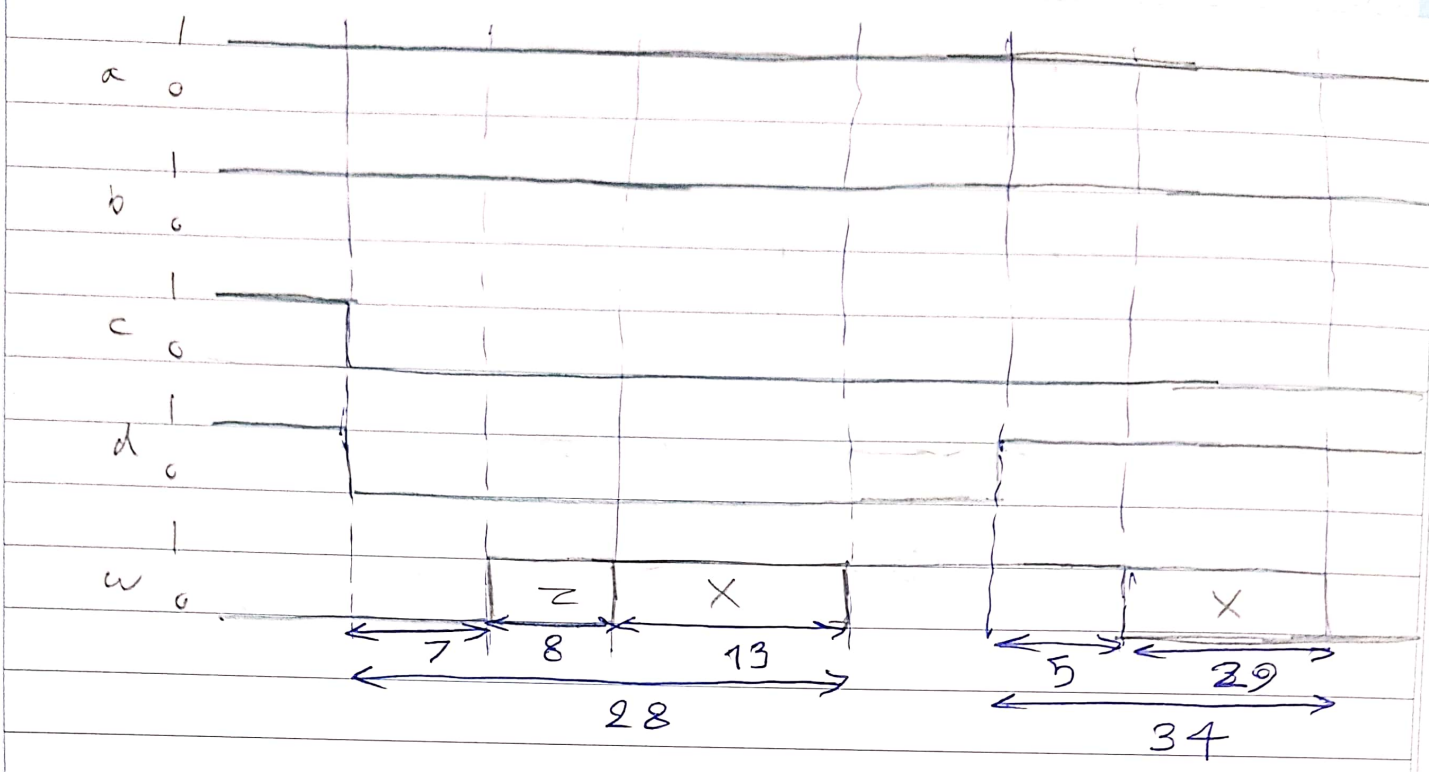
a)



b) T=1: abcd: 1101 → 1100 → 14 + 14 = 28

T=0: abcd: 1100 → 1101 → 16 + 18 = 34

Date: Subject:



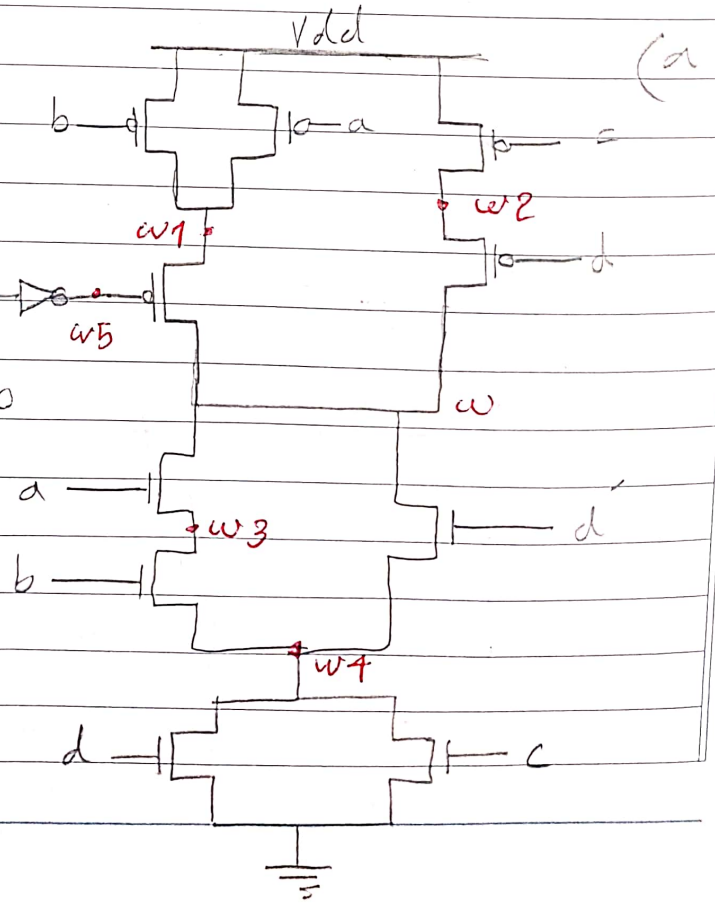
d) وقتی دستی حساب کردیم TO1 ، 28 بدست آمد اما وقتی در System Verilog تست کردیم TO1 ، 27 می‌شود.

a) $w = \bar{d} \cdot \bar{c} + d \cdot (\bar{a} + \bar{b})$

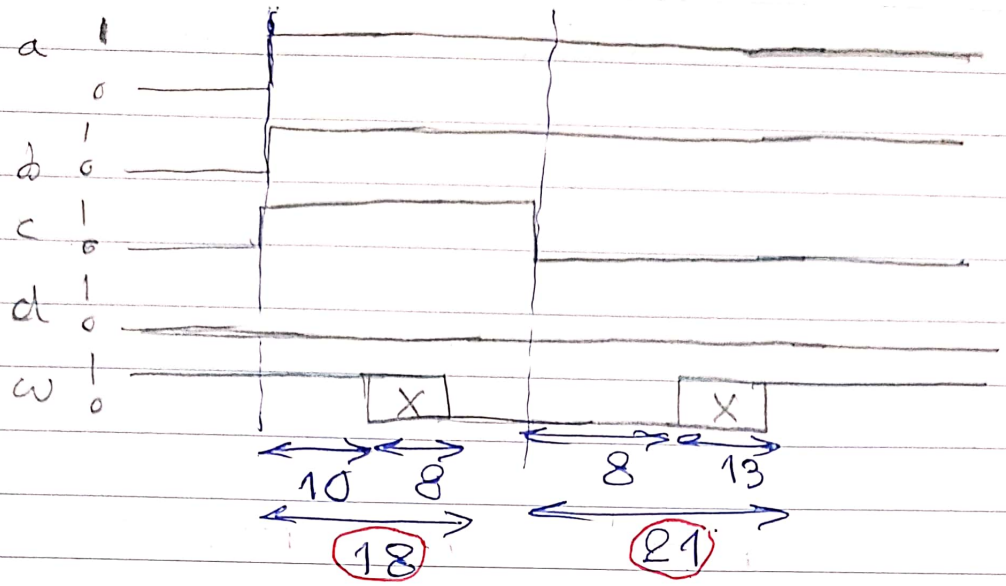
b) TO1: $\max(3\times7, 9+4) = 21$

TO0: $\max(3\times5, 9+9) = 18$

→ abcd : 0000 → 1110 → 1100



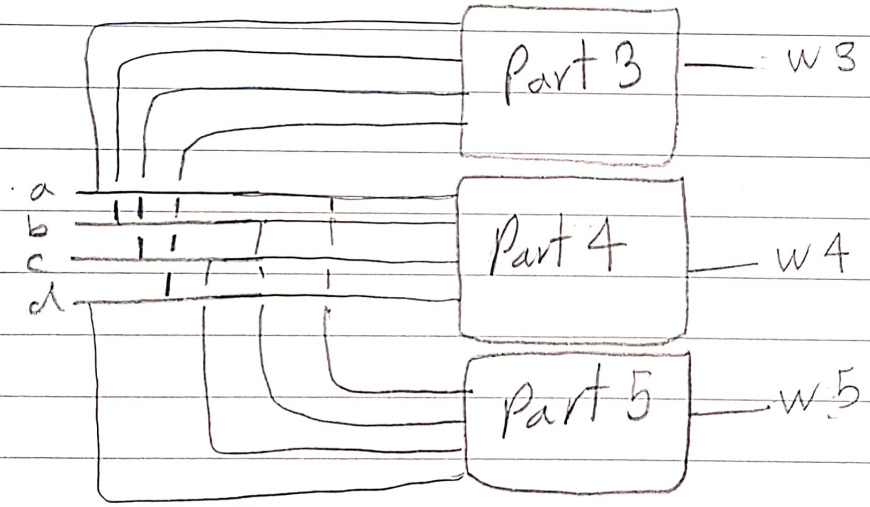
Date: Subject:



d) تفاوتی دیده نمیشود.

6

a)



	worst-case (timing)	Number of transistors
Part 3	(38, 34)	nand nand 2×2 + 4×4 = 20
Part 4	(28, 24)	nand if not if 1×8 + 2×6 = 20
Part 5	(21, 18)	Pmos/nmos not 2×5 + 1×2 = 12
	3 > 4 > 5 (Part)	3 = 4 > 5 (Part)

and

Power ∝ num transistor gate

3 > 4 > 5