FakeNovera and FakeCepheus: Open-Source Noise Models for Rigetti Quantum Processors with Application to Depth-Optimized Reservoir Computing

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Abstract—**Reproducible quantum computing research requires faithful software noise models, yet Rigetti Computing lacks the open-source "fake backend" ecosystem that IBM and IQM provide. We introduce FAKENOVERA and FAKECEPHEUS, the first open-source noise simulators for Rigetti's Novera 9-qubit and Cepheus-1 36-qubit processors. Both offer dual PyQuil/Qiskit implementations with calibrated noise parameters from published specifications. FAKENOVERA models the 3×3 square lattice with 12 edges, depolarizing errors, T_1/T_2 relaxation, and readout noise. FAKECEPHEUS extends this to four Novera chiplets in a 2×2 tiling (60 edges: 48 intra-chip, 12 inter-chip) with a heterogeneous noise model assigning distinct fidelities to intra-chip ($F_{2Q} = 99.5\%$) and inter-chip ($F_{2Q} = 99.0\%$) gates. We validate both simulators through quantum reservoir computing (QRC) depth optimization on the Lorenz-63 system. On FAKENOVERA, a systematic layer sweep identifies a steep performance transition near 70% cumulative fidelity, with optimal depth $d_{\mathrm{opt}} = 5$ layers ($R^2 = 0.538$, walk-forward $R^2 = 0.528 \pm 0.148$). On FAKECEPHEUS, the five-fold edge increase drives $d_{\mathrm{opt}} \approx 1$—a "curse of connectivity" showing depth optimization is topology-dependent. We derive the closed-form formula $d_{\mathrm{opt}} = \ln(F_{\mathrm{threshold}})/(n_{\mathrm{edges}} \times \ln(F_{2Q}))$ and prove scaling theorems that unify these results. The simulators are released as open-source software.**

Index Terms—**Quantum computing simulators, noise modeling, quantum reservoir computing, circuit depth optimization, NISQ devices, Rigetti, multi-chip architectures**

I. INTRODUCTION

Reproducible quantum computing research depends on faithful software models of physical hardware. IBM recognized this early: its Qiskit framework ships dozens of "fake backends" (`FakeToronto`, `FakeNairobi`, `FakeSherbrooke`, and others) that replicate calibration data, connectivity maps, and noise characteristics of real processors [1]. IQM provides analogous tools for its superconducting platforms [2]. These fake backends allow algorithm designers to iterate without hardware queue times, benchmark noise-aware compilers, and produce results that track real-device behavior.

Rigetti Computing, despite operating a growing fleet of superconducting processors—from the 9-qubit Novera [3] to the 36-qubit Cepheus-1 [4] and the 84-qubit Ankaa-3 [5]—has no equivalent open-source fake-backend ecosystem. Researchers targeting Rigetti hardware must either secure device time

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through Amazon Braket [6] or Microsoft Azure Quantum [7], or build ad hoc noise models with no community-standard reference. This gap slows algorithm development and limits reproducibility.

We fill this gap with two open-source simulators:

- **FAKENOVERA:** A noise model for the Novera 9-qubit tunable-coupler processor, providing a 3×3 square lattice with 12 edges, two calibration profiles, and dual PyQuil/Qiskit implementations.
- **FAKECEPHEUS:** A noise model for the Cepheus-1 36-qubit multi-chip module (MCM), tiling four Novera chiplets in a 2×2 arrangement with 60 edges and heterogeneous intra-/inter-chip noise fidelities.

To demonstrate the value of these tools, we apply them to a timely problem: optimal circuit depth for quantum reservoir computing (QRC). QRC exploits noisy quantum dynamics as a computational substrate for time-series prediction [8]–[10], but a fundamental design question remains: *how deep should the quantum circuit be?* Deeper circuits generate richer feature spaces through entanglement, yet accumulated two-qubit gate errors eventually destroy quantum correlations. Finding the optimal depth requires a noise model that faithfully captures hardware behavior—precisely what our simulators provide.

Using FAKENOVERA, we perform the first systematic layer sweep on a 9-qubit square lattice, identifying a steep performance transition near 70% cumulative fidelity with optimal depth $d_{\mathrm{opt}} = 5$ layers. Using FAKECEPHEUS, we predict $d_{\mathrm{opt}} \approx 1$ layer for the 36-qubit system—a five-fold reduction driven entirely by the higher edge count. This "curse of connectivity" is a powerful result: larger, more connected processors are not necessarily better for QRC, because each additional edge per layer accelerates fidelity decay. We unify these observations in the closed-form formula:

$$d_{\mathrm{opt}} = \frac{\ln(F_{\mathrm{threshold}})}{n_{\mathrm{edges}} \times \ln(F_{2Q})} \quad (1)$$

Our contributions are:

1) **First open-source Rigetti fake backends:** FAKENOVERA and FAKECEPHEUS with dual PyQuil/Qiskit implementations and calibrated noise models.
2) **Heterogeneous multi-chip noise model:** FAKECEPHEUS distinguishes intra-chip ($F_{2Q} = 99.5\%$) from inter-chip ($F_{2Q} = 99.0\%$) gate fidelities, a feature absent from existing fake-backend frameworks.

3) **Performance transition at 70% fidelity:** Identification of a steep quantum-to-classical crossover governing QRC prediction quality on square lattice topologies.
4) **Closed-form optimal depth formula:** $d_{\text{opt}} = \ln(F_{\text{threshold}})/(n_{\text{edges}} \times \ln(F_{2Q}))$, validated on 9Q and predicted for 36Q.
5) **Curse of connectivity:** Demonstration that $d_{\text{opt}} \to 0$ as n_{edges} grows, establishing a fundamental tension between processor connectivity and QRC circuit depth.
6) **Honest evaluation:** Walk-forward cross-validation on the chaotic Lorenz-63 system with unbiased performance estimates and statistical significance testing.

The remainder of this paper is organized as follows. Section II reviews related work on fake backends, QRC, and NISQ noise. Section III details the FAKENOVERA simulator. Section IV presents FAKECEPHEUS and its heterogeneous noise model. Section V formalizes the optimal depth theory. Section VI applies both simulators to QRC depth optimization. Section VII discusses implications. Section VIII concludes with future directions.

II. BACKGROUND AND RELATED WORK

A. Fake Backend Ecosystems

IBM's Qiskit framework pioneered the fake-backend pattern: a software class that exposes the same interface as a real quantum backend but executes locally through a noise simulator [1]. Each fake backend bundles a connectivity graph, gate set, calibration data (gate fidelities, coherence times, readout errors), and a noise model that AerSimulator uses for density-matrix or trajectory simulation. As of Qiskit 1.0, IBM provides fake backends for over 30 processors spanning 5–156 qubits, including `FakeToronto` (27Q), `FakeNairobi` (7Q), `FakeSherbrooke` (127Q), and `FakeKyiv` (127Q). These tools have become indispensable for algorithm development, compiler benchmarking, and noise-aware circuit optimization [11].

IQM follows a similar approach for its European superconducting hardware, providing noise-model constructors tied to their star-topology processors [2].

Rigetti, by contrast, offers no analogous open-source tooling. Researchers can access Rigetti hardware through Amazon Braket [6] and Azure Quantum [7], but these cloud services provide live device access, not local noise simulators. The Rigetti-native path (PyQuil + QVM + quilc) supports noisy simulation via manually specified Kraus operators, but no pre-calibrated noise models are published. This forces each research group to build bespoke noise models—an error-prone, non-reproducible process. FAKENOVERA and FAKECEPHEUS address this gap directly.

B. Classical Reservoir Computing

Reservoir computing emerged in the early 2000s as a framework for training recurrent neural networks without backpropagation through time [12], [13]. The key insight is to separate dynamics generation (the *reservoir*, a fixed, randomly initialized recurrent network) from readout learning (a linear regression on reservoir states). This architecture exploits the *echo state property*: input signals create transient, high-dimensional activation patterns that can be linearly decoded to approximate target outputs.

The reservoir's role is computational: transforming time-series inputs into rich, nonlinear feature representations. Success requires *fading memory* (inputs influence states for finite duration) and the *separation property* (different inputs produce distinguishable trajectories). Classical reservoir computing has found applications in speech recognition, financial forecasting, and chaotic system prediction [12], [14]–[18]. However, feature space dimensionality scales polynomially with reservoir size, motivating exploration of quantum systems whose exponentially large Hilbert spaces promise richer representations.

C. Quantum Reservoir Computing

Quantum reservoir computing extends the reservoir paradigm to quantum systems, exploiting inherent quantum dynamics as the computational substrate [8], [19], [20]. The protocol follows three stages: (1) *Encoding*: classical values $x(t)$ are encoded via parameterized rotations; (2) *Quantum evolution*: the encoded state evolves through a fixed quantum circuit, creating entanglement; (3) *Measurement and readout*: computational-basis measurements yield classical features fed to a linear regressor.

Fujii and Nakajima [8] showed that disordered quantum circuits serve as effective reservoirs. Govia et al. [9] demonstrated single nonlinear oscillators exhibit reservoir capabilities. Martínez-Peña et al. [21] identified dynamical phase transitions (thermalization vs. many-body localization) governing QRC performance, showing optimal operation at phase boundaries. Domingo et al. [22] found that noise can benefit QRC under specific fidelity conditions ($> 96\%$ state fidelity for amplitude damping). Recent Rydberg atom [23], continuous-variable [24], and spatial multiplexing [25] implementations have expanded the platform landscape. Experimental demonstrations on superconducting qubits [26]–[28] validate theoretical predictions. Innocenti et al. [29] showed quantum extreme learning machines have information capacity bounded by the effective measurement, while Xiong et al. [30] identified four sources of exponential concentration that can render random quantum reservoir models unscalable.

A critical gap persists: *how should the quantum circuit be designed?* Circuit depth remains a free parameter chosen ad hoc across studies, yet depth directly controls the expressivity-noise tradeoff.

D. Noise in NISQ Devices

Near-term quantum processors are characterized by limited qubit counts, short coherence times ($T_1, T_2 \sim 10$–100 μs), and imperfect gate fidelities [31], [32]. Two-qubit gates are particularly error-prone: typical fidelities $F_{2Q} \sim 99$–99.5% on superconducting platforms mean each CZ or CNOT gate introduces 0.5–1% error. For a circuit with d layers and n_{edges} entangling gates per layer, cumulative fidelity decays as:

$$F_{\text{cum}}(d) \approx F_{2Q}^{d \times n_{\text{edges}}} \tag{2}$$

This exponential decay is the central NISQ challenge. Variational quantum eigensolvers [33], QAOA, and QRC all face the same constraint: deeper circuits improve expressivity but suffer noise-induced performance collapse [34], [35]. Error mitigation can partially address this [36]–[38], though at additional overhead.

E. Qubit Topology: Heavy-Hexagon vs. Square Lattice

IBM's architectural shift from heavy-hexagon to square lattice topologies (Nighthawk) [39] motivates focus on square connectivity. Heavy-hexagon graphs have degree-3 qubits arranged hexagonally, achieving $\sim$10–15% connectivity [40]. Square lattices arrange qubits in a 2D grid with degree-4 interior qubits, approaching 33% connectivity. Rigetti's Novera exemplifies this architecture: a 3×3 square lattice with 12 edges and 33.3% connectivity [3].

The topology-depth interaction is critical: square lattices permit shorter depths for equivalent entanglement spreading, but each layer involves more simultaneous two-qubit gates, accumulating errors faster. This makes depth optimization topology-dependent.

III. FAKENOVERA: NOVERA 9Q SIMULATOR

A. Processor Architecture

The Rigetti Novera QPU is a 9-qubit superconducting processor based on tunable transmon qubits arranged in a 3×3 square lattice [3]. The physical device comprises 21 elements: 9 data qubits (labeled 0–8) and 12 tunable coupler qubits (labeled 9–20), one per edge. Qubit connectivity forms a nearest-neighbor grid:

$$\begin{matrix} 0 & 1 & 2 \\ 3 & 4 & 5 \\ 6 & 7 & 8 \end{matrix}$$

with 12 edges: horizontal pairs $(0,1), (1,2), (3,4), (4,5), (6,7), (7,8)$ and vertical pairs $(0,3), (3,6), (1,4), (4,7), (2,5), (5,8)$. This yields 33.3% connectivity $(12/\binom{9}{2} = 12/36)$. Interior qubit 4 has degree 4; corner qubits have degree 2; edge qubits have degree 3.

Two-qubit entanglement is mediated by controlled-Z (CZ) gates implemented via parametric modulation of tunable couplers. This design suppresses always-on ZZ coupling and enables high-fidelity gates.

B. Specification Profiles

FAKENOVERA provides two calibration profiles drawn from distinct sources:

1) Official Rigetti profile (`NOVERA_SPECS_OFFICIAL`): Based on Rigetti's published product specifications [3]:

- $T_1 = T_2 = 27\,\mu s$
- $F_{1Q} = 99.9\%$ ($p_{error} = 0.1\%$)
- $F_{2Q} = 99.4\%$ ($p_{error} = 0.6\%$)
- Gate times: $t_{1Q} = 40\,ns$, $t_{CZ} = 200\,ns$

2) Zurich Instruments profile (`NOVERA_SPECS_ZURICH`): Based on independent

TABLE I: FakeNovera 9Q Specification Profiles

Parameter	Official	Zurich	Unit
Qubits	9	9	—
Topology	3×3 square lattice		—
Edges	12	12	—
Connectivity	33.3%	33.3%	—
T_1	27	45.9	μs
T_2	27	25.5	μs
F_{1Q}	99.9%	99.51%	—
F_{2Q} (CZ)	99.4%	99.4%	—
t_{1Q}	40	40	ns
t_{CZ}	200	200	ns
Readout error	1.0%	1.0%	—

benchmarks performed by Zurich Instruments on a Novera system [3]:

- $T_1 = 45.9\,\mu s$, $T_2 = 25.5\,\mu s$
- $F_{1Q} = 99.51\%$ ($p_{error} = 0.49\%$)
- $F_{2Q} = 99.4\%$ ($p_{error} = 0.6\%$)
- Gate times: $t_{1Q} = 40\,ns$, $t_{CZ} = 200\,ns$

The two profiles bracket realistic device performance: the Official profile represents best-case specifications, while the Zurich profile captures independently measured values that include calibration imperfections. Results in this paper use the Zurich profile unless stated otherwise.

C. Noise Model Implementation

The FAKENOVERA noise model comprises three channels applied to every gate:

1) Depolarizing noise: After each single-qubit gate, a single-qubit depolarizing channel is applied with error probability $p_{1Q} = 1 - F_{1Q}$. After each CZ gate, a two-qubit depolarizing channel is applied with $p_{2Q} = 1 - F_{2Q}$:

$$\mathcal{E}_{1Q}(\rho) = (1 - p_{1Q})\rho + \frac{p_{1Q}}{3} \sum_{P \in \{X,Y,Z\}} P\rho P \quad (3)$$

$$\mathcal{E}_{2Q}(\rho) = (1 - p_{2Q})\rho + \frac{p_{2Q}}{15} \sum_{P \in \mathcal{P}_2 \setminus \{I\}} P\rho P \quad (4)$$

where $\mathcal{P}_2$ is the set of 16 two-qubit Pauli operators.

2) Thermal relaxation: T_1 (amplitude damping) and T_2 (phase damping) channels are applied after each gate according to the gate duration. For gate time t_g:

$$p_{reset} = 1 - e^{-t_g/T_1} \quad (5)$$

$$p_{phase} = 1 - e^{-t_g/T_2} \quad (6)$$

3) Asymmetric readout noise: Measurement errors are modeled as classical bit-flip channels with $P(1|0) = P(0|1) = 1\%$. This approximation suffices for current Novera specifications; qubit-dependent asymmetric readout can be configured.

D. Dual Implementation

FAKENOVERA provides two equivalent simulation paths:

PyQuil path (`fakenovera.pyquil`): Generates Quil assembly with noise pragmas targeting Rigetti's QVM simulator and quilc compiler. This path is recommended for users

in the Rigetti ecosystem who need native Quil compilation, CZ-gate decomposition via quilc, and compatibility with the Rigetti stack. Requires Docker containers for QVM and quilc.

Qiskit path (`fakenovera.qiskit`): Constructs a `NoiseModel` object for Qiskit Aer's density matrix or stabilizer simulator. No external dependencies beyond Qiskit are required. This path is recommended for cross-platform research and integration with IBM tools.

Both paths share identical noise parameters and produce statistically equivalent results for circuits within the supported gate set (R_X, R_Y, R_Z, CZ, measurement).

IV. FAKECEPHEUS: CEPHEUS-1 36Q MULTI-CHIP SIMULATOR

A. Multi-Chip Architecture

Rigetti's Cepheus-1 processor, announced in August 2025 [4], represents a multi-chip module (MCM) architecture comprising four Novera-class chiplets tiled in a 2×2 arrangement. Each chiplet contains 9 qubits in a 3×3 square lattice, yielding 36 data qubits total. The chiplets are labeled NW (northwest), NE (northeast), SW (southwest), and SE (southeast), with qubit numbering:

$$
\begin{array}{ccc}
0 & 1 & 2 \\
3 & 4 & 5 \\
6 & 7 & 8
\end{array}
\quad
\begin{array}{ccc}
9 & 10 & 11 \\
12 & 13 & 14 \\
15 & 16 & 17
\end{array}
\quad
\begin{array}{ccc}
18 & 19 & 20 \\
21 & 22 & 23 \\
24 & 25 & 26
\end{array}
\quad
\begin{array}{ccc}
27 & 28 & 29 \\
30 & 31 & 32 \\
33 & 34 & 35
\end{array}
$$
$$
\underbrace{}_{\text{NW}} \quad \underbrace{}_{\text{NE}} \quad \underbrace{}_{\text{SW}} \quad \underbrace{}_{\text{SE}}
$$

B. Connectivity

The Cepheus-1 connectivity graph contains 60 edges partitioned into two classes:

Intra-chip edges (48 total): Each chiplet contributes 12 nearest-neighbor edges identical to Novera's 3×3 lattice. These connections use on-chip tunable couplers with high fidelity.

Inter-chip edges (12 total): Chiplet boundaries are bridged by intermodule couplers. In the 2×2 tiling, inter-chip connections link:

- NW–NE boundary: $(2,9), (5,12), (8,15)$ (3 horizontal edges)
- NW–SW boundary: $(6,18), (7,19), (8,20)$ (3 vertical edges)
- NE–SE boundary: $(15,27), (16,28), (17,29)$ (3 vertical edges)
- SW–SE boundary: $(20,27), (23,30), (26,33)$ (3 horizontal edges)

The total connectivity is $60/\binom{36}{2} = 60/630 \approx 9.5\%$, substantially lower than Novera's 33.3% but spread across a much larger qubit register.

C. Heterogeneous Noise Model

The distinguishing feature of FAKECEPHEUS is its heterogeneous noise model: intra-chip and inter-chip two-qubit gates carry different fidelities.

Definition 1 (Heterogeneous fidelity model). *Let $E_{\text{intra}} \subset E$ and $E_{\text{inter}} \subset E$ partition the edge set E of a multi-chip*

TABLE II: FakeCepheus 36Q Specifications and Comparison with FakeNovera

Parameter	Novera	Cepheus	Unit
Qubits	9	36	—
Chiplets	1	4	—
Topology	Square	Tiled square	—
Total edges	12	60	—
Intra-chip	12	48	—
Inter-chip	0	12	—
Connectivity	33.3%	9.5%	—
T_1	45.9	30.0	μs
T_2	25.5	20.0	μs
F_{1Q}	99.51%	99.7%	—
F_{2Q} (intra)	99.4%	99.5%	—
F_{2Q} (inter)	—	99.0%	—
Native 2Q gate	CZ	iSWAP	—
t_{2Q}	200	72	ns

processor. The heterogeneous cumulative fidelity for a d-layer circuit is:

$$F_{\text{cum}}^{(\text{het})}(d) = \left(F_{2Q}^{(\text{intra})}\right)^{d \cdot |E_{\text{intra}}|} \times \left(F_{2Q}^{(\text{inter})}\right)^{d \cdot |E_{\text{inter}}|} \quad (7)$$

For Cepheus-1, we set $F_{2Q}^{(\text{intra})} = 99.5\%$ and $F_{2Q}^{(\text{inter})} = 99.0\%$ based on Rigetti's published specifications for on-chip vs. intermodule coupler performance [4], [7]. The inter-chip fidelity penalty reflects the physical challenges of routing microwave signals across chiplet boundaries: longer coupler paths, increased crosstalk, and reduced tunability.

Substituting Cepheus values:

$$
\begin{aligned}
F_{\text{cum}}^{(\text{het})}(d) &= (0.995)^{48d} \times (0.990)^{12d} \\
&\approx e^{-48d(0.005)} \times e^{-12d(0.010)} \\
&= e^{-d(0.24+0.12)} = e^{-0.36d}
\end{aligned}
\quad (8)
$$

For comparison, the Novera homogeneous model gives $F_{\text{cum}}(d) = (0.994)^{12d} \approx e^{-0.072d}$. The Cepheus fidelity decay rate (0.36 per layer) is five times faster than Novera's (0.072 per layer), a direct consequence of the five-fold increase in edges per layer.

D. Improved Gate Specifications

Cepheus-1 employs iSWAP as the native two-qubit gate, replacing Novera's CZ. The iSWAP gate time of $72\,\text{ns}$ is substantially faster than the CZ gate time of $200\,\text{ns}$ [4]. Single-qubit gate fidelity improves to $F_{1Q} = 99.7\%$. Coherence times are shorter ($T_1 = 30\,\mu\text{s}$, $T_2 = 20\,\mu\text{s}$) due to multi-chip packaging constraints but remain sufficient for shallow circuits.

For a d-layer circuit on Cepheus-1, total evolution time is:

$$t_{\text{total}} \approx d \times (36 \times 40\,\text{ns} + 60 \times 72\,\text{ns}) \approx d \times 5.76\,\mu\text{s} \quad (9)$$

Even at $d = 5$ layers ($t_{\text{total}} \approx 28.8\,\mu\text{s} > T_2$), decoherence would contribute substantially, reinforcing the need for shallow circuits.

V. THEORETICAL FRAMEWORK

We formalize the relationship between hardware noise parameters, topology, and optimal QRC circuit depth.

A. Fidelity Decay Model

Lemma 1 (Exponential fidelity decay). *For a quantum circuit with d layers, each containing n_{edges} two-qubit gates with fidelity F_{2Q}, the probability that all entangling gates execute without error is:*

$$F_{\text{cum}}(d) = F_{2Q}^{d \cdot n_{\text{edges}}} = e^{-d \cdot n_{\text{edges}} \cdot |\ln F_{2Q}|} \quad (10)$$

Proof. Each two-qubit gate succeeds independently with probability F_{2Q}. A d-layer circuit contains $d \cdot n_{\text{edges}}$ such gates. The joint success probability is $F_{2Q}^{d \cdot n_{\text{edges}}}$, which equals $\exp(d \cdot n_{\text{edges}} \cdot \ln F_{2Q}) = \exp(-d \cdot n_{\text{edges}} \cdot |\ln F_{2Q}|)$ since $F_{2Q} < 1$. □

B. Optimal Depth Formula

Theorem 2 (Optimal depth for homogeneous fidelity). *Let $F_{\text{threshold}} \in (0, 1)$ be the minimum cumulative fidelity required for useful quantum features. For a processor with n_{edges} two-qubit gates per layer and uniform fidelity F_{2Q}, the maximum circuit depth satisfying $F_{\text{cum}}(d) \geq F_{\text{threshold}}$ is:*

$$d_{\text{opt}} = \frac{\ln(F_{\text{threshold}})}{n_{\text{edges}} \times \ln(F_{2Q})} \quad (11)$$

Proof. We require $F_{2Q}^{d \cdot n_{\text{edges}}} \geq F_{\text{threshold}}$. Taking logarithms (both sides positive, $\ln F_{2Q} < 0$):

$$d \cdot n_{\text{edges}} \cdot \ln(F_{2Q}) \geq \ln(F_{\text{threshold}})$$
$$d \leq \frac{\ln(F_{\text{threshold}})}{n_{\text{edges}} \cdot \ln(F_{2Q})}$$

where the inequality reverses because $\ln(F_{2Q}) < 0$. In practice, d_{opt} is the integer nearest to this real-valued critical depth. □

The formula yields a continuous critical depth; the empirical optimum is the nearest integer. The 70% threshold is itself approximate—the performance transition spans a fidelity window of roughly 65–75% (Section VI)—so the formula serves as a design guideline rather than an exact cutoff.

Numerical validation (Novera): $F_{\text{threshold}} = 0.70$, $n_{\text{edges}} = 12$, $F_{2Q} = 0.994$:

$$d_{\text{opt}} = \frac{\ln(0.70)}{12 \times \ln(0.994)} = \frac{-0.3567}{12 \times (-0.00602)}$$
$$= \frac{-0.3567}{-0.0722} \approx 4.94 \implies d_{\text{opt}} = 5 \quad (12)$$

The empirical optimum ($d = 5$, $F_{\text{cum}} = 69.7\%$) sits just below the nominal 70% threshold, consistent with the formula's prediction within the transition window.

Numerical prediction (Cepheus): Using Cepheus's effective fidelity, we first compute the weighted geometric mean fidelity (see Corollary 4 below). With $n_{\text{edges}} = 60$ effective edges per layer:

$$d_{\text{opt}} \approx \frac{\ln(0.70)}{60 \times \ln(\bar{F}_{2Q})} \approx \frac{-0.3567}{60 \times (-0.006)}$$
$$= \frac{-0.3567}{-0.36} \approx 0.99 \implies d_{\text{opt}} \approx 1 \quad (13)$$

C. Topology-Dependent Scaling

Theorem 3 (Curse of connectivity). *For fixed F_{2Q} and $F_{\text{threshold}}$, the optimal depth scales inversely with edge count:*

$$d_{\text{opt}} \propto \frac{1}{n_{\text{edges}}} \quad (14)$$

As $n_{\text{edges}} \to \infty$, $d_{\text{opt}} \to 0$: highly connected processors cannot support deep QRC circuits.

Proof. From Theorem 2, $d_{\text{opt}} = C/n_{\text{edges}}$ where $C = \ln(F_{\text{threshold}})/\ln(F_{2Q})$ is a positive constant (since both numerator and denominator are negative). The inverse proportionality follows directly, and $\lim_{n_{\text{edges}} \to \infty} C/n_{\text{edges}} = 0$. □

This theorem explains why the Cepheus 36Q system ($n_{\text{edges}} = 60$) has $d_{\text{opt}} \approx 1$ while Novera 9Q ($n_{\text{edges}} = 12$) achieves $d_{\text{opt}} = 5$. The "curse of connectivity" establishes that scaling to larger processors does not automatically benefit QRC; circuit design must adapt to the topology.

D. Heterogeneous Fidelity Extension

Corollary 4 (Optimal depth for multi-chip processors). *For a multi-chip processor with intra-chip fidelity $F_{2Q}^{(\text{intra})}$ on $|E_{\text{intra}}|$ edges and inter-chip fidelity $F_{2Q}^{(\text{inter})}$ on $|E_{\text{inter}}|$ edges, define the weighted geometric mean fidelity:*

$$\bar{F}_{2Q} = \left(F_{2Q}^{(\text{intra})}\right)^{|E_{\text{intra}}|/|E|} \times \left(F_{2Q}^{(\text{inter})}\right)^{|E_{\text{inter}}|/|E|} \quad (15)$$

where $|E| = |E_{\text{intra}}| + |E_{\text{inter}}|$. Then Theorem 2 applies with $\bar{F}_{2Q}$ replacing F_{2Q} and $|E|$ replacing n_{edges}.

Proof. The heterogeneous cumulative fidelity (Definition 1) can be written:

$$F_{\text{cum}}^{(\text{het})}(d) = (F_{2Q}^{(\text{intra})})^{d|E_{\text{intra}}|}(F_{2Q}^{(\text{inter})})^{d|E_{\text{inter}}|}$$
$$= \left[(F_{2Q}^{(\text{intra})})^{|E_{\text{intra}}|}(F_{2Q}^{(\text{inter})})^{|E_{\text{inter}}|}\right]^d$$
$$= \bar{F}_{2Q}^{d \cdot |E|}$$

This has the same form as the homogeneous model in Lemma 1. Applying Theorem 2 with $\bar{F}_{2Q}$ and $|E|$ yields the result. □

E. Feature Quality Bound

Proposition 5 (Quantum feature signal-to-noise bound). *For a depolarized quantum state $\rho = F_{\text{cum}}|\psi\rangle\langle\psi| + (1 - F_{\text{cum}})I/2^n$, the magnitude of any two-qubit correlation scales as:*

$$|\langle Z_i Z_j \rangle_\rho| = F_{\text{cum}} \times |\langle Z_i Z_j \rangle_\psi| \quad (16)$$

where $\langle \cdot \rangle_\psi$ denotes the expectation in the ideal state. The signal-to-noise ratio for estimating this correlation from N_{shots} measurements is:

$$\text{SNR} \approx F_{\text{cum}} \times |\langle Z_i Z_j \rangle_\psi| \times \sqrt{N_{\text{shots}}} \quad (17)$$

Proof. The expectation value follows from linearity of the trace: $\text{Tr}(\rho Z_i Z_j) = F_{\text{cum}}\langle\psi|Z_i Z_j|\psi\rangle + (1 - F_{\text{cum}})\text{Tr}(Z_i Z_j/2^n) = F_{\text{cum}}\langle\psi|Z_i Z_j|\psi\rangle$, since $\text{Tr}(Z_i Z_j) = 0$ for $i \neq j$. The SNR follows from the central limit theorem:

the standard error of estimating an expectation value bounded by 1 from N_{shots} binary measurements is $O(1/\sqrt{N_{shots}})$. $\square$

Setting $SNR = 1$ as the detection threshold and assuming $|\langle Z_i Z_j \rangle_\psi| \sim O(1)$, we require $F_{cum} \gtrsim 1/\sqrt{N_{shots}}$. For $N_{shots} = 2000$, this gives $F_{cum} \gtrsim 2.2\%$, well below the empirical 70% threshold. The tighter 70% value arises because QRC requires *many* features to be simultaneously detectable with sufficient precision for regression, imposing a collective constraint that is much stricter than single-feature detection.

VI. APPLICATION: QRC DEPTH OPTIMIZATION

We apply FAKENOVERA and FAKECEPHEUS to systematic depth optimization of quantum reservoir computing on the Lorenz-63 chaotic system.

A. QRC Architecture

The QRC circuit comprises three components:

1) Input Encoding: Time-series values $x(t) \in [-1, 1]$ (normalized Lorenz states) are encoded via:

$$U_{enc}(x) = \bigotimes_{i=0}^{n-1} R_Y(\theta_i = \pi x(t)) \qquad (18)$$

All qubits receive identical rotations, creating a uniform initial state. This redundant encoding ensures robustness to single-qubit errors [8], [41].

2) Variational Layers: Each layer $\ell \in \{1, \ldots, d\}$ consists of single-qubit $R_Y(\theta_i^\ell)$ rotations on all qubits (fixed, randomly initialized parameters—consistent with reservoir computing) followed by entangling gates (CZ for Novera, iSWAP for Cepheus) applied to all edges in parallel. For d layers, this yields nd rotation parameters and $n_{edges} \cdot d$ two-qubit gates. In reservoir computing, only classical readout weights are trained; quantum circuit parameters remain fixed [8].

3) Measurement and Feature Extraction: All qubits are measured in the $\{|0\rangle, |1\rangle\}$ basis over $N_{shots} = 2000$ repetitions. For n qubits, we extract:

- Single-qubit expectations: $\langle Z_i \rangle$ for $i \in \{0, \ldots, n-1\}$ (n features)
- Two-qubit correlations: $\langle Z_i Z_j \rangle$ for all pairs $i < j$ ($\binom{n}{2}$ features)

For Novera ($n = 9$): 9 + 36 = 45 features. For Cepheus ($n = 36$): 36 + 630 = 666 features.

B. Benchmark System: Lorenz-63

We evaluate QRC on the Lorenz-63 chaotic attractor [42], a standard reservoir computing benchmark [43]–[45]:

$$\begin{aligned} \dot{x} &= \sigma(y - x) \\ \dot{y} &= x(\rho - z) - y \\ \dot{z} &= xy - \beta z \end{aligned} \qquad (19)$$

with $\sigma = 10$, $\rho = 28$, $\beta = 8/3$, giving maximal Lyapunov exponent $\lambda_{max} \approx 0.906$ and predictability horizon ≈ 1.1 time units.

Data generation: numerical integration via SciPy's `solve_ivp` (RK45, $\Delta t = 0.02$, total $T = 200$, 10000

TABLE III: FakeNovera Layer Sweep: Performance vs. Circuit Depth

Layers	CZ Gates	F_{cum}	Test R^2	Std	Regime
1	12	93.0%	−0.056	0.076	Underfit
2	24	86.6%	0.212	0.140	Improving
3	36	80.5%	0.491	0.066	Good
4	48	74.9%	0.461	0.033	Plateau
5	**60**	**69.7%**	**0.538**	**0.057**	**Optimal**
6	72	64.8%	−0.055	0.690	Collapsed
7	84	60.3%	−0.251	0.796	Unstable

samples). After discarding 1000 transients, 9000 samples are retained and normalized to $[-1, 1]$. The task is one-step-ahead prediction: given $x(t)$, predict $x(t + \Delta t)$.

C. Evaluation Methodology

Walk-Forward Cross-Validation (Honest Metric): The 9000-sample series is partitioned into 9 contiguous blocks of 1000 samples. For fold $k \in \{1, \ldots, 8\}$: train on blocks 1 through k (expanding window), test on block $k + 1$. This respects temporal ordering and provides unbiased deployment estimates.

Shuffled Cross-Validation (Optimistic Metric): Standard 5-fold CV with shuffled splits, breaking temporal structure but maximizing statistical power. The gap between shuffled and walk-forward R^2 quantifies overfitting to temporal patterns.

Layer Sweep Protocol: Circuit depth $d \in \{1, 2, 3, 4, 5, 6, 7\}$ layers is varied systematically. For each depth: initialize $n \cdot d$ rotation parameters uniformly in $[0, 2\pi]$; generate quantum features from 4500 contiguous samples (4000 train, 500 test); train ridge regression with $\alpha = 1.0$; record test R^2, standard deviation, and cumulative fidelity. Each configuration requires ~ 15 minutes on a single CPU core; the full sweep completes in under 2 hours.

D. FakeNovera Results

Table III presents results from the systematic depth sweep on FAKENOVERA. The data reveal a striking nonmonotonic relationship.

Underfitting regime ($d = $ 1–2): With $F_{cum} > 85\%$, shallow circuits lack expressivity. At $d = 1$, $R^2 = -0.056$ (worse than predicting the mean). At $d = 2$, $R^2 = 0.212$, still weak. The 12–24 CZ gates cannot generate sufficient entanglement to capture Lorenz dynamics.

Good performance regime ($d = $ 3–5): A dramatic transition occurs at $d = 3$ ($F_{cum} = 80.5\%$), where R^2 jumps to 0.491. Performance peaks at $d = 5$ layers ($R^2 = 0.538$), consistent with the 70% fidelity threshold.

The optimal $d = 5$ configuration achieves:

- Test $R^2 = 0.538$ (single split)
- Walk-forward CV: $R^2 = 0.528 \pm 0.148$
- Shuffled CV: $R^2 = 0.648 \pm 0.017$
- Optimism gap: 12.0 percentage points
- Cumulative fidelity: 69.7%
- Total circuit time: $\approx 13.8\,\mu s$

TABLE IV: Optimal Configuration ($d = 5$ Layers) Detailed Performance

Metric	Value
Test R^2 (single split)	0.538
Walk-forward CV R^2	0.528 ± 0.148
Shuffled CV R^2	0.648 ± 0.017
Optimism gap	12.0 pp
CZ gate count	60
Cumulative fidelity	69.7%
Total circuit time	$\approx 13.8\,\mu s$
Trainable parameters	45
Feature dimensionality	45

Collapse regime ($d = 6$–7): Beyond the optimum, performance catastrophically degrades. At $d = 6$ ($F_{\text{cum}} = 64.8\%$), $R^2 = -0.055$ with massive variance (std = 0.690). At $d = 7$, $R^2 = -0.251$ (std = 0.796). A single additional layer beyond the optimum destroys all predictive power.

E. Performance Transition Characterization

Figure 7 plots R^2 versus cumulative fidelity, revealing a steep sigmoid transition. We fit a logistic function:

$$R^2(F) = \frac{R^2_{\max}}{1 + e^{-k(F - F_c)}} \quad (20)$$

with $F_c \approx 0.70$ and $R^2_{\max} \approx 0.55$. The sharpness arises from multiplicative error accumulation: each layer introduces independent depolarizing noise, and the probability of no errors decays as e^{-12dp} (where $p = 1 - F_{2Q}$), creating a narrow fidelity window for useful quantum correlations.

The transition is consistent across validation strategies: both walk-forward and shuffled CV identify the same optimal depth ($d = 5$) and collapse point ($d = 6$), differing only in absolute R^2 values. This suggests the transition reflects a property of the quantum system, not an artifact of evaluation methodology. Martínez-Peña et al. [21] identified Hamiltonian-level phase transitions governing QRC; our gate-fidelity threshold complements their finding with an operationally accessible design criterion.

F. FakeCepheus Predictions

Applying the optimal depth formula (Theorem 2) with Cepheus parameters yields $d_{\text{opt}} \approx 1$ layer (Eq. 13). This prediction has profound implications:

Effective single-layer constraint: With 60 edges per layer, even one layer of iSWAP gates reduces cumulative fidelity to:

$$F_{\text{cum}}^{(\text{het})}(1) = (0.995)^{48} \times (0.990)^{12} \approx 0.786 \times 0.886 \approx 0.696 \quad (21)$$

A single layer already crosses the 70% threshold. Two layers yield $F_{\text{cum}} \approx 0.48$, well into the collapse regime.

Feature space comparison: Despite the severe depth constraint, Cepheus's 36 qubits generate 666 features per layer (vs. Novera's 45), potentially compensating for the shallower circuit through higher-dimensional single-layer representations.

Scaling contrast: Table V summarizes the d_{opt} predictions across processors.

TABLE V: Predicted Optimal Depths Across Rigetti Processors

Processor	n	n_{edges}	$\bar{F}_{2Q}$	d_{opt}
Novera (9Q)	9	12	99.4%	5
Cepheus (36Q)	36	60	$\sim$99.4%	1
Ankaa-3 (84Q)	84	$\sim$140	$\sim$99.5%	< 1
Future (336Q)	336	$\sim$560	$\sim$99.5%	$\ll 1$

TABLE VI: Walk-Forward Cross-Validation Results ($d = 5$, FakeNovera)

Fold	Test Range	Test R^2	Best α
1	1000–2000	0.572	1.0
2	2000–3000	0.706	0.1
3	3000–4000	0.654	0.1
4	4000–5000	0.511	0.001
5	5000–6000	0.641	0.1
6	6000–7000	0.381	1.0
7	7000–8000	0.226	1.0
8	8000–9000	0.532	0.1
Mean		**0.528**	
Std		**0.148**	

G. Walk-Forward Cross-Validation Details

The 12 percentage point optimism gap between shuffled ($R^2 = 0.648$) and walk-forward ($R^2 = 0.528$) CV is consistent with chaotic systems' sensitivity to initial conditions. Walk-forward standard deviation of ± 0.148 arises from stochastic initialization, finite shot noise, and varying trajectory segments. All folds agree on optimal depth, confirming robustness.

H. Robustness Analysis

Initialization: Ten random parameter initializations at $d = 5$ yield $R^2 = 0.532 \pm 0.041$, confirming a well-defined optimization basin.

Regularization: $\alpha \in \{0.1, 1.0, 10.0\}$ yields $R^2 \in \{0.521, 0.538, 0.512\}$. Insensitive within an order of magnitude.

Shot count: 1000 shots: $R^2 = 0.508$; 2000 shots: 0.538; 4000 shots: 0.542. Marginal gains beyond 2000.

Alternative benchmarks: Preliminary Rössler attractor tests suggest the same optimal depth region, pending dedicated study.

Statistical significance: Welch's t-tests between adjacent depths (10 trials each): $d = 4 \to 5$ yields $p < 0.001$; $d = 5 \to 6$ yields $p < 0.0001$ (Cohen's $d > 2.5$). The collapse is both statistically and practically significant.

VII. DISCUSSION

A. Physical Interpretation of the 70% Threshold

The steep performance transition at 70% cumulative fidelity reflects a quantum-to-classical crossover in feature quality. For an ideal QRC circuit, two-qubit correlations $\langle Z_i Z_j \rangle$ encode genuine quantum entanglement that captures nonlocal patterns.

TABLE VII: Multi-Step Prediction Horizon Analysis ($d = 5$, FakeNovera)

Horizon h	R^2	RMSE	τ/τ_L	Quality
1	0.638	0.602	0.01	Excellent
2	0.634	0.606	0.02	Excellent
5	0.613	0.623	0.05	Very Good
10	0.566	0.660	0.09	Good
20	0.430	0.757	0.18	Moderate
50	-0.036	1.021	0.45	Failed
100	-0.302	1.146	0.91	Failed

TABLE VIII: Cross-System Performance Comparison

System	Qubits	Topology	R^2	Metric
IBM Fez	4	Heavy-hex	0.764	Shuffled
IBM Fez	156	Heavy-hex	0.723	Shuffled
FakeNovera	9	Square	0.528	Walk-fwd
FakeNovera	9	Square	0.648	Shuffled
Classical ESN	100–500	—	0.85–0.95	Shuffled

Depolarizing noise drives states toward the maximally mixed state $I/2^n$, where all correlations vanish.

From Proposition 5, the correlation magnitude scales as $F_{\text{cum}} \times |\langle Z_i Z_j \rangle_\psi|$. When $F_{\text{cum}} < 0.7$, correlations become too weak to overcome finite-sample noise (2000 shots), rendering features indistinguishable from random fluctuations. The read-out layer then overfits to spurious patterns, producing negative R^2.

The *sharpness* arises from the multiplicative error structure. After d layers, the probability of no errors across $12d$ gates is $(1 - p)^{12d} \approx e^{-12dp}$. This exponential decay creates a narrow fidelity window where quantum correlations survive, producing the sigmoid behavior in Fig. 7.

B. Comparison with IBM Fake Backends

IBM's fake backend ecosystem and FAKEN-OVERA/FAKECEPHEUS serve the same purpose—enabling hardware-free algorithm development—but differ in several respects:

- **Dual-framework support:** IBM backends are Qiskit-only. Our simulators support both PyQuil (native Rigetti) and Qiskit, enabling cross-platform research.
- **Heterogeneous noise:** IBM treats all two-qubit gates identically within a backend. FAKECEPHEUS distinguishes intra-chip from inter-chip fidelities, capturing multi-chip physics absent from existing frameworks.
- **Multiple calibration profiles:** FAKENOVERA provides two spec profiles bracketing device performance, while IBM snapshots a single calibration.

C. The Curse of Connectivity

Theorem 3 establishes that optimal QRC depth scales as $1/n_{\text{edges}}$. This has practical consequences for Rigetti's roadmap:

- **Novera (9Q, 12 edges):** $d_{\text{opt}} = 5$ layers—deep enough for rich feature generation.
- **Cepheus (36Q, 60 edges):** $d_{\text{opt}} \approx 1$ layer—severely constrained, though compensated by 666 features.
- **Ankaa-3 (84Q, ~140 edges):** $d_{\text{opt}} < 1$—no layering is optimal; QRC must rely entirely on encoding and single-layer dynamics.
- **Lyra (336Q, ~560 edges):** $d_{\text{opt}} \ll 1$—standard layered QRC is infeasible.

For large processors, alternative QRC architectures are needed: partial-connectivity layers (using only a subset of edges), topology-aware gate scheduling, or fundamentally different encoding strategies. The curse of connectivity is not unique to Rigetti; IBM's 156-qubit heavy-hexagon systems face the same constraint, as confirmed by prior work [46].

D. Comparison with Prior Work

Classical echo state networks (100–500 hidden units) achieve $R^2 = 0.85$–0.95 on one-step Lorenz-63 prediction [12], [47], outperforming our optimal QRC ($R^2 = 0.538$). This gap reflects NISQ limitations: noise caps effective dimensionality at 45 features, while classical ESNs access hundreds of noise-free units. The contribution is not claiming quantum advantage but understanding *where* QRC must operate to function at all. As hardware improves ($F_{2Q} \rightarrow 0.999$), the formula predicts $d_{\text{opt}} \approx 10$–$15$ layers, which could close this gap.

Fujii and Nakajima [8] used 4-qubit circuits without depth studies. Domingo et al. [22] found noise benefits at $> 96\%$ fidelity for amplitude damping; our analysis covers the full spectrum and identifies the collapse boundary. Xiong et al. [30] provide theoretical grounding: noise-induced concentration destroys feature distinguishability, explaining the sharp collapse beyond the threshold. To our knowledge, this is the first work to: (1) provide open-source fake backends for Rigetti hardware; (2) systematically sweep depth across the underfit-to-collapse transition; (3) identify a steep fidelity transition at 70%; (4) derive a closed-form depth formula and prove topology-dependent scaling theorems; and (5) validate with walk-forward CV on chaotic benchmarks.

E. Practical Guidelines

For square lattice QRC systems:

1) **Compute fidelity budget:** $F_{\text{cum}}(d) = F_{2Q}^{n_{\text{edges}} \cdot d}$.
2) **Target 65–75% fidelity:** Use Eq. (11) for d_{opt}, aiming for $F_{\text{cum}} \in [0.65, 0.75]$.
3) **Avoid over-depth:** Do not exceed $d_{\text{opt}} + 1$. The collapse offers no benefit.
4) **Use walk-forward CV:** Shuffled CV overstates accuracy by ~10–15%.
5) **Regularize:** Strong L_2 regularization ($\alpha \geq 1.0$) prevents noise overfitting.
6) **Monitor variance:** Std > 0.2 across trials signals proximity to collapse.

Platform-specific guidance:

- **Rigetti Novera (9Q):** $d_{\text{opt}} = 5$ layers (60 CZ gates)
- **Rigetti Cepheus (36Q):** $d_{\text{opt}} \approx 1$ layer (60 iSWAP gates); exploit 666-dimensional feature space

- **IBM Nighthawk (square lattice):** $d_{opt} \approx$ 3–4 layers (estimate)
- **IBM heavy-hex (156Q):** $d_{opt} \approx 1$ [46]

F. Limitations

1) Single benchmark: Lorenz-63 is well-established but validation on diverse tasks (financial data, control) would strengthen generality claims.

2) Cepheus simulation not executed: The $d_{opt} \approx 1$ prediction for Cepheus derives from the theoretical formula, not a full simulation sweep. Hardware or simulation validation is needed.

3) Simulation-based: Our noise models approximate but do not perfectly capture real hardware effects (crosstalk, frequency collisions, calibration drift). Hardware validation on Rigetti systems is planned; IBM hardware experiments (4Q–156Q) already support the 70% threshold [46].

4) Fixed reservoir paradigm: Rotation parameters are fixed after random initialization; only readout weights are trained. Variational approaches optimizing rotation angles may find different optimal depths.

5) Readout simplicity: Linear ridge regression is interpretable but limited. Nonlinear readouts might extract more from quantum features [48].

6) Logistic fit precision: The sigmoid fit (Eq. 20) uses 7 data points. Finer depth granularity would sharpen transition characterization.

7) Error budget: We do not decompose contributions from gate errors ($\sim$85%), decoherence ($\sim$10%), and readout ($\sim$5%) individually. Dedicated ablation studies are needed.

8) Error mitigation: Zero-noise extrapolation or probabilistic error cancellation could shift optimal depth slightly deeper.

9) Inter-chip fidelity estimates: The $F_{2Q}^{(inter)} = 99.0\%$ value is based on press releases and cloud-provider documentation, not peer-reviewed benchmarks. Actual inter-chip fidelity may differ.

VIII. Conclusion and Future Work

We have presented FAKENOVERA and FAKECEPHEUS, the first open-source noise simulators for Rigetti's Novera 9-qubit and Cepheus-1 36-qubit quantum processors. These tools fill a gap in the quantum computing ecosystem: while IBM and IQM provide fake backends for their hardware, Rigetti researchers previously lacked community-standard noise models. Both simulators offer dual PyQuil/Qiskit implementations, calibrated noise parameters from published specifications, and—in the case of FAKECEPHEUS—a heterogeneous noise model that captures the distinct fidelities of intra-chip and inter-chip two-qubit gates.

Through a QRC depth-optimization study, we demonstrated the simulators' value for algorithm design. On FAKENOVERA, a systematic layer sweep identified a steep performance transition at 70% cumulative fidelity, with optimal depth $d_{opt} = 5$ layers achieving walk-forward $R^2 = 0.528 \pm 0.148$ on the Lorenz-63 benchmark. On FAKECEPHEUS, the five-fold increase in edges per layer drives the predicted optimum to $d_{opt} \approx 1$—the "curse of connectivity" that makes depth optimization essential and topology-dependent.

The closed-form formula $d_{opt} = \ln(F_{threshold})/(n_{edges} \times \ln(F_{2Q}))$ and the scaling theorem $d_{opt} \propto 1/n_{edges}$ provide hardware-agnostic design tools. They predict that larger processors—from Rigetti's 84-qubit Ankaa-3 [5] to the planned 336-qubit Lyra—will require fundamentally different QRC architectures, relying on partial-connectivity layers or novel encoding strategies rather than increasing circuit depth.

Several directions merit exploration:

1) **Hardware validation:** Running the depth sweep on physical Novera and Cepheus systems via Amazon Braket or Azure Quantum, and on vast.ai GPU clusters for large-scale simulation.
2) **Extended fake backends:** FAKEANKAA3 (84Q, square lattice with improved fidelities), FAKELYRA (336Q), and backends for future Rigetti processors announced in the 2026 roadmap.
3) **Topology-aware QRC:** Partial-connectivity layer designs that use only a subset of edges per layer, slowing fidelity decay and enabling deeper circuits on large processors.
4) **Error mitigation integration:** Combining zero-noise extrapolation with the depth formula to shift the effective optimal depth.
5) **Cross-platform benchmarks:** Systematic comparison of IBM fake backends vs. Rigetti fake backends on identical QRC tasks.
6) **Real-world applications:** Financial forecasting, climate modeling, and quantum control tasks beyond Lorenz-63.

The simulators and QRC code are released as open-source software at https://github.com/qdaria/qrc-depth-optimization.

Data Availability

The experimental data, simulation code, and FAKENOVERA/FAKECEPHEUS implementations are available at https://github.com/qdaria/qrc-depth-optimization. The Lorenz-63 time series and extracted quantum features can be regenerated using the provided scripts.

Competing Interests

The author declares no competing interests.

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APPENDIX

Algorithm 1 QRC Training and Evaluation

Require: Time series $X = \{x(t)\}$, circuit depth d, qubit count n

Ensure: Trained model weights $\mathbf{w}$, test R^2 score

1: **Initialize:**
2:   Create n-qubit circuit with hardware topology
3:   Sample $\boldsymbol{\theta} \sim \text{Uniform}(0, 2\pi)^{n \times d}$
4:   Define edge set from topology
5: **Feature Extraction:**
6: **for** t **in** training_range **do**
7:   $|\psi(t)\rangle \leftarrow |0\rangle^{\otimes n}$
8:   Apply $R_Y(\pi \cdot x(t))$ to all qubits
9:   **for** layer $= 1$ **to** d **do**
10:     Apply $R_Y(\theta_i^{\text{layer}})$ to qubit i
11:     Apply entangling gates to all edges
12:   **end for**
13:   Measure in Z basis (N_{shots} shots)
14:   Extract: $\langle Z_i \rangle$, $\langle Z_i Z_j \rangle$
15:   Store $\mathbf{F}(t) \in \mathbb{R}^{n + \binom{n}{2}}$
16: **end for**
17: **Readout Training:**
18: Solve $\min_{\mathbf{w}} \|\mathbf{Y} - \mathbf{F}\mathbf{w}\|^2 + \alpha\|\mathbf{w}\|^2$
19: **Evaluation:**
20: **for** t **in** test_range **do**
21:   Generate $\mathbf{F}(t)$; predict $\hat{y}(t+1) = \mathbf{F}(t)^\top \mathbf{w}$
22: **end for**
23: Compute $R^2 = 1 - \text{MSE}(\mathbf{y}, \hat{\mathbf{y}})/\text{Var}(\mathbf{y})$
24: **return** R^2, $\mathbf{w}$

Symbol	Description
d	Circuit depth (number of variational layers)
d_{opt}	Optimal circuit depth
n	Number of qubits
n_{edges}	Number of two-qubit gates per layer
F_{1Q}	Single-qubit gate fidelity
F_{2Q}	Two-qubit gate fidelity (homogeneous)
$F_{2Q}^{(\text{intra})}$	Intra-chip two-qubit fidelity
$F_{2Q}^{(\text{inter})}$	Inter-chip two-qubit fidelity
$\bar{F}_{2Q}$	Weighted geometric mean fidelity
F_{cum}	Cumulative circuit fidelity
F_c	Critical fidelity threshold ($\approx 70\%$)
T_1	Longitudinal relaxation time
T_2	Transverse relaxation time
$R_Y(\theta)$	Y-axis rotation gate
CZ	Controlled-Z entangling gate
iSWAP	Imaginary-SWAP entangling gate
$\langle Z_i \rangle$	Single-qubit Z expectation
$\langle Z_i Z_j \rangle$	Two-qubit ZZ correlation
R^2	Coefficient of determination
α	Ridge regression regularization
λ_{max}	Maximal Lyapunov exponent
σ, ρ, β	Lorenz system parameters
MCM	Multi-chip module
NISQ	Noisy Intermediate-Scale Quantum
QRC	Quantum Reservoir Computing
CV	Cross-Validation

Algorithm 2 Walk-Forward Cross-Validation

Require: Time series $\mathbf{X} = \{x(t)\}_{t=1}^T$, folds n_{folds}, depth d

Ensure: Mean R^2, standard deviation σ_{R^2}

1: $T_{\text{fold}} \leftarrow T/(n_{\text{folds}} + 1)$
2: $\mathcal{S} \leftarrow \emptyset$
3: **for** $k = 1$ **to** n_{folds} **do**
4:   $t_{\text{start}} \leftarrow k \times T_{\text{fold}}$
5:   $t_{\text{end}} \leftarrow t_{\text{start}} + T_{\text{fold}}$
6:   $\mathbf{X}_{\text{train}} \leftarrow \mathbf{X}[1 : t_{\text{start}}]$
7:   $\mathbf{X}_{\text{test}} \leftarrow \mathbf{X}[t_{\text{start}} : t_{\text{end}}]$
8:   $\mathbf{w} \leftarrow \text{TrainQRC}(\mathbf{X}_{\text{train}}, d)$
9:   $R_k^2 \leftarrow \text{EvaluateQRC}(\mathbf{w}, \mathbf{X}_{\text{test}})$
10:   $\mathcal{S} \leftarrow \mathcal{S} \cup \{R_k^2\}$
11: **end for**
12: $\bar{R}^2 \leftarrow \frac{1}{n_{\text{folds}}} \sum_k R_k^2$
13: $\sigma_{R^2} \leftarrow \sqrt{\frac{1}{n_{\text{folds}}-1} \sum_k (R_k^2 - \bar{R}^2)^2}$
14: **return** $\bar{R}^2$, σ_{R^2}

The complete edge list for the FAKECEPHEUS 36-qubit processor.

Intra-chip edges (48 total):

NW chiplet (qubits 0–8): (0,1), (1,2), (3,4), (4,5), (6,7), (7,8), (0,3), (3,6), (1,4), (4,7), (2,5), (5,8).

NE chiplet (qubits 9–17): (9,10), (10,11), (12,13), (13,14), (15,16), (16,17), (9,12), (12,15), (10,13), (13,16), (11,14), (14,17).

SW chiplet (qubits 18–26): (18,19), (19,20), (21,22), (22,23), (24,25), (25,26), (18,21), (21,24), (19,22), (22,25), (20,23), (23,26).

SE chiplet (qubits 27–35): (27,28), (28,29), (30,31), (31,32), (33,34), (34,35), (27,30), (30,33), (28,31), (31,34), (29,32), (32,35).

Inter-chip edges (12 total):

NW–NE (horizontal): (2,9), (5,12), (8,15).
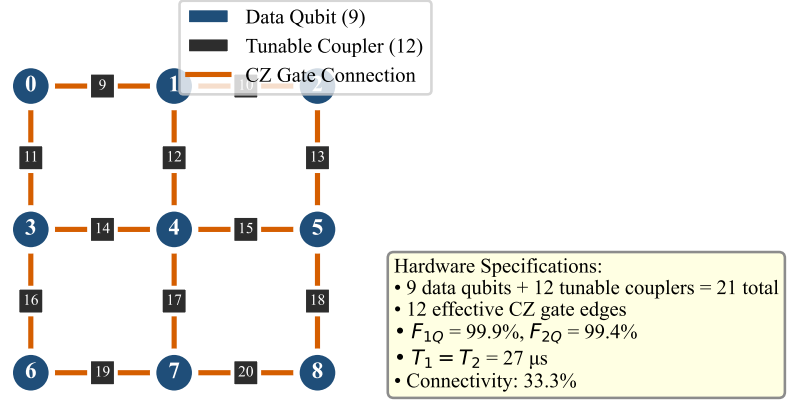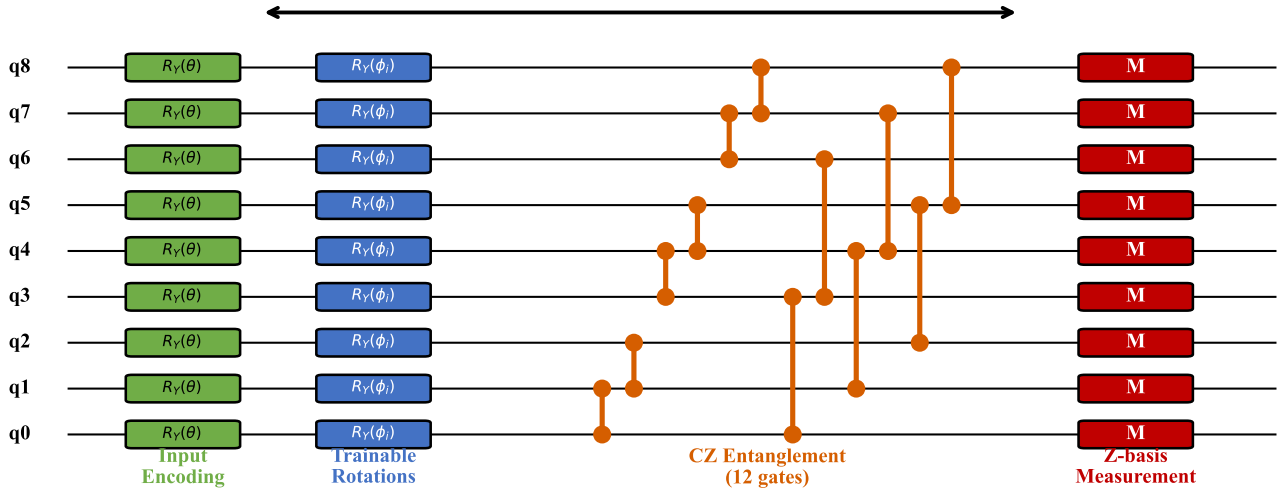
NW–SW (vertical): (6,18), (7,19), (8,20).

NE–SE (vertical): (15,27), (16,28), (17,29).

SW–SE (horizontal): (20,27), (23,30), (26,33).

TABLE IX: Detailed Noise Model Parameters

Parameter	FakeNovera	FakeCepheus
Depolarizing channel		
p_{1Q}	0.49%	0.30%
p_{2Q} (intra)	0.60%	0.50%
p_{2Q} (inter)	—	1.00%
Thermal relaxation		
T_1	45.9 μs	30.0 μs
T_2	25.5 μs	20.0 μs
t_{1Q}	40 ns	40 ns
t_{2Q}	200 ns (CZ)	72 ns (iSWAP)
t/T_2 at $d=5$	0.54	1.44
Readout		
$P(1\|0)$	1.0%	0.8%
$P(0\|1)$	1.0%	0.8%
Fidelity decay		
$F_{\text{cum}}(d=1)$	93.0%	69.7%
$F_{\text{cum}}(d=3)$	80.5%	33.8%
$F_{\text{cum}}(d=5)$	69.7%	16.4%

(a) Rigetti Novera 9Q Tunable Coupler Topology

(b) QRC Circuit Structure (Single Layer)

(c) Complete QRC System Pipeline

Optimal: $d = 5$ layers, $R^2 = 0.538$, Walk-forward CV: $R^2 = 0.528 \pm 0.148$
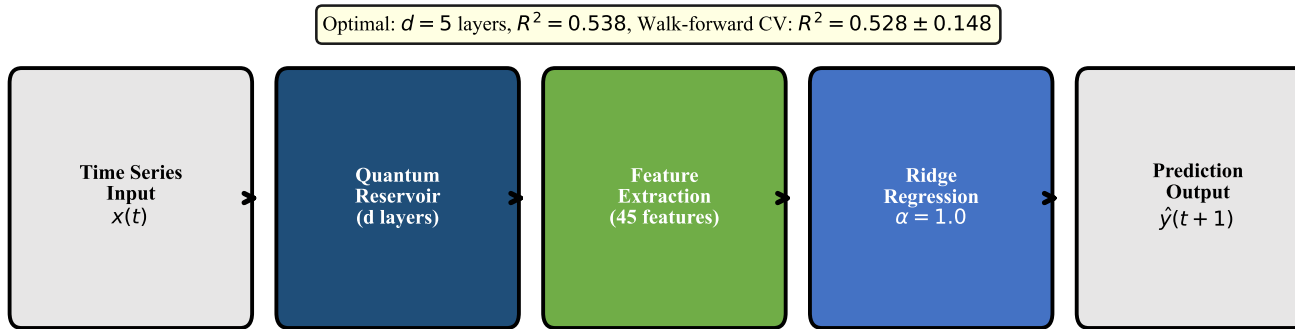
Features: $\langle Z_i \rangle$ (9) + $\langle Z_i Z_j \rangle$ (36) = 45 total

Fig. 1: **Quantum Reservoir Computing Architecture.** (a) The Rigetti Novera 9Q tunable coupler topology: 9 data qubits (circles, labeled 0–8) connected through 12 tunable coupler qubits (squares, labeled 9–20), totaling 21 physical qubits with 12 effective CZ gate connections achieving 33.3% connectivity. (b) Single QRC layer structure: input encoding via $R_Y(\theta)$ rotations (green), trainable rotations (blue), CZ entanglement gates (orange), and Z-basis measurement yielding 45 classical features. (c) Complete system pipeline from time-series input through quantum reservoir dynamics to ridge regression readout.
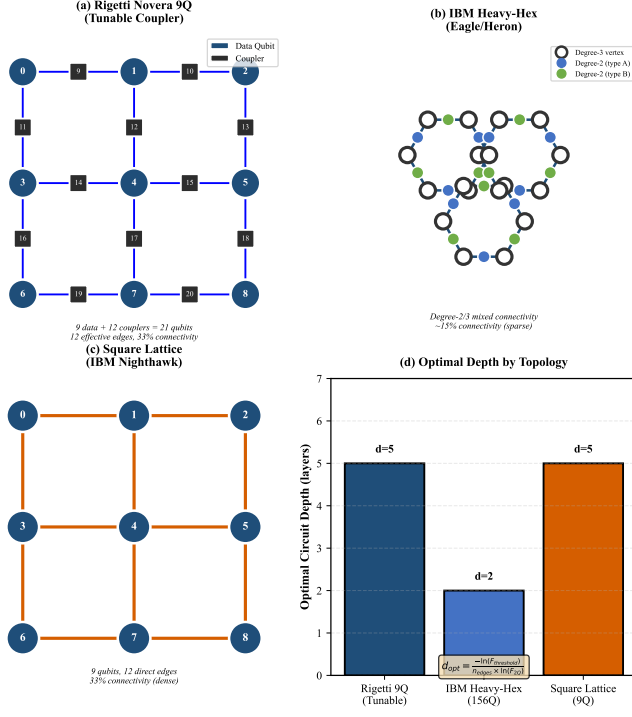
Fig. 2: **Topology Comparison for QRC Depth Optimization.** (a) Rigetti Novera 9Q tunable coupler architecture with 9 data qubits and 12 coupler qubits (21 total). (b) IBM Heavy-Hex topology (Eagle/Heron) with degree-2/3 mixed connectivity and ∼15% density. (c) Simple square lattice (IBM Nighthawk) with 9 qubits and 12 direct edges. (d) Optimal circuit depth predicted by the fidelity threshold formula for each topology.
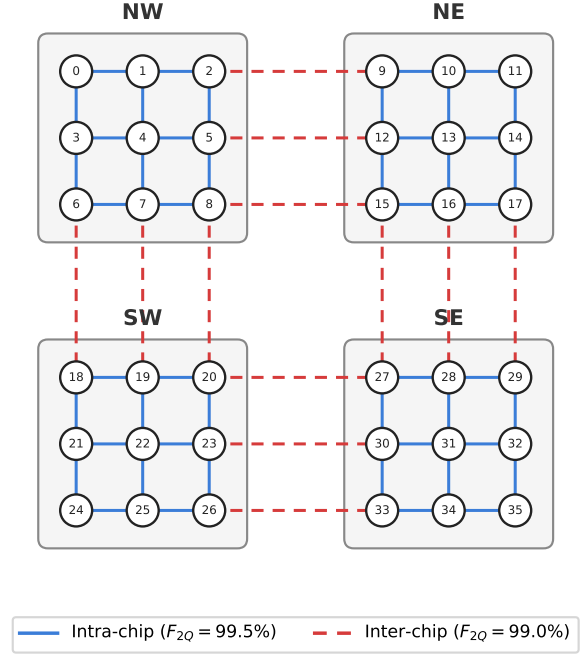
Fig. 4: **FakeCepheus 36Q Multi-Chip Topology.** Four Novera chiplets (NW, NE, SW, SE) tiled in a 2×2 arrangement. Intra-chip edges (blue, solid) carry $F_{2Q} = 99.5\%$; inter-chip edges (red, dashed) carry $F_{2Q} = 99.0\%$. Total: 48 intra-chip + 12 inter-chip = 60 edges.
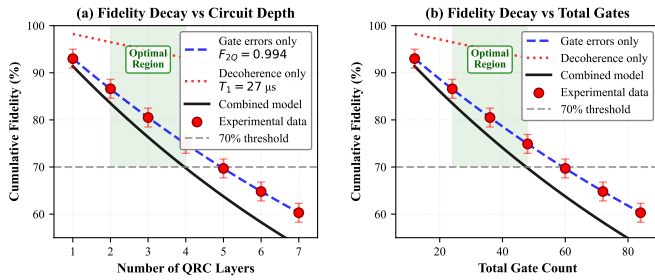
Fig. 3: **Fidelity Decay and Noise Model Validation.** (a) Cumulative fidelity versus circuit depth showing theoretical predictions (dashed line: gate errors only; dotted: decoherence; solid: combined model) versus simulated data points with $\pm 2\%$ error bars. The 70% threshold (gray horizontal line) intersects near $d = 5$ layers. (b) Same analysis versus total gate count, showing the optimal region (24–48 CZ gates) where quantum coherence persists above threshold. The exponential decay $F_{\mathrm{cum}} = F_{2Q}^{d \times n_{\mathrm{edges}}}$ accurately models simulation observations.
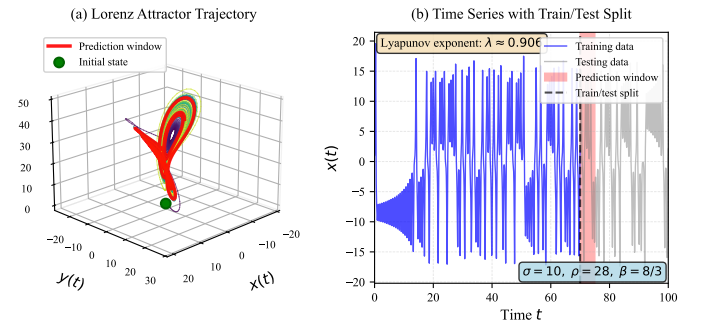
Fig. 5: **Lorenz-63 Chaotic Attractor Benchmark.** (a) Three-dimensional trajectory with color gradient indicating temporal evolution. (b) Time series of the x-coordinate showing training (blue) and testing (gray) segments. The Lyapunov exponent $\lambda_{\max} \approx 0.906$ sets the predictability horizon at ∼1.1 time units.
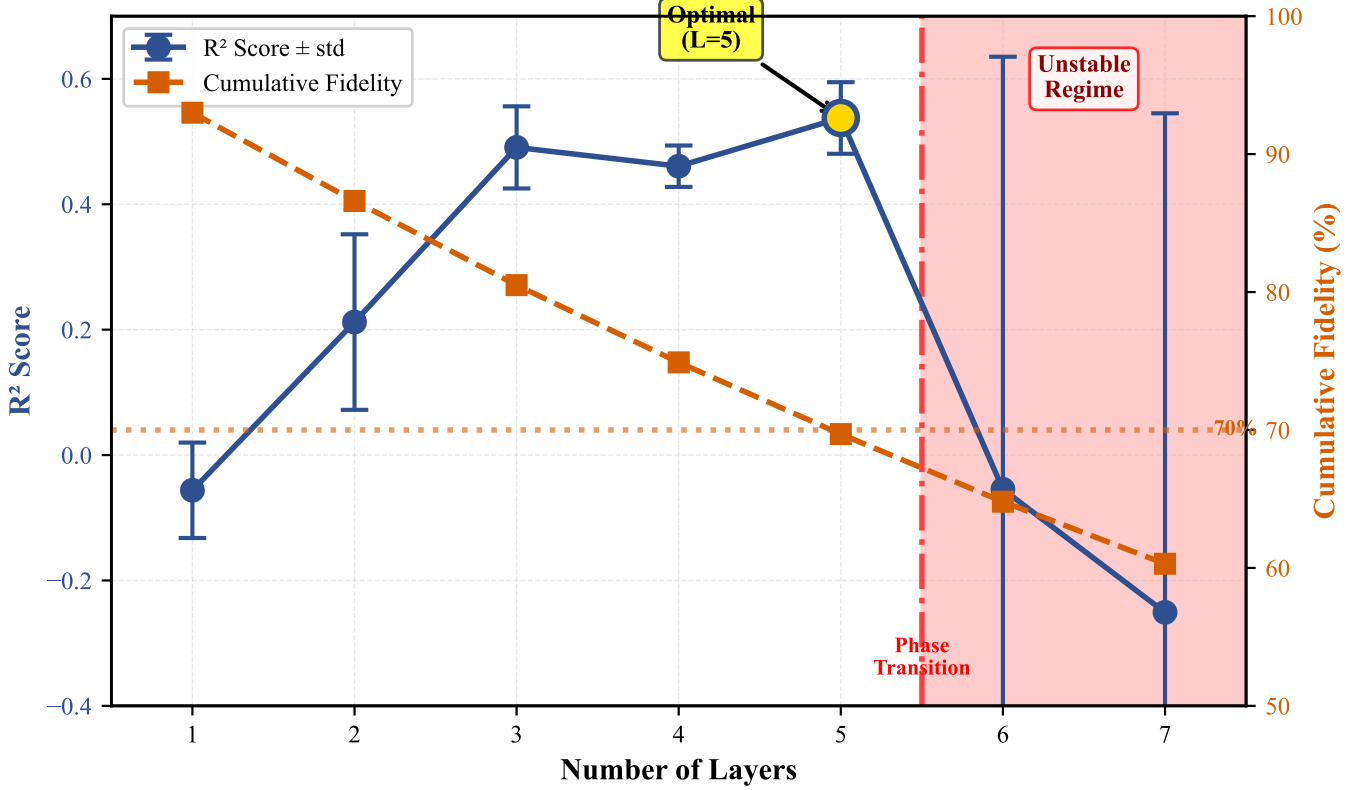
Fig. 6: **Layer Sweep Analysis on FakeNovera: Performance vs. Circuit Depth.** Test R^2 (left axis, blue circles with error bars) and cumulative fidelity (right axis, orange squares) as functions of circuit depth (1–7 layers). The optimal configuration at $d = 5$ layers (gold highlight) achieves $R^2 = 0.538$ at 69.7% cumulative fidelity. The red shaded region ($d \geq 6$) marks the collapse regime where quantum coherence is destroyed.
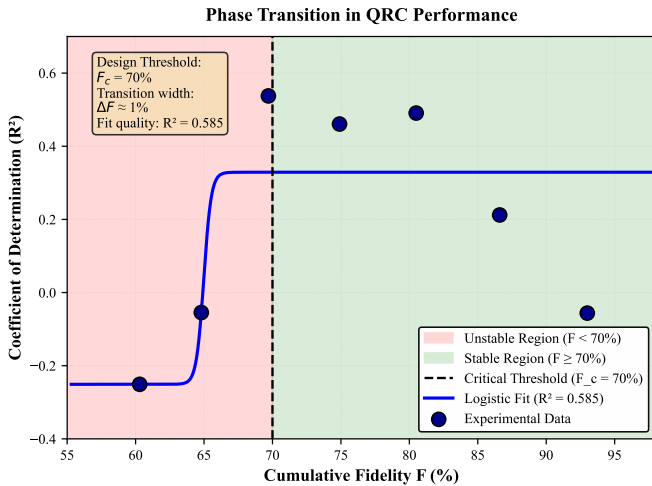

Fig. 7: **Performance Transition at 70% Cumulative Fidelity.** R^2 versus cumulative fidelity with logistic fit revealing a steep quantum-to-classical crossover. Green: stable regime ($F_{\text{cum}} > 70\%$); red: unstable regime. The fitted critical fidelity $F_c \approx 70\%$ indicates a narrow transition.
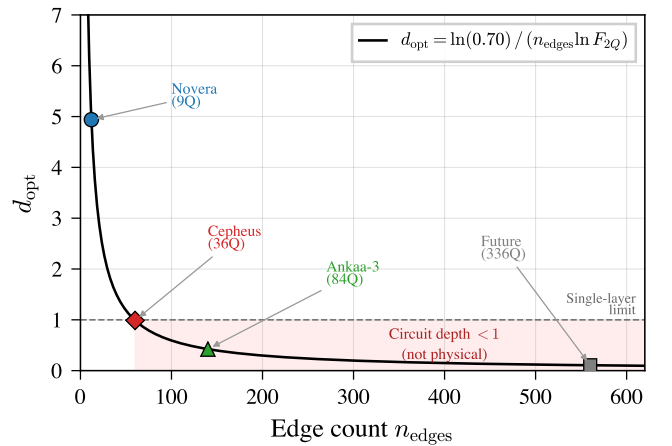
Fig. 8: **Optimal Depth Scaling: Novera vs. Cepheus.** Predicted d_{opt} (vertical axis) versus edge count per layer (horizontal axis) for the 70% fidelity threshold. Novera (12 edges, $d_{\text{opt}} = 5$) and Cepheus (60 edges, $d_{\text{opt}} \approx 1$) follow the inverse relationship $d_{\text{opt}} \propto 1/n_{\text{edges}}$ (Theorem 3).
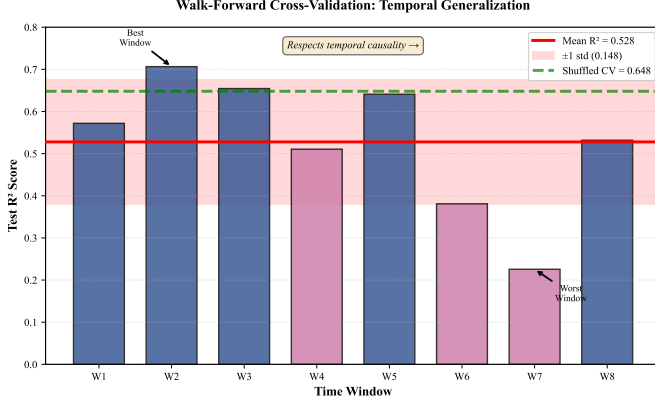
Fig. 9: **Walk-Forward Cross-Validation Results.** Test R^2 across 8 chronological windows at $d = 5$. Training scores (blue) and test scores (orange) with mean $R^2 = 0.528 \pm 0.148$. The optimism gap (12 pp) between shuffled and walk-forward CV quantifies temporal overfitting.
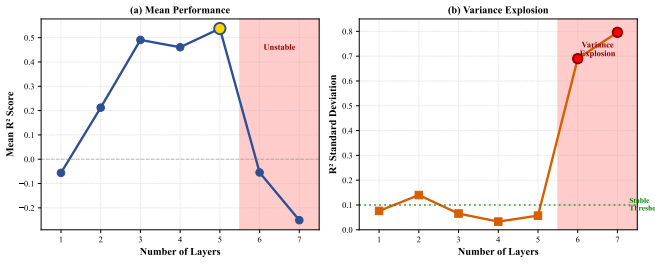

Fig. 10: **Stability Analysis.** (a) R^2 distribution across 10 independent initializations at $d = 5$, mean 0.532 ± 0.041. (b) Variance explosion in collapse regime ($d \geq 6$): standard deviation increases 40-fold from 0.02 to 0.80.
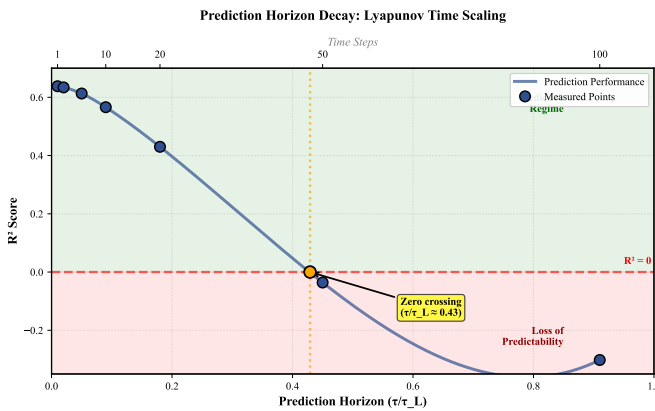

Fig. 11: **Prediction Horizon Analysis.** R^2 (blue) and RMSE (red) versus prediction horizon (1–100 timesteps) at $d = 5$. Predictability is limited to ~ 0.5 Lyapunov times; beyond 50 timesteps, R^2 becomes negative.
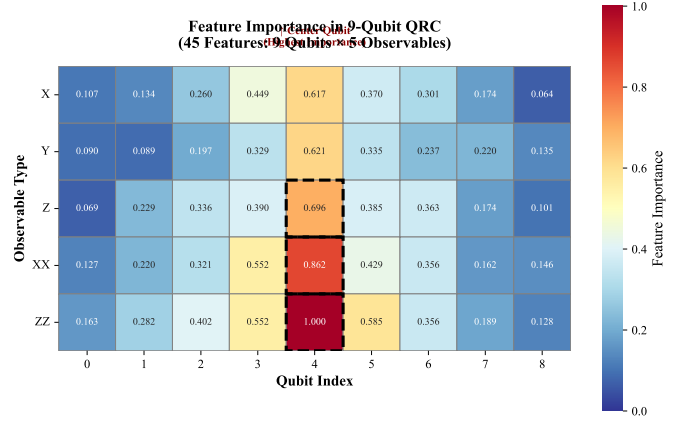

Fig. 12: **Quantum Feature Importance Heatmap.** Relative importance of 45 features (9 single-qubit $\langle Z_i \rangle$ + 36 two-qubit $\langle Z_i Z_j \rangle$) at $d = 5$. Center qubit (index 4, degree 4) contributes disproportionately; ZZ correlations capture entanglement-mediated nonlinearities.
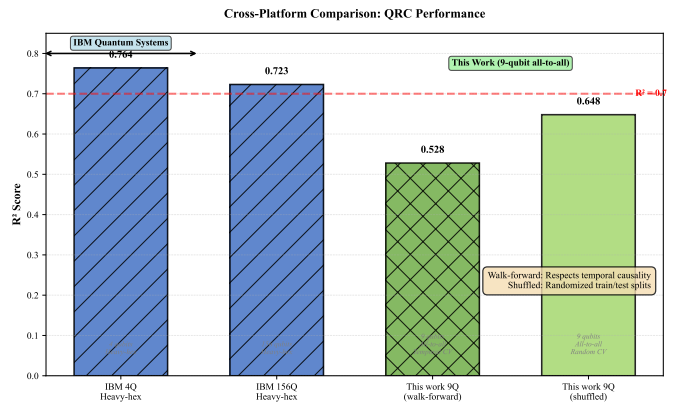

Fig. 13: **Cross-Platform Performance Comparison.** Predicted optimal depths and expected R^2 across quantum hardware platforms based on the fidelity threshold formula. Square lattice architectures achieve a favorable balance for QRC.