Name: Mohammad Elkholy

ID: 90020159

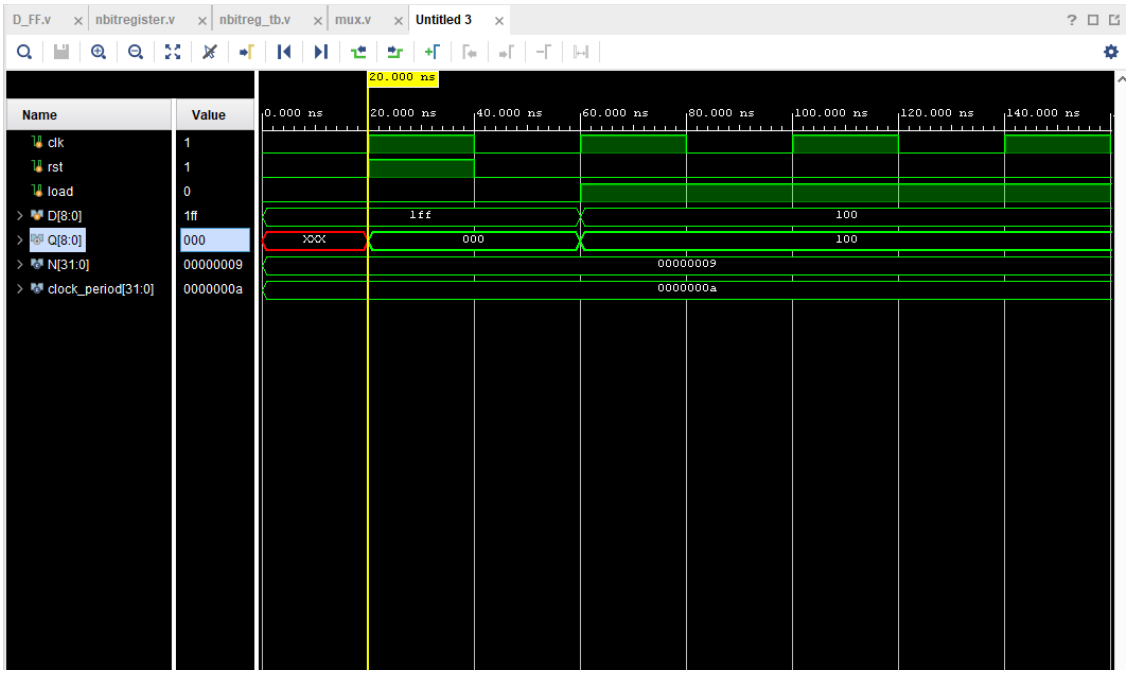
Team name: TwoBits

Team members: Mohammad Elkholy & Ahmed Bahssain

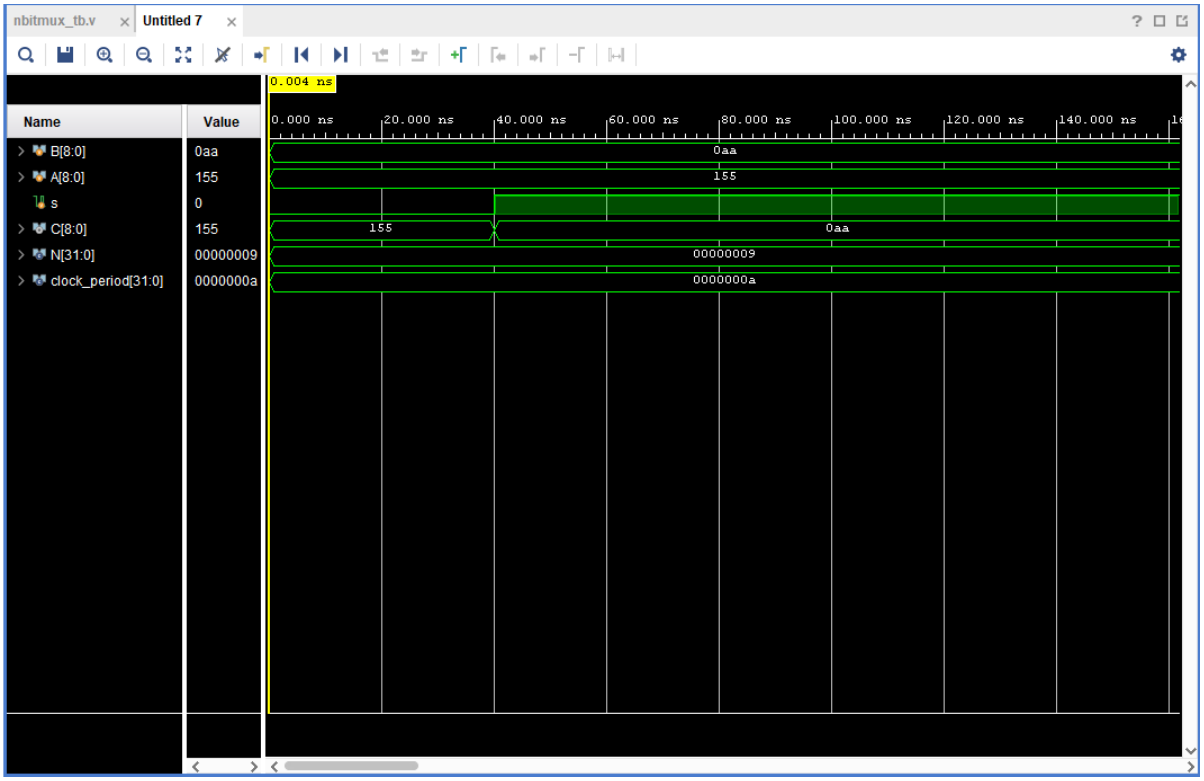
Lab # 3 Report

Summary:

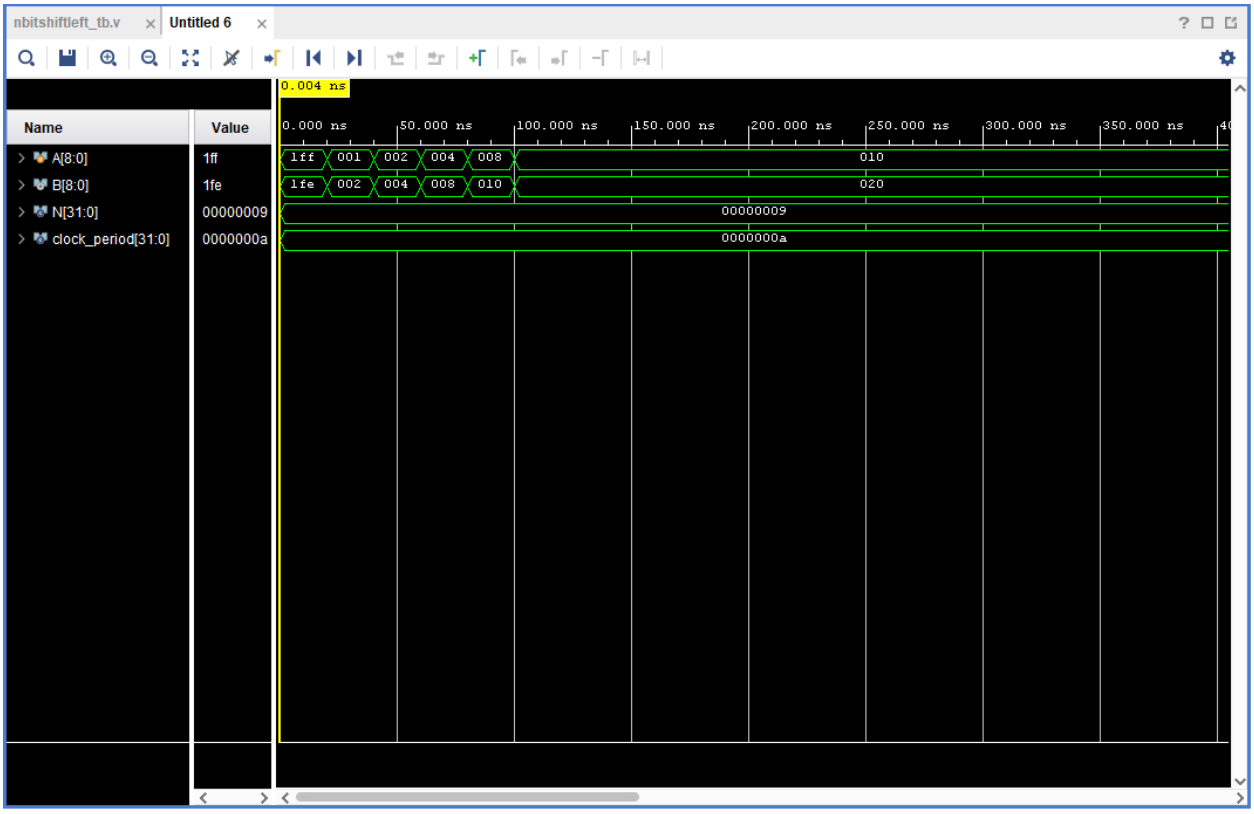
1. Expriment # 1: We implemented an N-bit register with load and reset controls. The register has a default parameter of N=8, which can be changed according to the number of bits we want to hold in the register. The register consists of N D-FlipFlops and N 2x1 MUXs. The D-FF store the values in the register, while the MUXs choose whether we should load the new value into the D-FFs or not. The input consist of an N-bit vector D containing the new values to be held by the register, the clock, reset and load. In order to generate an N-bit register, we need to generate N D-FFs and N 2x1 MUXs, we do so using a generate for loop inside the register module. The testbench tests the reset and load functionality and checking that it aligns with the rising edge of the clock. The register is first initialized to 0 by the reset. It is then loaded with value 256 (100 in hex), and it is loaded when we set load = 1 with the rising edge of the clock.



2. Experiment # 2: in this experiment we implemented an N-bit 2x1 MUXs, again we simply use a generate for loop to initialize the N 2x1 MUXs. The input consists of two vectors A and B of size N and a select bit and outputs to vector C, also of size N. We test the functionality by setting two vectors A = 341(155 in Hex) and B = 170 (aa in Hex) and we change the select bit and see the output in C change accordingly.



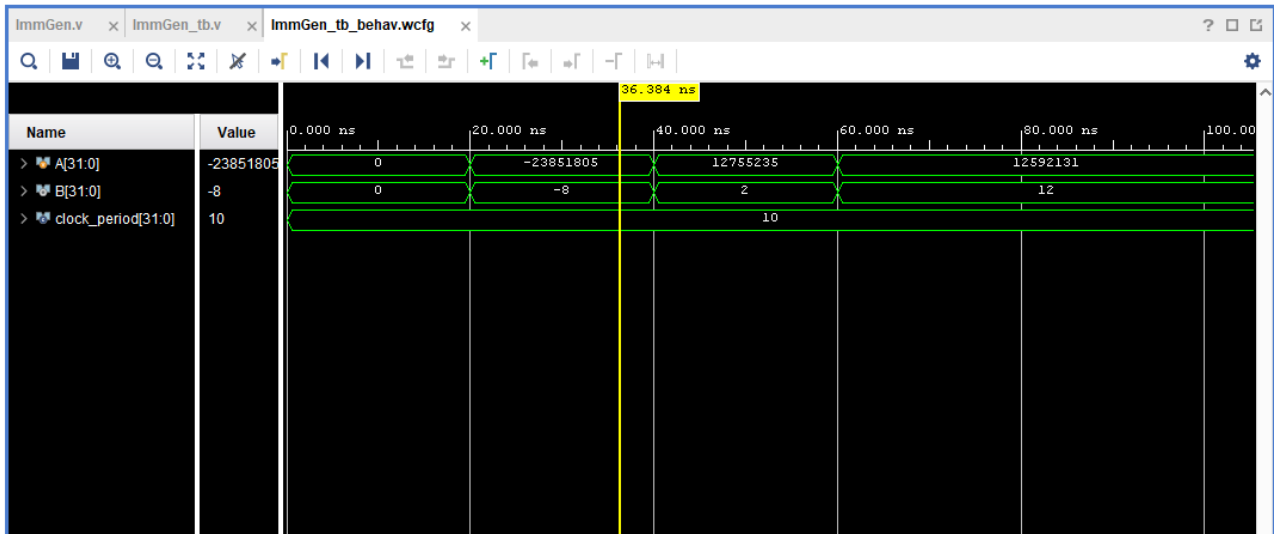
3. Experiment # 3: In this experiment we implemented an nbit shift left 1 module. We used the replication operator to take the last N-1 bits of the input and add a 0 bit to it to make it N-bits long. We tested this several times, firstly by setting A =511 (1ff in Hex) and seeing how the output vector changes. We then try that with powers of 2.



4. Experiment # 4: In this experiment, we implemented a module that generates immediates and sign extends them based on the instructions. We check the 7th bit for BEQ or (SW and LW) and 6th bit for LW or SW. We then generate the immediates and sign extend then using replication operator. We tested this module by generating machine code for 3 risc-v instructions and checking if immediates generated are correct.

Machine Code	Basic Code	Original Code
0x00c02403	lw x8 12(x0)	lw s0, 12(x0)
0x00c2a123	sw x12 2(x5)	sw x12, 2(x5)
0xfe940ce3	beq x8 x9 -8	beq s0, s1, main

```
#(clock_period *2)
// beq -> bit 6 = 1
A = 'hfe940ce3;
#(clock_period *2)
// sw -> bit 6 = 0, bit 5= 1
A = 'h00c2a123;
#(clock_period *2)
// lw -> bit 6 = 0, bit 5 = 0
A = 'h00c02403;
```



Nbit register with shift and load, load having priority if both are 1: