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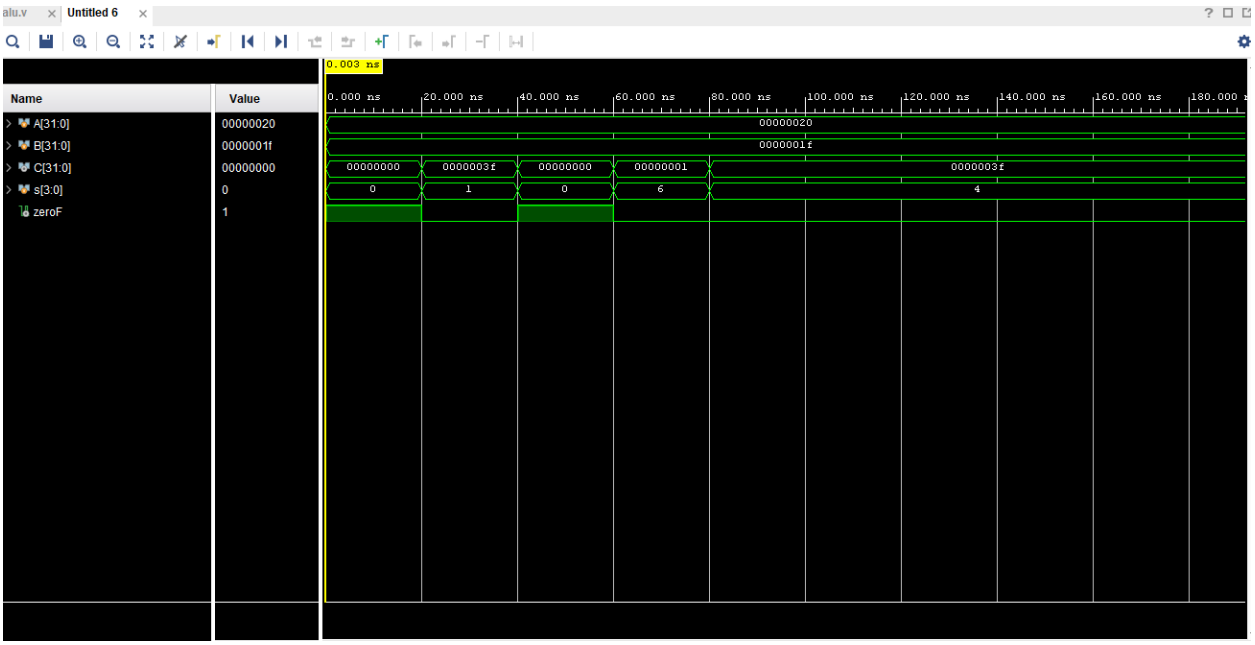
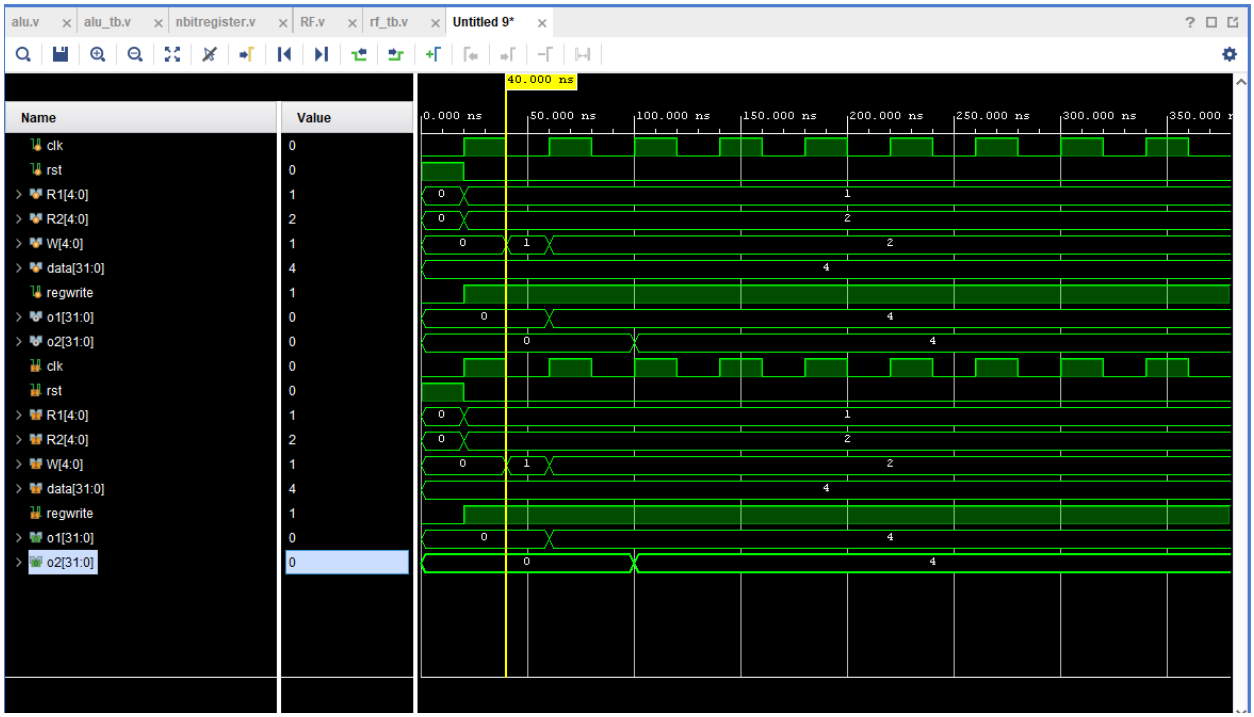
Lab # 4 Report

Summary:

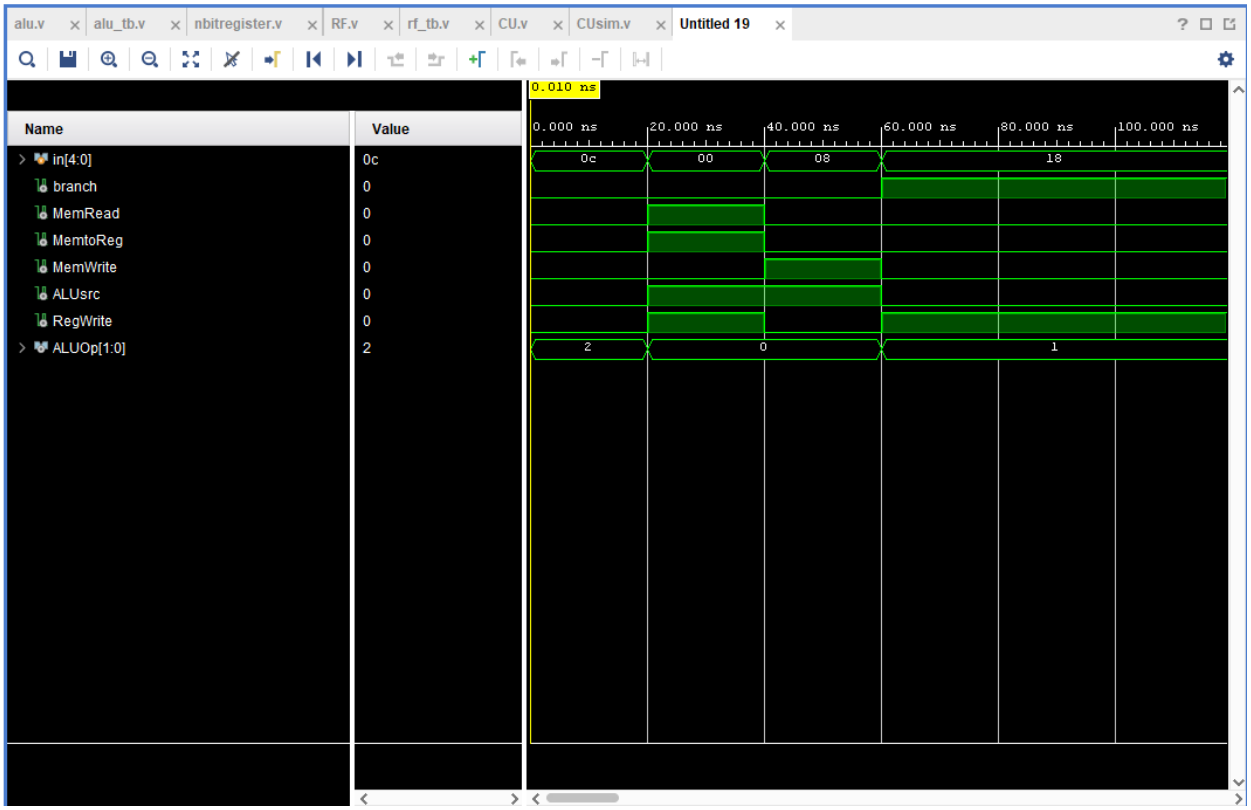
1. Expriment # 1: In this experiment, we implemented an ALU with zero flag that takes two 32 bit numbers and performs operations on them. The ALU can perform different operations based on the value of the 4 bit Selection bits. The ALU can perform Addition, subtraction, bitwise OR and bitwise AND. We tested this by trying out the different operations on the same inputs and verifying that the output is correct.



2. Experiment # 2: In this experiment, we implemented the register file module with reset. We reused the N bit register module we implemented in lab # 3 to generate 32 registers in a generate for loop. We set N=32 for all of them (in RegisterFile module) and passed the reset signal to them, the same way we did for the past lab. We simulated by setting all registers to 0, reading register 1 and 2, and writing to them one by one and see how they have updated



3. Experiment # 3: In this experiment we implemented the control unit that determines the different select lines. We tested by passing it the different formats and seeing the output of each select line.



4. Experiment # 4: In this experiment, we implemented the ALU control unit which produces the selection line for the ALU to determine the operation to be performed. We simulated by testing the output of the selection lines.