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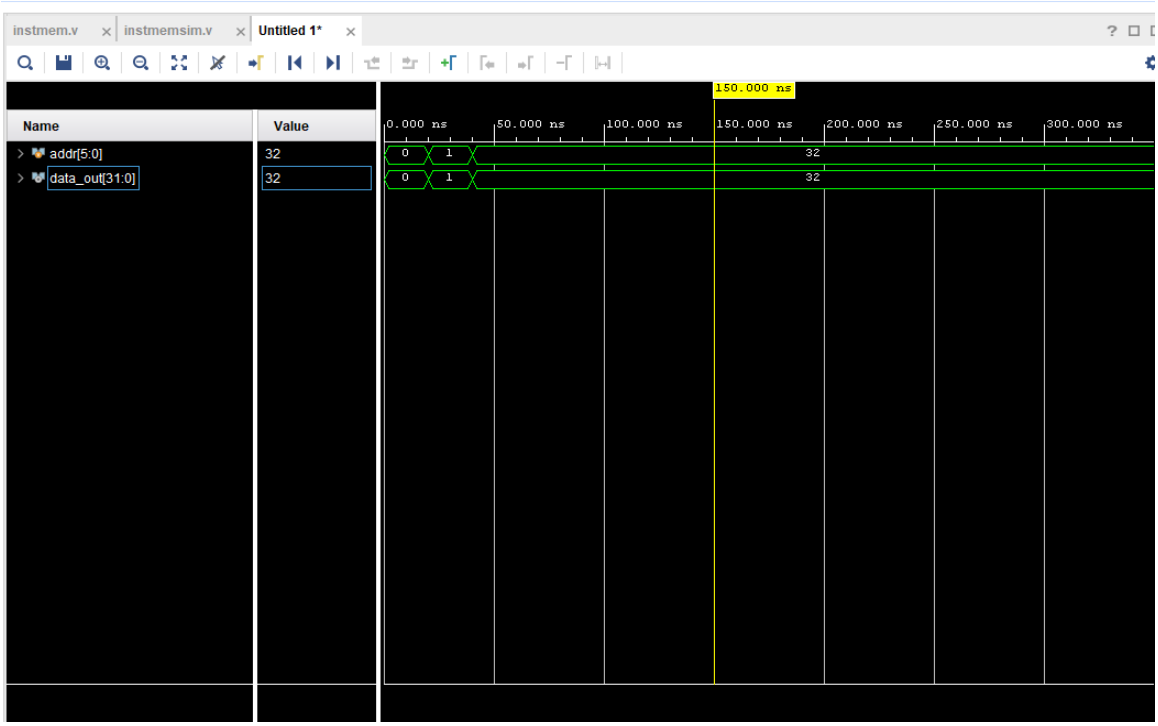
Lab # 5 Report

Summary:

1. Expriment # 1: In this experiment we implemented the memory modelling module which will represent the RAM available to our processor. We will only be using a memory module with 64 word capacity due to the limited resources we have on the fpga. The module takes the address from pc, discards 2 LSBs and that's the address of the word we want to load. We output the word stored at that address. This is essentially a ROM, so we intialized it with some values to test it in our testbench. We loaded 0, 1 and 32 at addresses 0, 1, 32 respectively and displayed them.



2. Experiment # 2: For this experiment we implemented a word addressable data memory that can store up to 64 words. Again, we have to divide the address by 4. We also take in the new data to be written. It also takes in a clock input, memread and memwrite from the Control unit. data reading is asynchronous while writing is synchronous. We simulated it in the testbench as follows. We first store value 9 at address 20, this gets done with the rising edge of the clock, We then write 9 to memory address 30 and then write 30 to memory address 30.