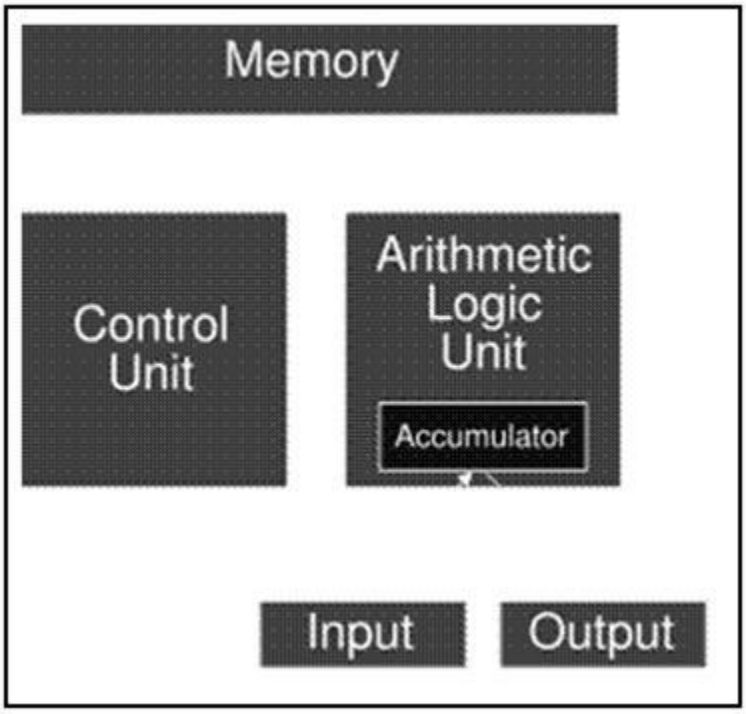
Design of Arithmetic Logic Unit

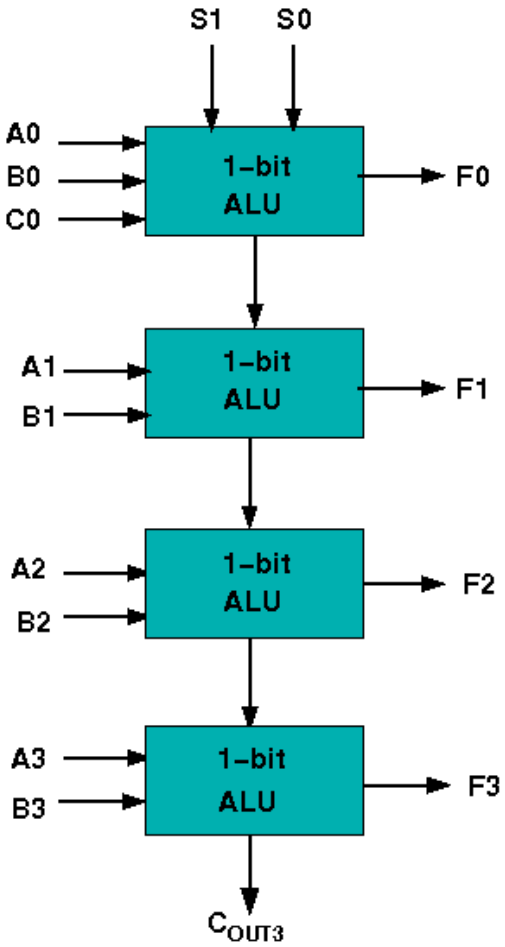
- ✓ **Introduction to Arithmetic Logic Unit**

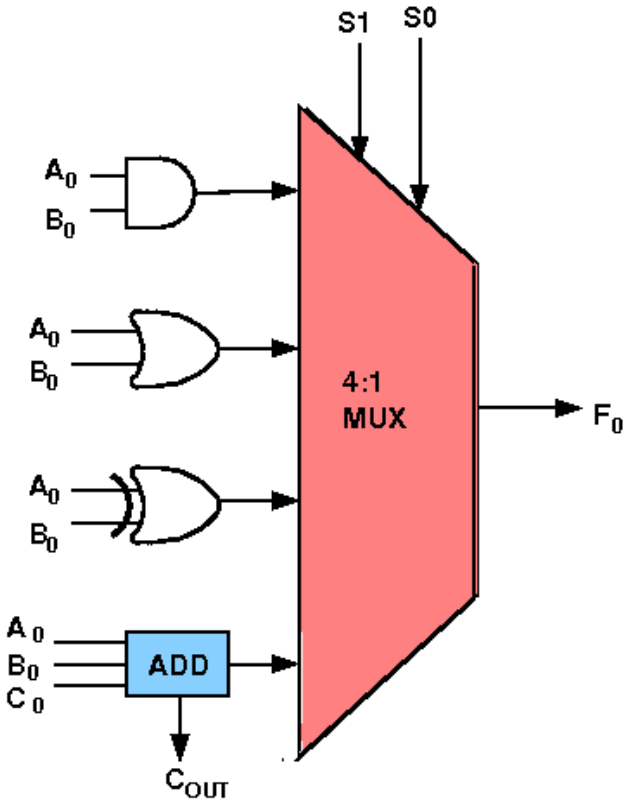
In ECL, TTL and CMOS, there are available integrated packages which are referred to as arithmetic logic units (ALU). The logic circuitry in this units is entirely combinational (i.e. consists of gates with no feedback and no flip-flops).The ALU is an extremely versatile and useful device since, it makes available, in single package, facility for performing many different logical and arithmetic operations. Arithmetic Logic Unit (ALU) is a critical component of a microprocessor and is the core component of central processing unit.



- ✓ **Design of ALU**

ALU or Arithmetic Logical Unit is a digital circuit to do arithmetic operations like addition, subtraction, division, multiplication and logical operations like and, or, xor, nand, nor etc. A simple block diagram of a 4 bit ALU for operations and, or, xor and Add is shown here





✓ **Design Issues**

The circuit functionality of a 1 bit ALU is shown here, depending upon the control signal S1 and S0 the circuit operates as follows:

- for Control signal S1 = 0 , S0 = 0, the output is A And B,
- for Control signal S1 = 0 , S0 = 1, the output is A Or B,
- for Control signal S1 = 1 , S0 = 0, the output is A Xor B,
- for Control signal S1 = 1 , S0 = 1, the output is A Add B.

✓ **Assignment Statements**

1. Design a 4 bit ALU comprising only the AND, OR, XOR and Add operations.
2. Design a 4-bit ALU with capabilities similar to 74181

S3	S2	S1	S0	F(M=L)	F(M=H)	
					Cn=L	Cn=H
L	L	L	L	A′	A Plus 1	A minus 1
L	L	L	H	A′+B′	(A+B) plus 1	(A+B) minus 1
L	L	H	L	A′B	(A+B′) plus 1	(A+B′) minus 1
L	L	H	H	0	1	-1
L	H	L	L	(AB)′	A plus AB′	A minus AB′
L	H	L	H	B′	(A + B) plus AB'	(A + B) minus AB'
L	H	H	L	A⊕B	A plus B plus 1	A minus B minus 1
L	H	H	H	AB'	AB plus 1	AB minus 1
H	L	L	L	A'+B	A plus AB	A minus AB
H	L	L	H	(A⊕B)′	A plus B	A minus B
H	L	H	L	B	(A + B') plus AB	(A + B') minus AB
H	L	H	H	AB	AB plus 1	AB minus 1
H	H	L	L	1	A plus A	A minus A
H	H	L	H	A+B'	(A + B) plus A	(A + B) minus A
H	H	H	L	A+B	(A + B') plus A	(A + B') minus A
H	H	H	H	A	A multiply B	A multiply B