Combinational Circuit Design Using Verilog HDL

Objectives

1. Understanding the internal structure of the general FPGAs.
2. Understanding how to write a behavioral description of combinational circuits.
3. Understanding how to write a test bench code to verify the functionality of your Verilog code.
4. Understanding how to implement and test your code on FPGA board.

Introduction

The internal structure of a general FPGA device is shown in Fig. 1. FPGA contains a two dimensional arrays of logic blocks and interconnections between logic blocks. Both the logic blocks and interconnects are programmable. Logic blocks are programmed to implement a desired function and the interconnects are programmed using the switch boxes to connect the logic blocks.

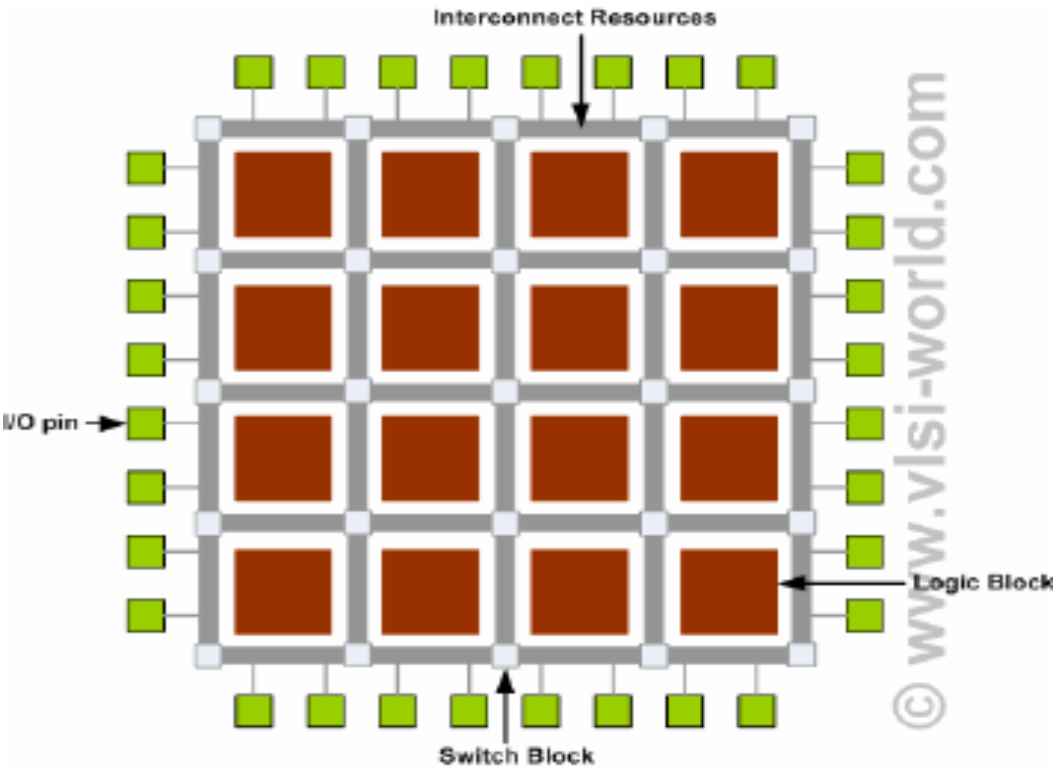

Fig. 1: Conventional structure of FPGA device.

Tools:-

1. Xilinx ISE program.
2. Vertex 5 FPGA kit.
3. User constraint file ".UCF".
4. J-tag cable.
5. PC.

Experiments:-

1) Problem1: Design 4-bit Priority Encoder

Follow the coming steps to design the 4-bit priority encoder, which its operation is shown in Table. 1.

- Write a Verilog code to describe behavior in Table. 1.
- Verify the design functionality.
- Implement the design on the FPGA kit.

Table 1: The functionality of the priority encoder.

Input	Output
1---	100
01--	010
001-	011
0001	001
0000	000

2) Problem2: Design priority decoder with enable

Follow the coming steps to design the required decoder, which its operation is shown in Table. 2.

- Write a Verilog code to describe the behavior in Table. 2.
- Verify the design functionality.
- Implement the design on FPGA Kit.

Table 2: The function table of the required decoder.

Enable	Input	Output
0	--	0000
1	00	0001
1	01	0010
1	10	0100
1	11	1000

3) Problem3: Design ALU circuit

Follow the coming steps to design the required decoder, which its operation is shown in Table. 3.

- Write a Verilog code to describe the behavior in Table. 3.

- Verify the design functionality.
- Implement the design on FPGA Kit.

Table 3: The function table of the ALU circuit.

Control	Instruction	Operation
000	Add	A + B + cin;
001	Sub	A + B - cin;
010	Or	A or B
011	And	A and B
100	Shl	A(2 down to 0) & ‘0’
101	Shr	‘0’ & A(3 down to 1)
110	Rol	A(2 down to 0) & A(3)
111	Ror	A(0) & A(3 down to 1)

4) Problem6: BCD Incrementor

The binary-coded-decimal (BCD) format uses 4 bits to represent 10 decimal digits. For example, 259_{10} is represented as "0010 0101 1001" in BCD format. A BCD Incrementor adds 1 to a number in BCD format. For example, after incrementing, "0010 0101 1001" (i.e., 25910) becomes "0010 0110 0000" (i.e., 26010).

- Design a three-digit 12-bit incrementor and derive the code.
- Derive a test bench and use simulation to verify operation of the code.
- Synthesize the circuit, program the FPGA, and verify its operation.