**Machine Learning**

***Definitions***

* **Artificial Intelligence** A branch of Computer Science that aims to enable machines to *behave and think like humans*.
* **Machine Learning** A branch of Artificial Intelligence that aims to enable machines to *simulate human learning*.
* **Cross Validation** A model evaluation technique where the data set is divided into *k* partitions, the model is then trained on each of these partitions.
* **Linear regression** One of the Machine Learning algorithms. It is a statistical method that is used for *predictive analysis*.

***Model Evaluation Techniques***

* Mean Absolute Error (MAE)
* Root Mean Square Error (RMSE)
* Coefficient of determination or R2
* Adjusted R2

***Machine Learning Cycle***

1. Data Gathering
2. Data Preparation
3. Data Wrangling
4. Data Analysis
5. Model Training
6. Model Testing and Validatio
7. Deployment

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**FPGA**

**Ch1**

***Classification of Device Technologies***

* Discrete logic
* Programmable devices (FPGAs)
* ASIC (Application specific IC)

***System Representation***

* Behavioral level
* Structural level
* Physical level

***System Abstraction Levels***

* Transistor level
* Gate level
* Register transfer level (RTL)
* Processor Level

***FPGA Definition***

An array of gates in addition to some other elements such as memory controllers and communication interfaces that can be programmed and reconfigured more than once.

***FPGA Applications***

Cryptography, ASIC prototyping, Industrial, medical and Scientific Instruments, Audio/Video and Image processing and broadcasting, high-performance computing, AI, and Deep Learning, Military and Space applications, Networking, packet processing, and other communications

***FPGA Design Flow***

1. **Architecture design** involves the analysis of the project requirements, problem decomposition.
2. **HDL design entry** using HDLs to describe the design.
3. **Test environment design** writing test environments and behavioral models to ensure the correctness of the HDL description.
4. **Behavioral simulation** comparing the HDL outputs and the behavioral model to ensure the correctness of the HDL description
5. **Synthesis** involves the conversion of an HDL description to a netlist
6. **Implementation** a synthesizer-generated netlist is mapped onto particular device's internal structure
7. **Timing analysis** to ensure the implemented design satisfies the timing constraints

**Ch3**

***Unfamiliar Verilog Operators***

* Exponentiation: \*\*
* Concatenation: {}{} → {2'b01}{2'b10} yields 4'b0110
* Replication: {{}} → {3{2'b01}} yields 6'b010101

***Coding Styles***

* Structural modeling: gate level → and(x, a, b);
* Dataflow modeling: C-style assignments → assign z = x && !y;
* Behavioral modeling: initial and always blocks →

      always @ (x or y)

        begin

          z=0;

          if (x ==y)

          z=1;

        end