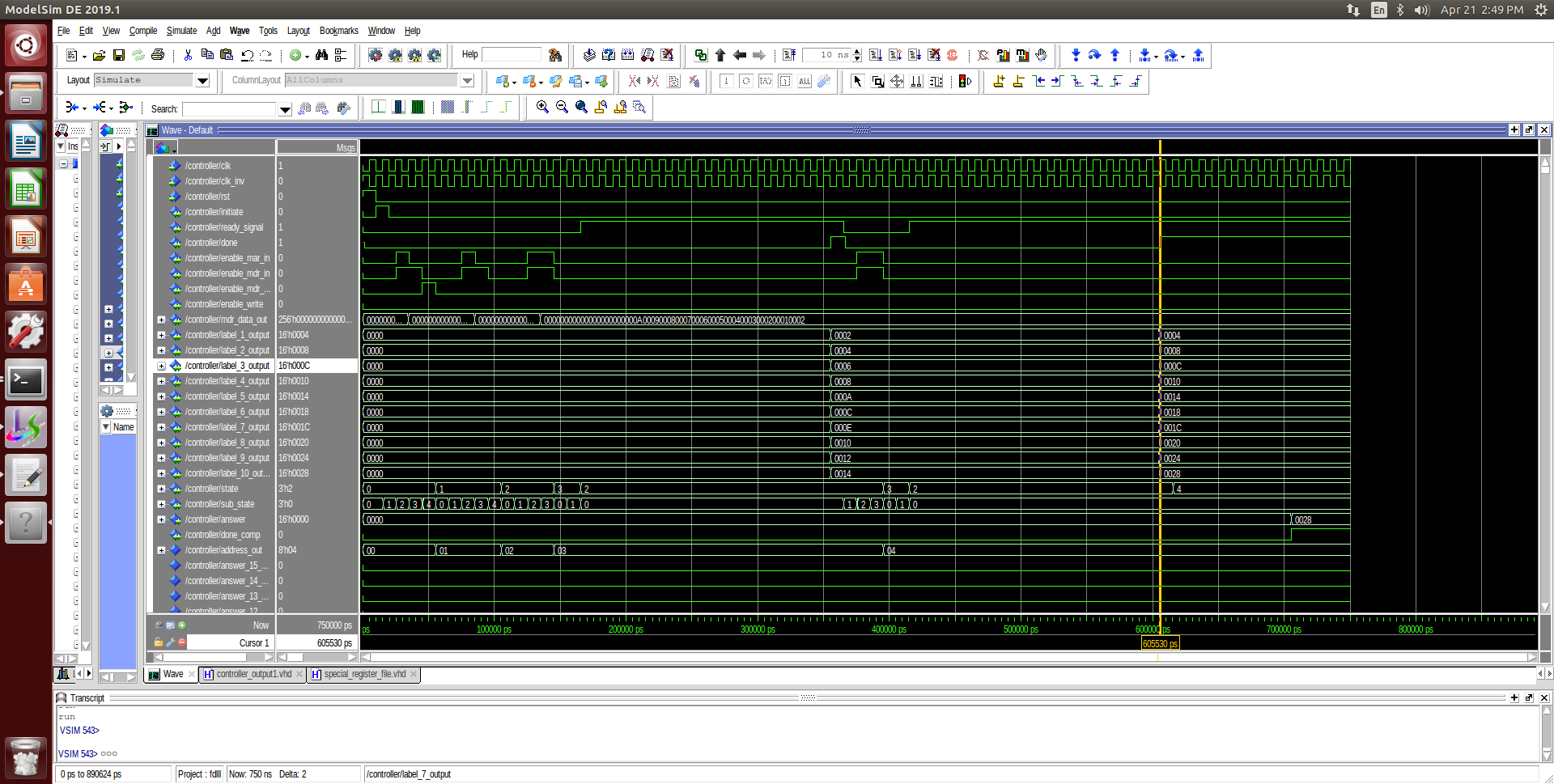
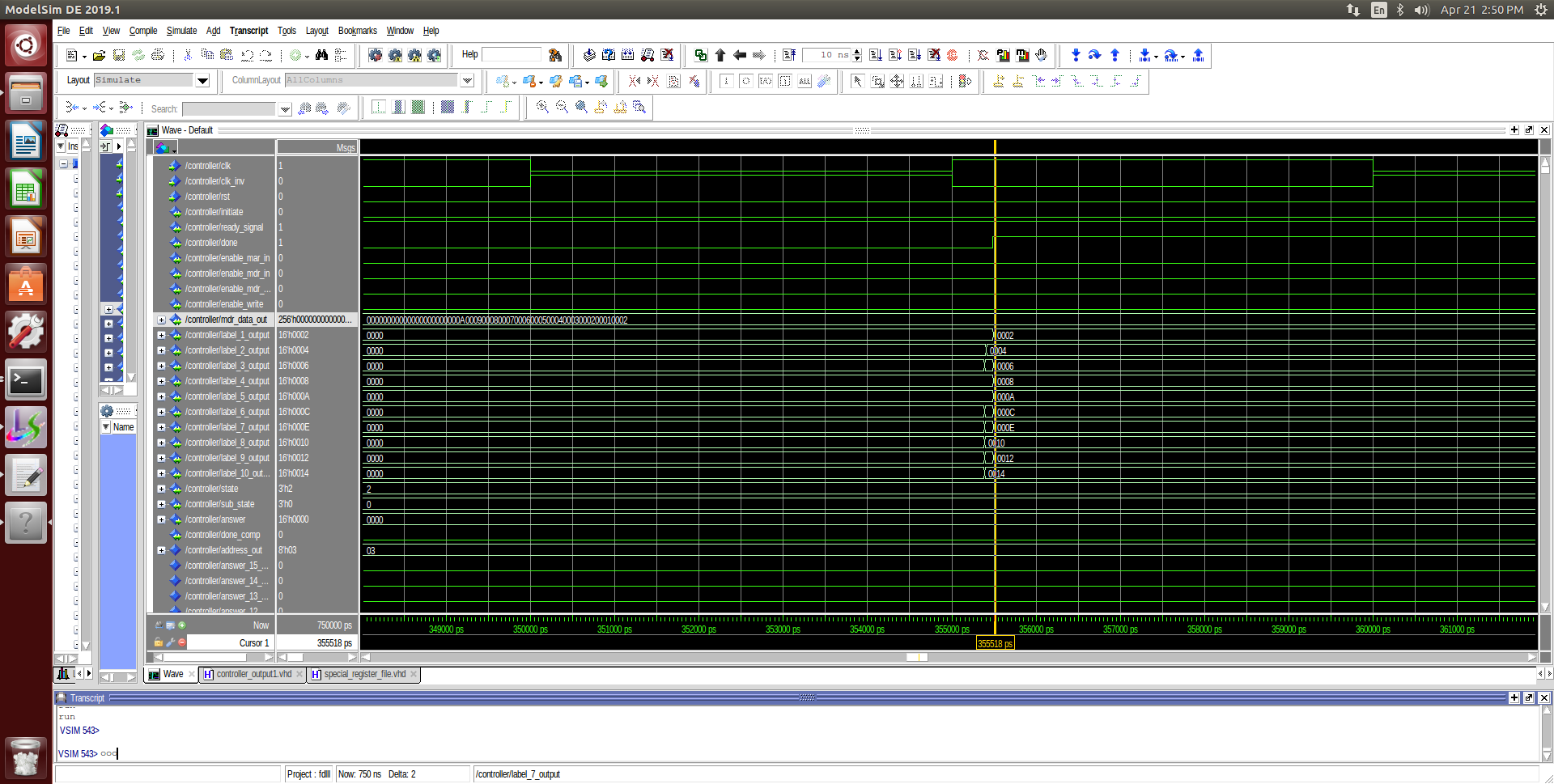
**VLSI Document**

* **Entity Description**

|  |  |
| --- | --- |
| **Twos\_complement** | Gets twos complement of the input. |
| **Compare\_add\_sub** | One step of booth algorithm. |
| **Shift Reg** | Initialization and stopping of booth ( states ). |
| **Booth\_Integration** | Perform multiplication using the previous components. |
| **Booth Adder Comp** | 10x **Booth\_Integration** and accumulation |
| **Shift\_Reg\_Integration** | Stops accumulation and raise done signal. |
| **Label\_Reg\_File** | File Containing all labels (10 labels Register). |
| **Specital\_Reg\_File** | File Dealing with **RAM**. It has **MAR**, **MDR**. |
| **Comparator** | Component uses the **ALU** to return the bigger input. |
| **Maximum\_IC** | Uses **5** **Comparators** to get the maximum label in 9 cycles. |
| **Counter\_Controller** | Contains the state machine. |

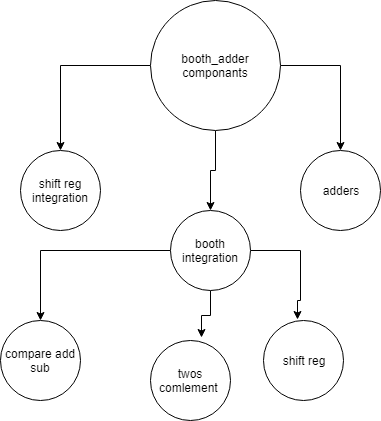
* **Timing Diagrams**



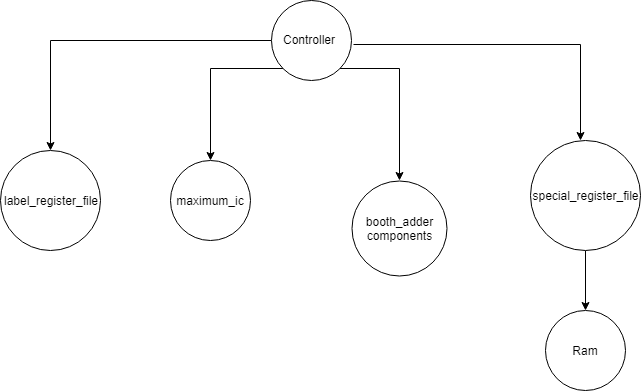


**File Tree**

* **Multiplication**



* **State Machine**

****

* **I/O Ports (Controller)**

|  |  |
| --- | --- |
| **Clk** | Global |
| **Clk\_Inv** | Global |
| **Rst** | Global |
| **Initiate** | Signal from previous module |
| **Ready\_Signal** | Ready for Begin multiplication |
| **Done** | Booth Done |
| **Done\_comp** | Maximum\_IC done |
| **Label1 – Label10** | Labels to booth part |
| **Answer** | Final Answer |

* **Design flow Reports**

**data required time 9.53**

**data arrival time 7.1**

**slack 2.37**

**Number of gates: 14251**

**Clk 10 ns**