project 2

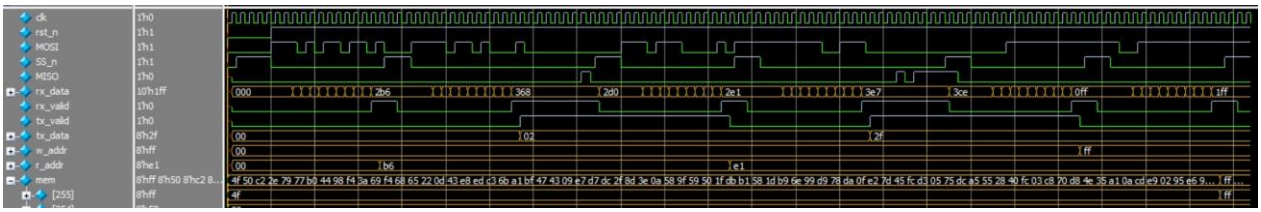
SPI Slave with Single Port RAM

By team: Chipions league

BY:

- **moataz ballah Mohsen**
- **Ashraf sherif**

waveforms captured from QuestaSim:



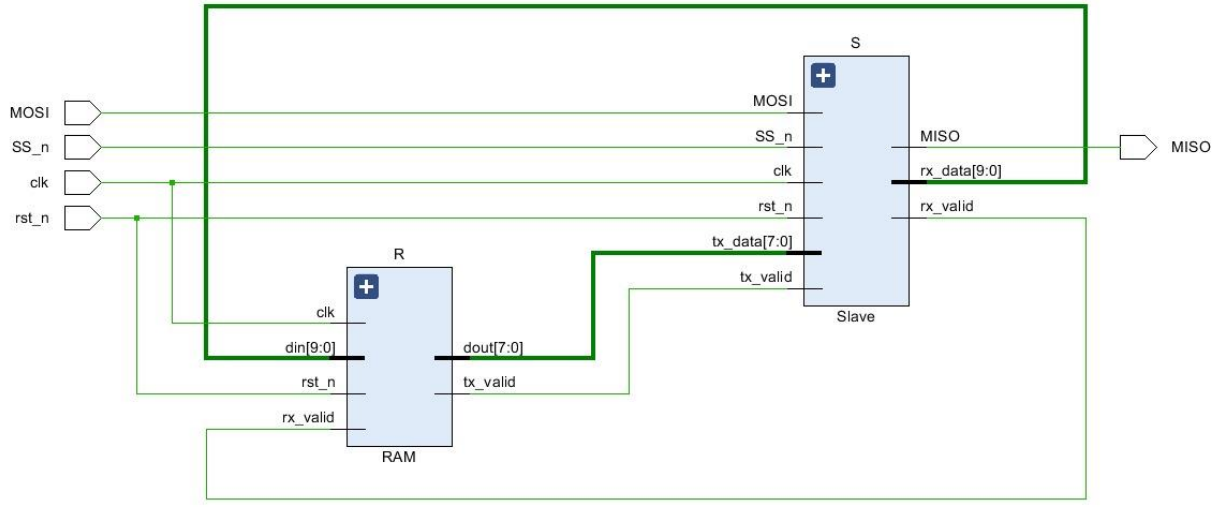
-from write a write of ff address with value of ff also to make it easy to see the write on mem.

Snippet from QuestaLint showing no errors:

Severity	Status	Check	Alias	Message
		seq_block_has_duplicate...		Signal is assigned more than once in a sequential block. Signal rx_valid, Module Slave, File C:/Users/mostafa/Desktop/SPI/SPI_SLAVE.v, Total Assigns Count 3,
		multi_ports_in_single_line		Multiple ports are declared in one line. Module RAM, File C:/Users/mostafa/Desktop/SPI/RAM.v, Line 5.
		multi_ports_in_single_line		Multiple ports are declared in one line. Module Slave, File C:/Users/mostafa/Desktop/SPI/SPI_SLAVE.v, Line 3.
		multi_ports_in_single_line		Multiple ports are declared in one line. Module WRAPPER, File C:/Users/mostafa/Desktop/SPI/SPI_WRAPPER.v, Line 2.

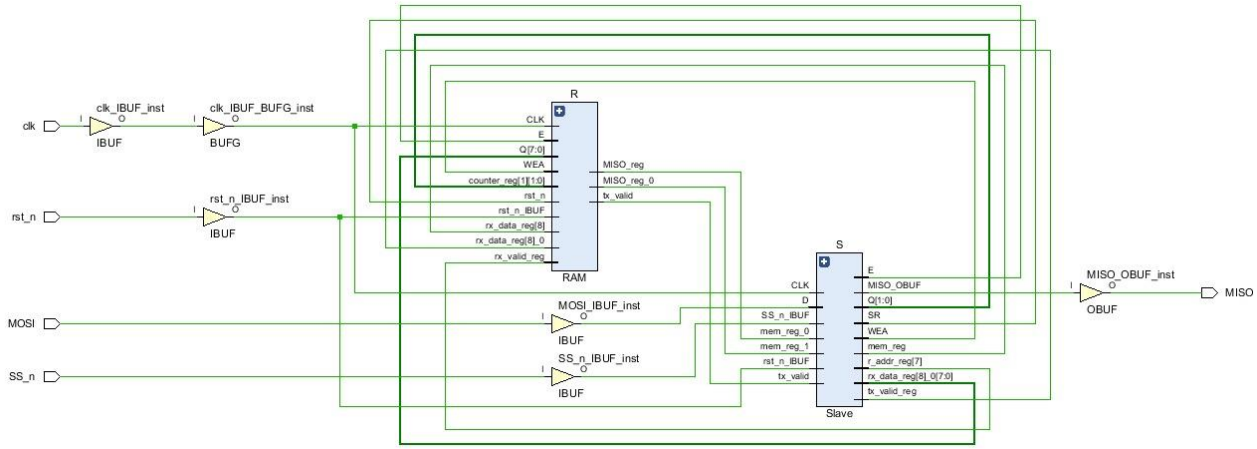
First gray encode:

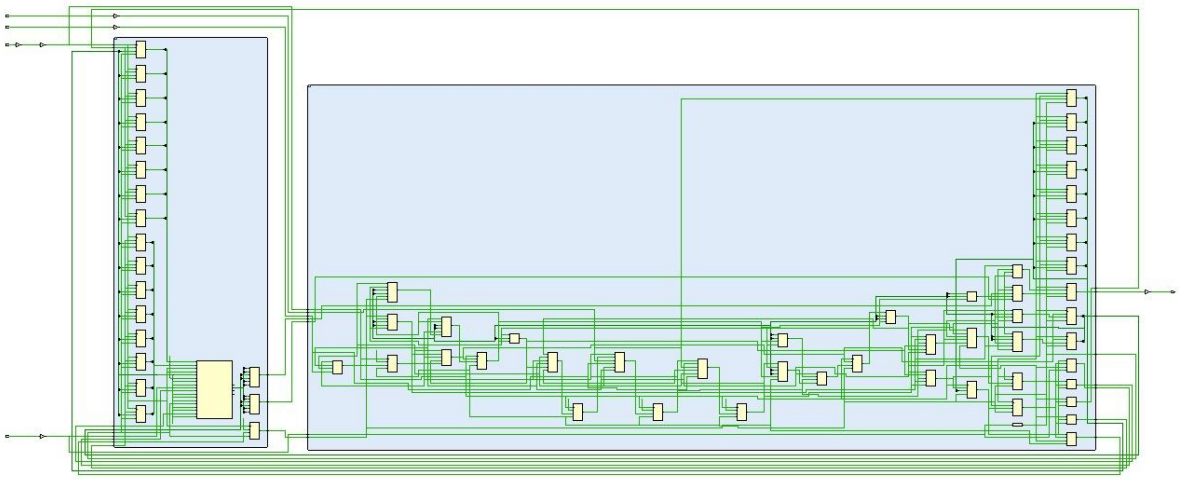
Elaboration:




Tcl Console
Messages
Log
Reports
Design Runs
Info (15)
Status (11)
Show All
[Synth 8-6157] synthesizing module 'WRAPPER' [SPI_WRAPPER.v:1] (2 more like this)
[Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI_SLAVE.v:20]
[Synth 8-155] case statement is not full and has no default [SPI_SLAVE.v:76]
[Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
[Device 21-403] Loading part xc7a35ticpg236-1L
[Project 1-570] Preparing netlist for logic optimization
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synthesis:


clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
rst_n
rst_n_IBUF_inst
IBUF
MOSI
MOSI_IBUF_inst
IBUF
SS_n
SS_n_IBUF_inst
IBUF
R
RAM
S
Slave
MISO_OBUF_inst
OBUF
MISO



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.445 ns	Worst Hold Slack (WHS):	0.144 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	40

All user specified timing constraints are met.

Hierarchy

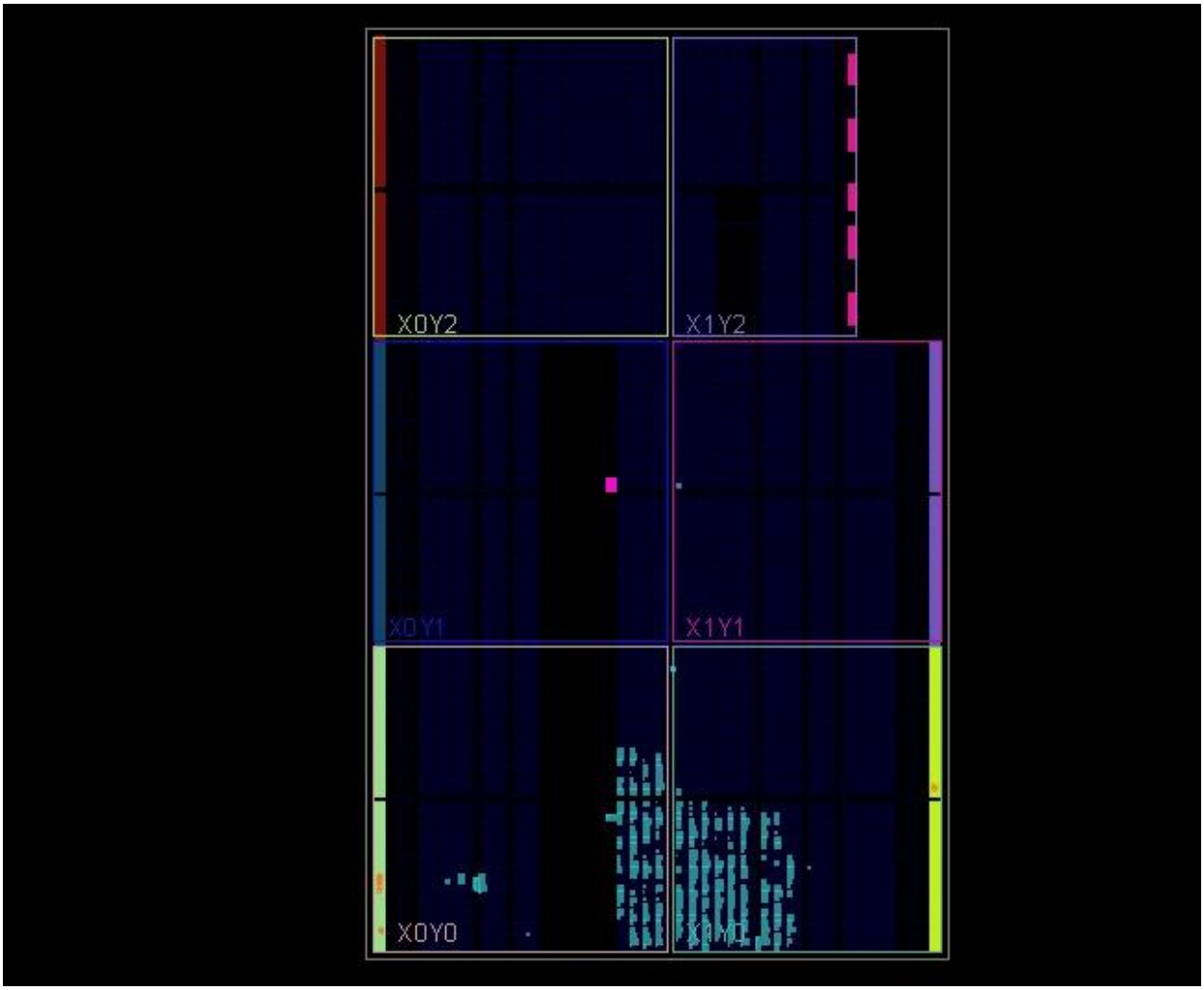
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER	26	37	0.5	5	1
R (RAM)	2	17	0.5	0	0
S (Slave)	24	20	0	0	0

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug

Warning (1) Info (43) Status (19) Show All

[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
[Timing 38-35] Done setting XDC timing constraints.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

Implementation:

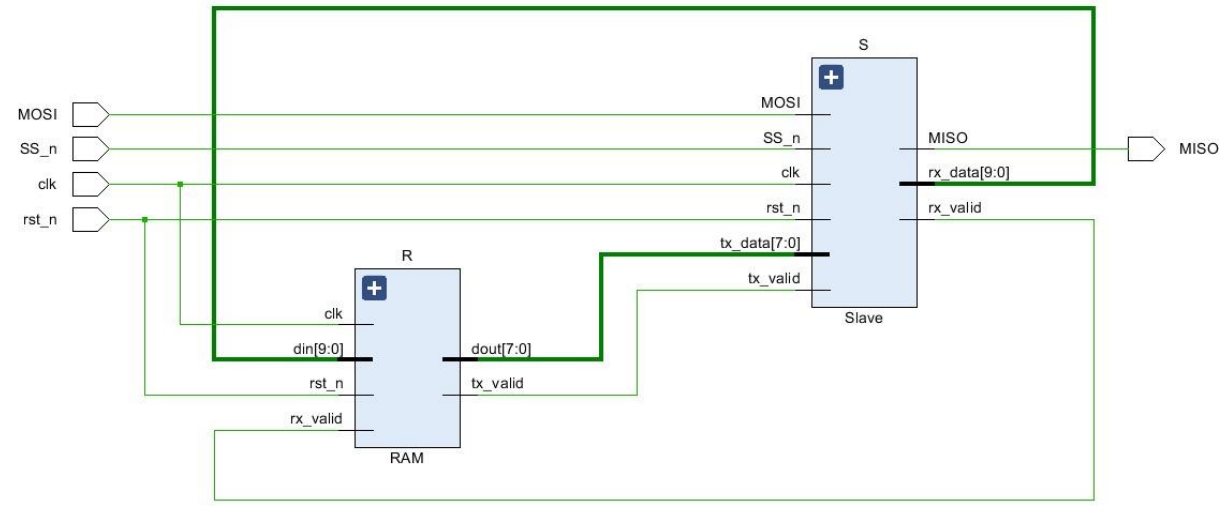


One hot :

Elaboration:

- Elaborated Design (11 infos, 7 status messages)
  - General Messages (11 infos, 7 status messages)
    - [Synth 8-6157] synthesizing module 'WRAPPER' [SPI_WRAPPER.v:1] (2 more like this)
    - [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_SLAVE.v:20]
    - [Synth 8-155] case statement is not full and has no default [SPI_SLAVE.v:76]
    - [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
    - [Project 1-570] Preparing netlist for logic optimization
    - Processing XDC Constraints (6 more like this)
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

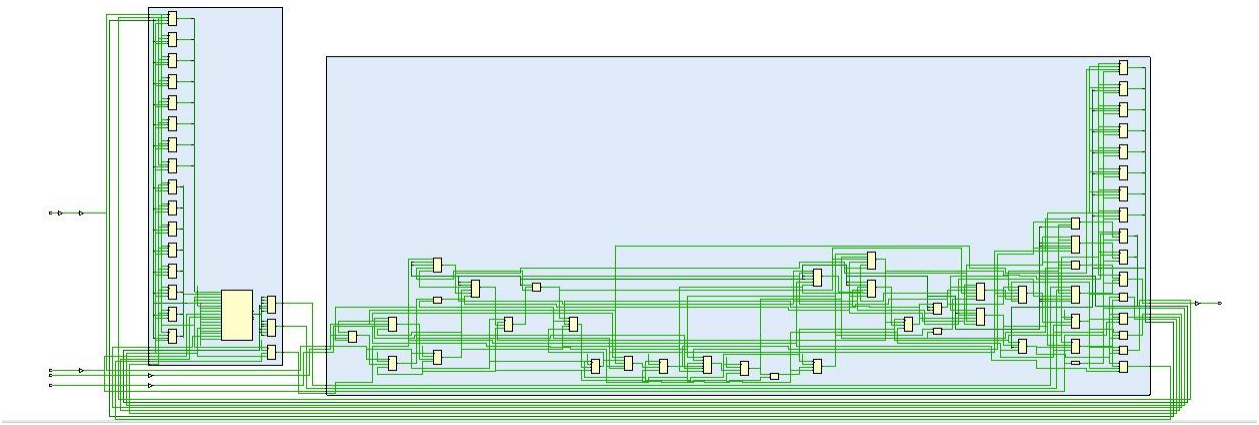
```
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                              000
                 CHK_CMD |                            00010 |                              001
                   WRITE |                            00100 |                              100
                READ_ADD |                            01000 |                              010
               READ_DATA |                            10000 |                              011
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'Slave'
```



Synthesis:

Synthesis (1 warning, 31 infos, 11 status messages)

- Command: synth_design -top WRAPPER -part xc7a35ticpg236-1L (10 more like this)
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- [Synth 8-6157] synthesizing module 'WRAPPER' [SPI_WRAPPER.v:1] (2 more like this)
- [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_SLAVE.v:20]
- [Synth 8-155] case statement is not full and has no default [SPI_SLAVE.v:76]
- [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/lenovo/Desktop/spi/basys_spi.xdc]. Th
  xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with th
- [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'Slave'
- [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
- [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'Slave'
- [Synth 8-4480] The timing for the instance i_0/R/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output regist
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis



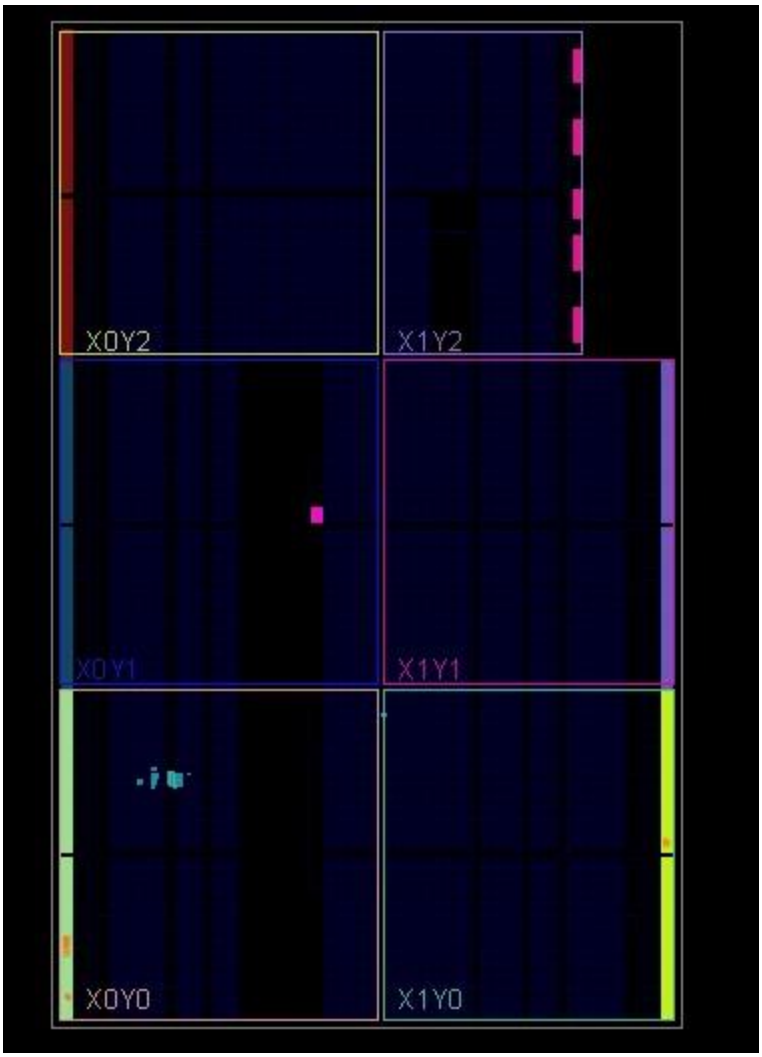
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.898 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	96	Total Number of Endpoints:	96	Total Number of Endpoints:	42

All user specified timing constraints are met.

Hierarchy

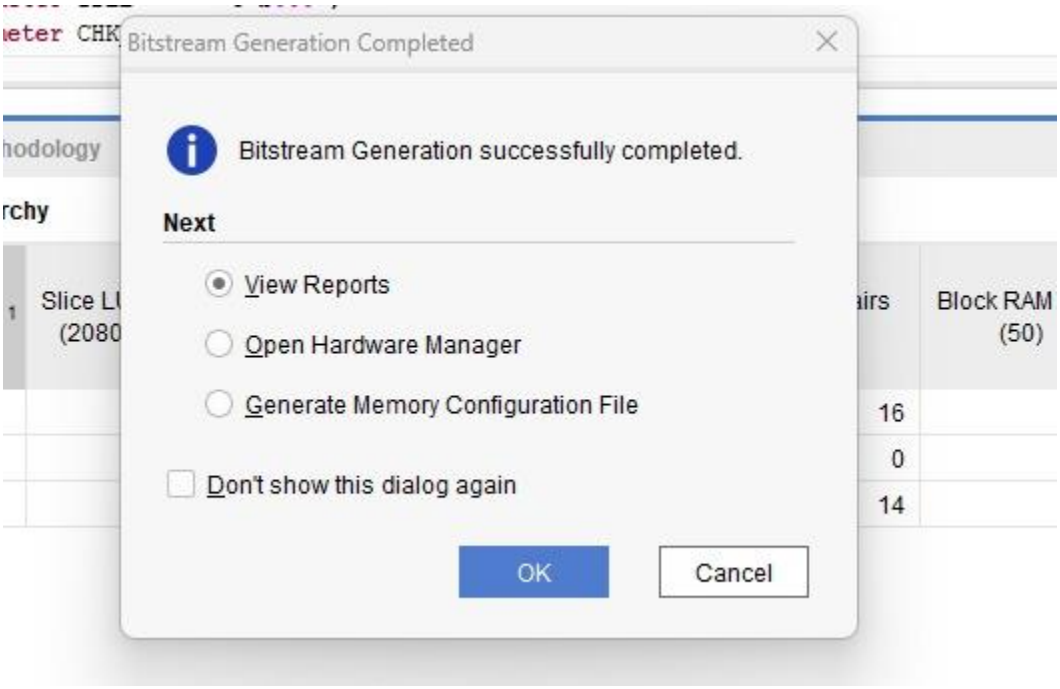
Name 1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER	28	39	0.5	5	1
R (RAM)	2	17	0.5	0	0
S (Slave)	26	22	0	0	0

sImplementation:



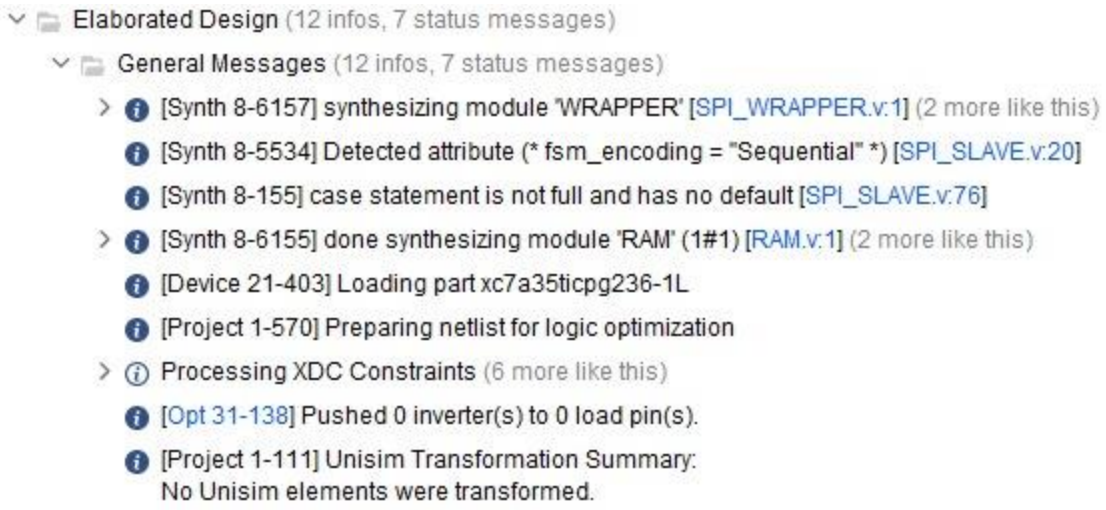
Hierarchy

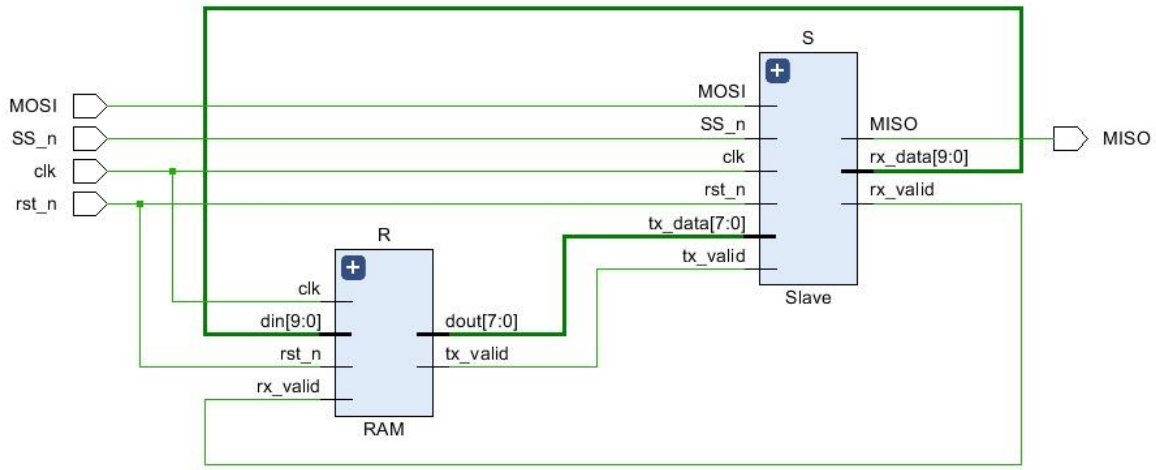
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N WRAPPER	29	39	13	29	16	0.5	5	1
R (RAM)	3	17	5	3	0	0.5	0	0
S (Slave)	26	22	10	26	14	0	0	0



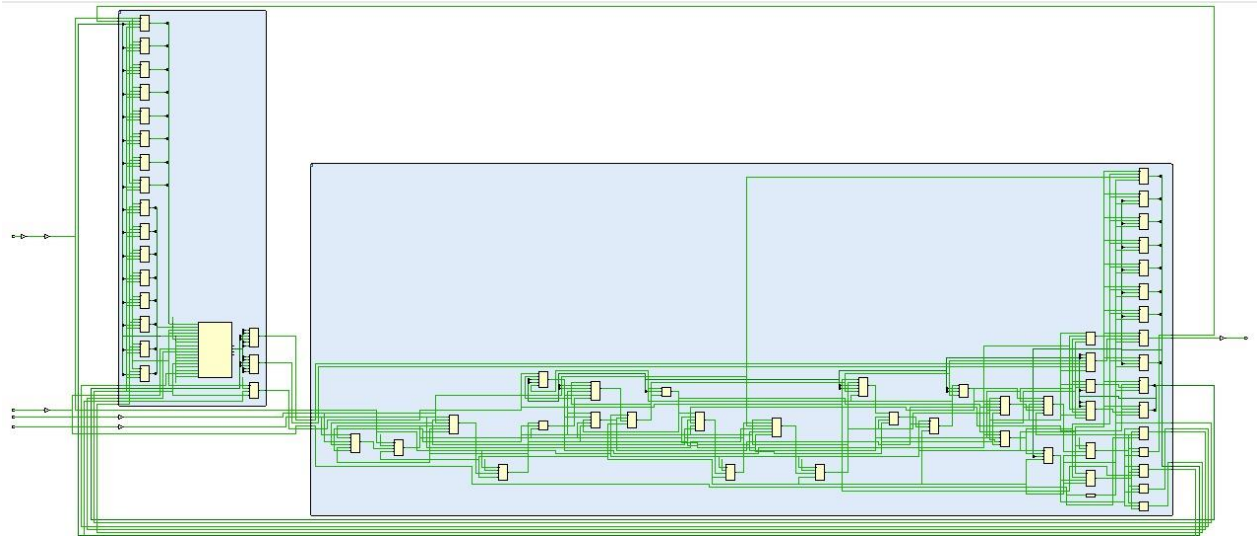
Last for sequential:

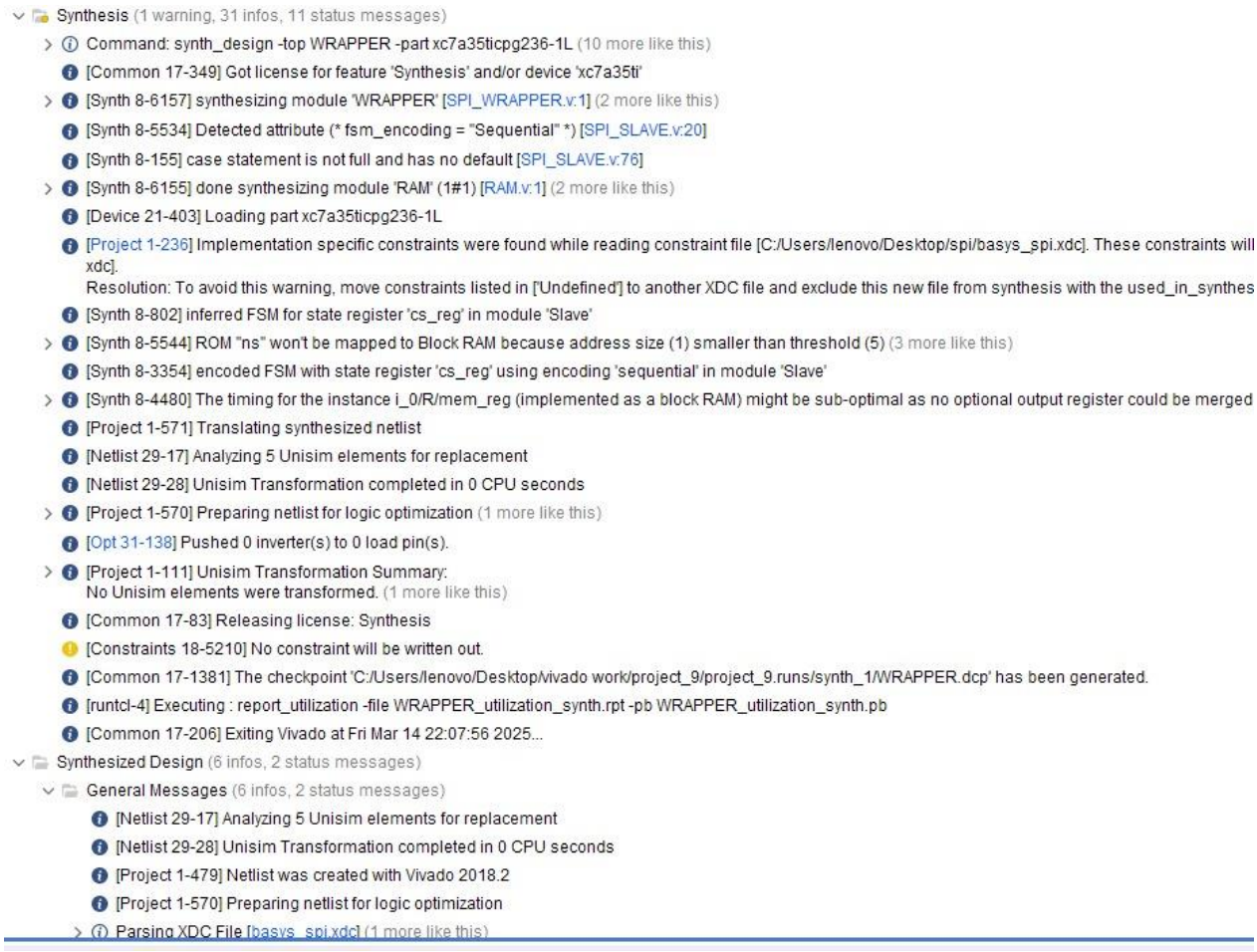
Elaboration:




S
MOSI
SS_n
clk
rst_n
MISO
rx_data[9:0]
rx_valid
tx_data[7:0]
tx_valid
Slave
MOSI
SS_n
clk
rst_n
MISO
R
clk
din[9:0]
rst_n
rx_valid
dout[7:0]
tx_valid
RAM

Synthesis:






```
92  ---------------------------------------------------------------------------------------------------
93  |                   State |                     New Encoding |               Previous Encoding
94  ---------------------------------------------------------------------------------------------------
95  |                    IDLE |                              000 |                              000
96  |                 CHK_CMD |                              001 |                              001
97  |                   WRITE |                              010 |                              100
98  |                READ_ADD |                              011 |                              010
99  |               READ_DATA |                              100 |                              011
100 ---------------------------------------------------------------------------------------------------
101 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'Slave'
```

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.898 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	40

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N WRAPPER	25	37	0.5	5	1
R (RAM)	2	17	0.5	0	0
S (Slave)	23	20	0	0	0

Implementation:

Warning (1) Info (239) Status (477) Hide All

- Implementation (98 infos, 228 status messages)
  - Design Initialization (11 infos, 7 status messages)
    - Command: open_checkpoint {C:/Users/lenovo/Desktop/vivado work/project_9/project_9.runs/impl_1/WRAPPER.dcp} (6 more like th
    - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - Opt Design (30 infos, 54 status messages)
    - Command: opt_design (53 more like this)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [Opt 31-49] Retargeted 0 cell(s).
    - [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
    - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    - [Pwropt 34-9] Applying IDT optimizations

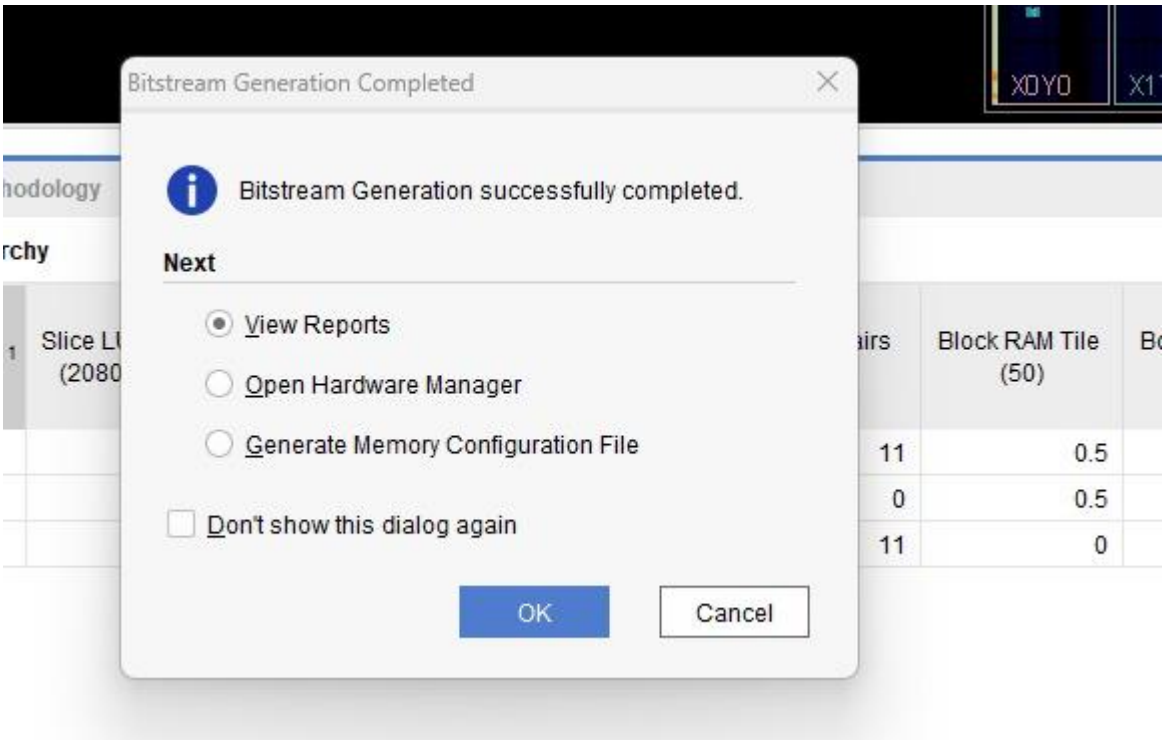
Design Timing Summary

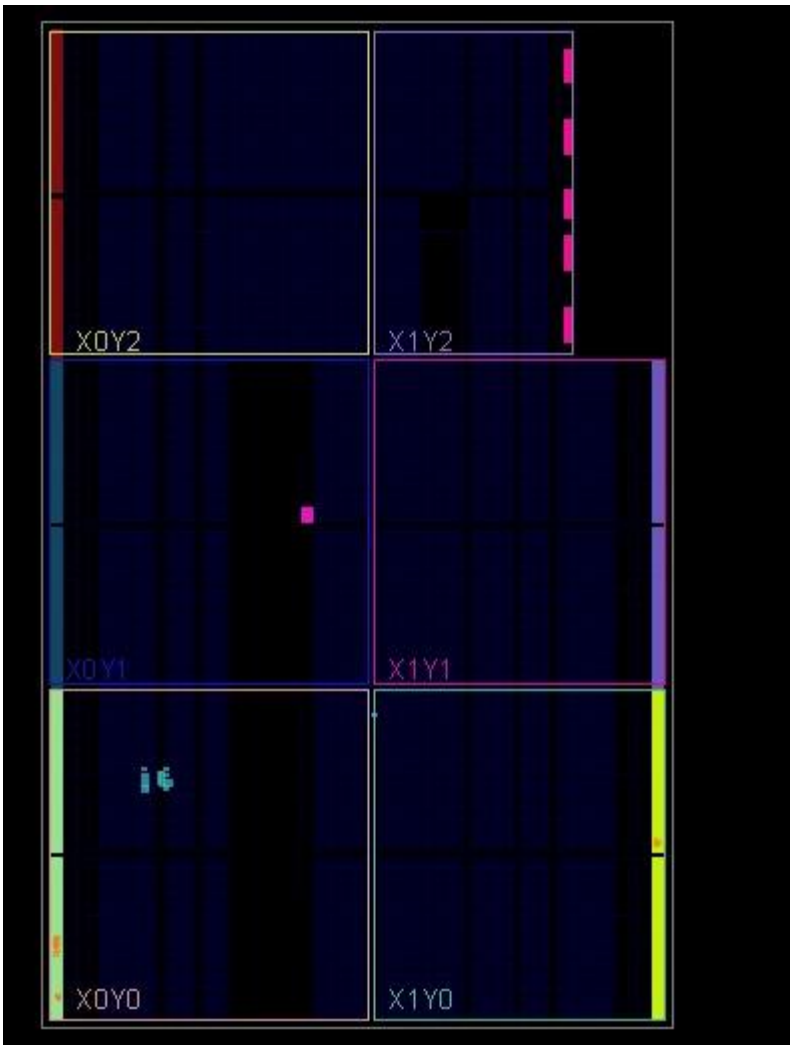
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.373 ns	Worst Hold Slack (WHS):	0.101 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	40

All user specified timing constraints are met.

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N WRAPPER	26	37	13	26	11	0.5	5	1
R (RAM)	3	17	6	3	0	0.5	0	0
S (Slave)	23	20	9	23	11	0	0	0




X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0