

project 2

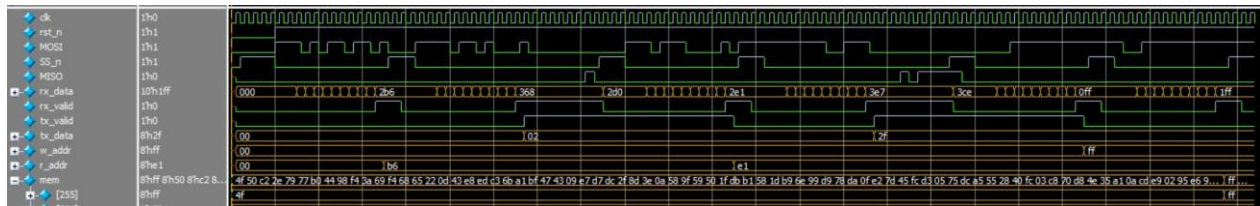
## SPI Slave with Single Port RAM

**By team: Chipions league**

**BY:**

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waveforms captured from QuestaSim:



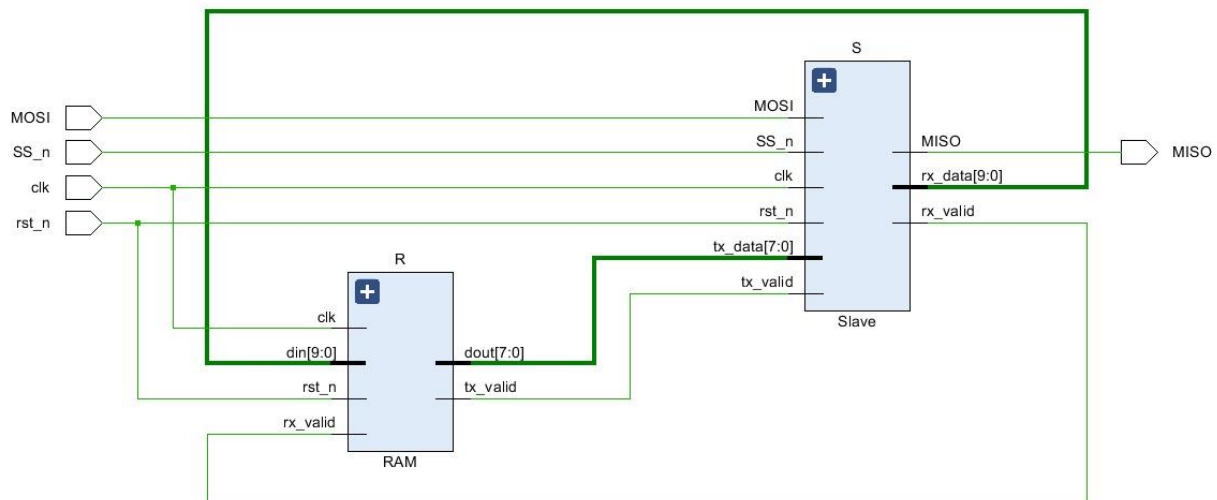
-from write a write of ff address with value of ff also to make it easy to see the write on mem.

Snippet from QuestaLint showing no errors:

Severity	Status	Check	Alias	Message
		seq_block_has_duplicate...		Signal is assigned more than once in a sequential block. Signal rx_valid, Module Slave, File C:/Users/mostafa/Desktop/SPI/SPI_SLAVE.v, Total Assigns Count 3.
		multi_ports_in_single_line		Multiple ports are declared in one line. Module RAM, File C:/Users/mostafa/Desktop/SPI/RAM.v, Line 5.
		multi_ports_in_single_line		Multiple ports are declared in one line. Module Slave, File C:/Users/mostafa/Desktop/SPI/SPI_SLAVE.v, Line 3.
		multi_ports_in_single_line		Multiple ports are declared in one line. Module WRAPPER, File C:/Users/mostafa/Desktop/SPI/SPI_WRAPPER.v, Line 2.

First gray encode:

Elaboration:





Design Timing Summary

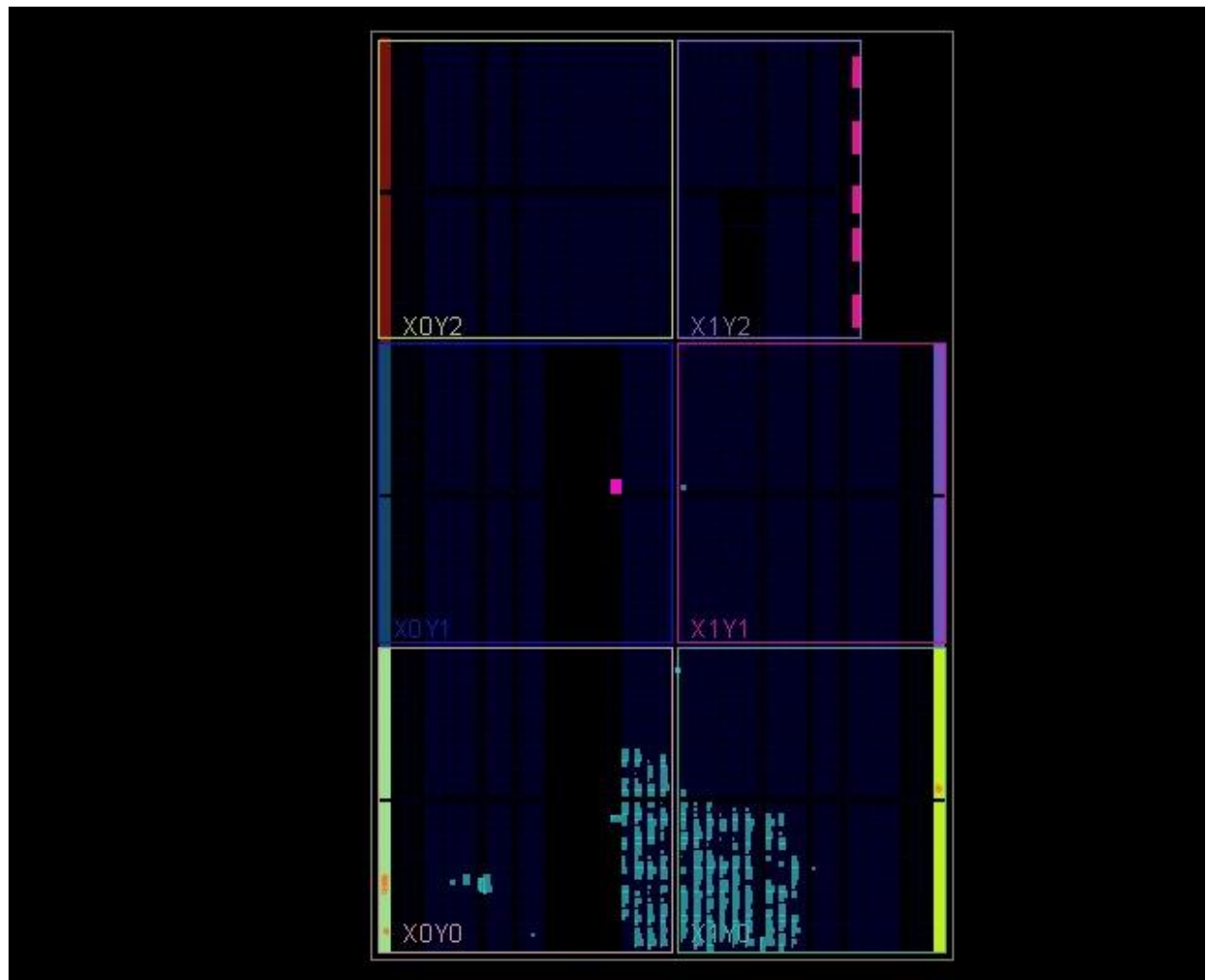
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.445 ns	Worst Hold Slack (WHS): 0.144 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 94	Total Number of Endpoints: 94	Total Number of Endpoints: 40

All user specified timing constraints are met.

Hierarchy					
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER	26	37	0.5	5	1
R (RAM)	2	17	0.5	0	0
S (Slave)	24	20	0	0	0

Tcl Console	Messages	Log	Reports	Design Runs	Timing	Debug
<div><div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div></div><div><div>Warning (1)</div><div>Info (43)</div><div>Status (19)</div></div><div>Show All</div></div><div><div>[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds</div><div>[Project 1-479] Netlist was created with Vivado 2018.2</div><div>[Project 1-570] Preparing netlist for logic optimization</div><div>[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).</div><div>[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.</div><div>[Timing 38-35] Done setting XDC timing constraints.</div><div>[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.</div><div>[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs</div></div></div>						

## Implementation:



One hot :

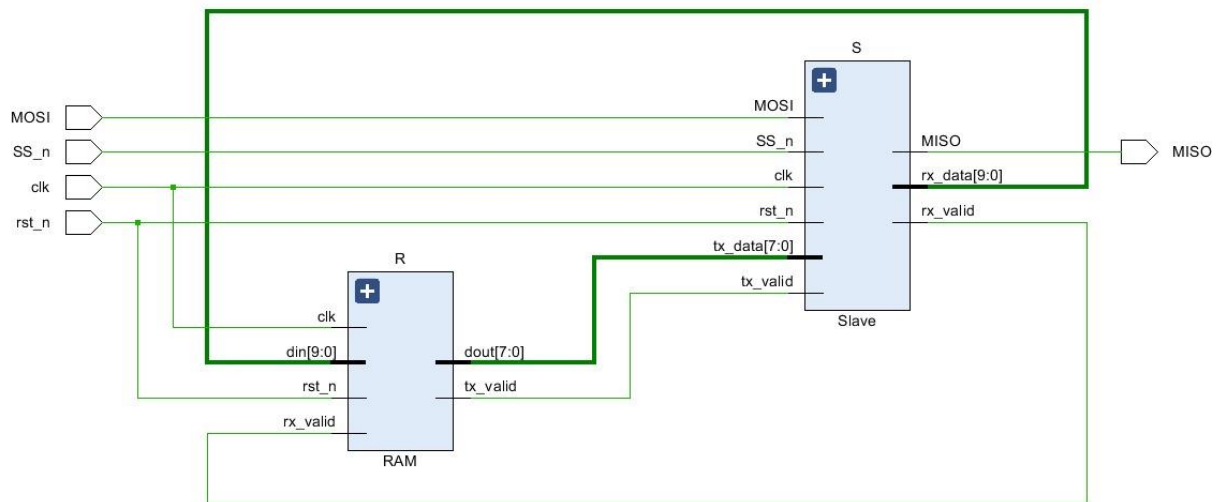
## Elaboration:

- ✓ Elaborated Design (11 infos, 7 status messages)
  - ✓ General Messages (11 infos, 7 status messages)
    - > [Synth 8-6157] synthesizing module 'WRAPPER' [SPI\_WRAPPER.v:1] (2 more like this)
      - [Synth 8-5534] Detected attribute (\* fsm\_encoding = "one\_hot" \*) [SPI\_SLAVE.v:20]
      - [Synth 8-155] case statement is not full and has no default [SPI\_SLAVE.v:76]
    - > [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
      - [Project 1-570] Preparing netlist for logic optimization
    - > Processing XDC Constraints (6 more like this)
      - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

```

92 |-----|
93 |           State |           New Encoding |           Previous Encoding
94 |-----|-----|-----|
95 |           IDLE |           00001 |           000
96 |          CHK_CMD |           00010 |           001
97 |           WRITE |           00100 |           100
98 |         READ_ADD |           01000 |           010
99 |         READ_DATA |           10000 |           011
100 |-----|-----|-----|
101 | INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'Slave'

```

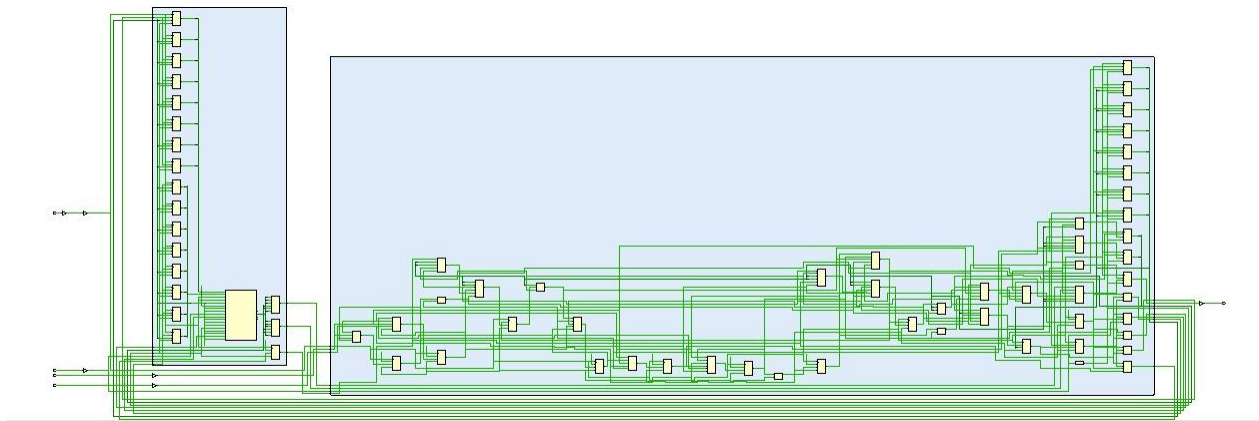


## Synthesis:

### ▼ Synthesis (1 warning, 31 infos, 11 status messages)

- > ⓘ Command: synth\_design -top WRAPPER -part xc7a35ticipg236-1L (10 more like this)
  - ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- > ⓘ [Synth 8-6157] synthesizing module 'WRAPPER' [SPI\_WRAPPER.v:1] (2 more like this)
  - ⓘ [Synth 8-5534] Detected attribute (\* fsm\_encoding = "one\_hot" \*) [SPI\_SLAVE.v:20]
  - ⓘ [Synth 8-155] case statement is not full and has no default [SPI\_SLAVE.v:76]
- > ⓘ [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
  - ⓘ [Device 21-403] Loading part xc7a35ticipg236-1L
  - ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/lenovo/Desktop/spi/basys\_spi.xdc]. Try xdc].
    - Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with it
  - ⓘ [Synth 8-802] inferred FSM for state register 'cs\_reg' in module 'Slave'
- > ⓘ [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
  - ⓘ [Synth 8-3354] encoded FSM with state register 'cs\_reg' using encoding 'one-hot' in module 'Slave'
- > ⓘ [Synth 8-4480] The timing for the instance i\_0/R/mem\_reg (implemented as a block RAM) might be sub-optimal as no optional output register
  - ⓘ [Project 1-571] Translating synthesized netlist
  - ⓘ [Netlist 29-17] Analyzing 5 Unisim elements for replacement
  - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ⓘ [Project 1-111] Unisim Transformation Summary:
  - No Unisim elements were transformed. (1 more like this)
- ⓘ [Common 17-83] Releasing license: Synthesis





Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 96	Total Number of Endpoints: 96	Total Number of Endpoints: 42

All user specified timing constraints are met.

Hierarchy						
Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N WRAPPER		28	39	0.5	5	1
R (RAM)		2	17	0.5	0	0
S (Slave)		26	22	0	0	0

Tcl Console

Messages

×

Log

Reports

Design Runs

Power

Methodology

Timing

🔍

⏮

⏭

🔍

🗑

🔍

⚠ Warning (1)

🔍

ℹ Info (239)

🔍

📊 Status (483)

Hide All

ℹ [Common 17-206] Exiting Vivado at Fri Mar 14 21:44:44 2025...

📁 Implementation (98 infos, 228 status messages)

📁 Design Initialization (11 infos, 7 status messages)

➤ ⌚ Command: open\_checkpoint {C:/Users/lenovo/Desktop/vivado work/SPI2/SPI2.runs/impl\_1/WRAPPER.dcp} (6 more like this)

ℹ [Netlist 29-17] Analyzing 5 Unisim elements for replacement

ℹ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

ℹ [Project 1-479] Netlist was created with Vivado 2018.2

ℹ [Device 21-403] Loading part xc7a35ticpg236-1L

ℹ [Project 1-570] Preparing netlist for logic optimization

ℹ [Timing 38-478] Restoring timing data from binary archive.

ℹ [Timing 38-479] Binary timing data restore complete.

ℹ [Project 1-856] Restoring constraints from binary archive.

ℹ [Project 1-853] Binary constraint restore complete.

ℹ [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.

ℹ [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

➤ 📁 Opt Design (30 infos, 54 status messages)

➤ ⌚ Command: opt\_design (53 more like this)

ℹ [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'

ℹ [Project 1-461] DRC finished with 0 Errors

ℹ [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

ℹ [Opt 31-49] Retargeted 0 cell(s).

➤ ℹ [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)

➤ ℹ [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)

ℹ [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

ℹ [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

ℹ [Pwropt 34-9] Applying IDT optimizations ...

ℹ [Pwropt 34-10] Applying ODC optimizations ...

ℹ [Physopt 32-619] Estimated Timing Summary | WNS=5.898 | TNS=0.000 |

ℹ [Pwropt 34-162] WRITE\_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report\_power\_opt to get a complete listing of the BRAM

ℹ [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports

➤ ℹ [Timing 38-35] Done setting XDC timing constraints. (1 more like this)

ℹ [Common 17-83] Releasing license: Implementation

ℹ [Timing 38-480] Writing timing data to binary archive.

ℹ [Common 17-1381] The checkpoint 'C:/Users/lenovo/Desktop/vivado work/SPI2/SPI2.runs/impl\_1/WRAPPER\_opt.dcp' has been generated.

ℹ [runtcl-4] Executing : report\_drc -file WRAPPER\_drc\_opted.rpt -pb WRAPPER\_drc\_opted.pb -rpx WRAPPER\_drc\_opted.rpx

ℹ [IP\_Flow 19-234] Refreshing IP repositories

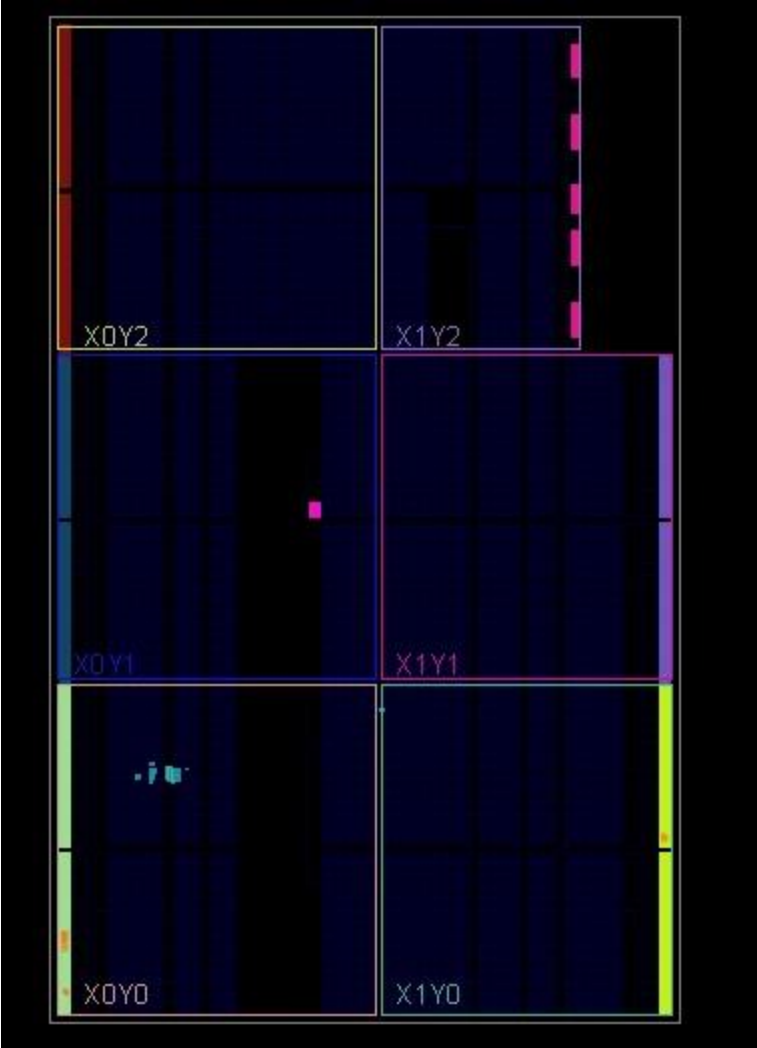
ℹ [IP\_Flow 19-1704] No user IP repositories specified

ℹ [IP\_Flow 19-2313] Loaded Vivado IP repository 'D:/vivado/2018.2/data/ip'.

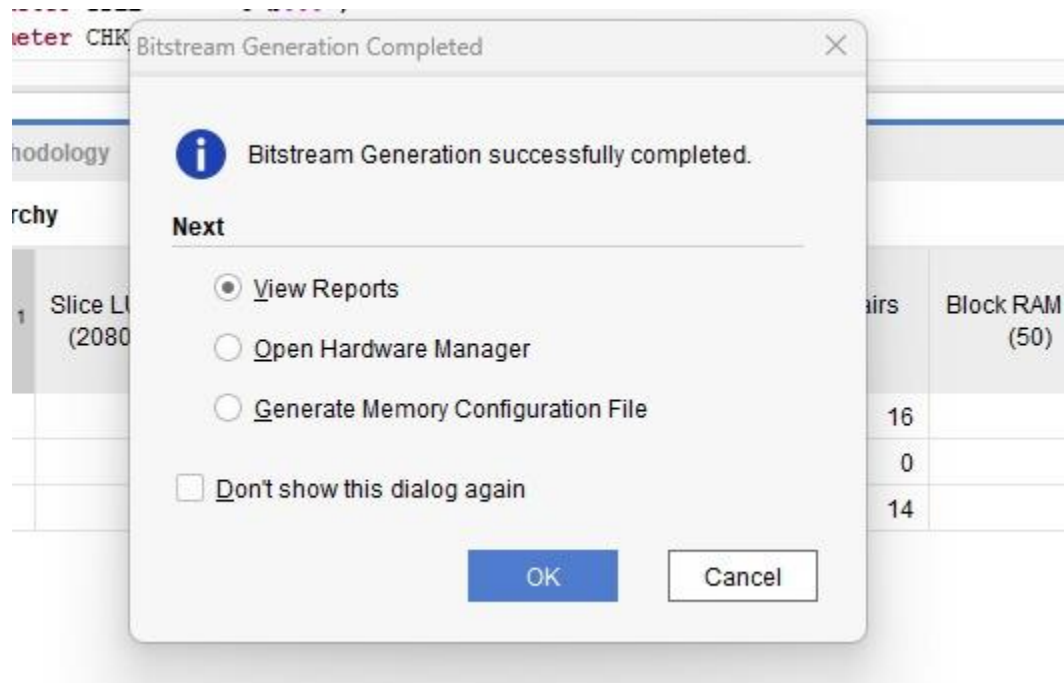
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.602 ns	Worst Hold Slack (WHS): 0.055 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 97	Total Number of Endpoints: 97	Total Number of Endpoints: 42

**All user specified timing constraints are met.**





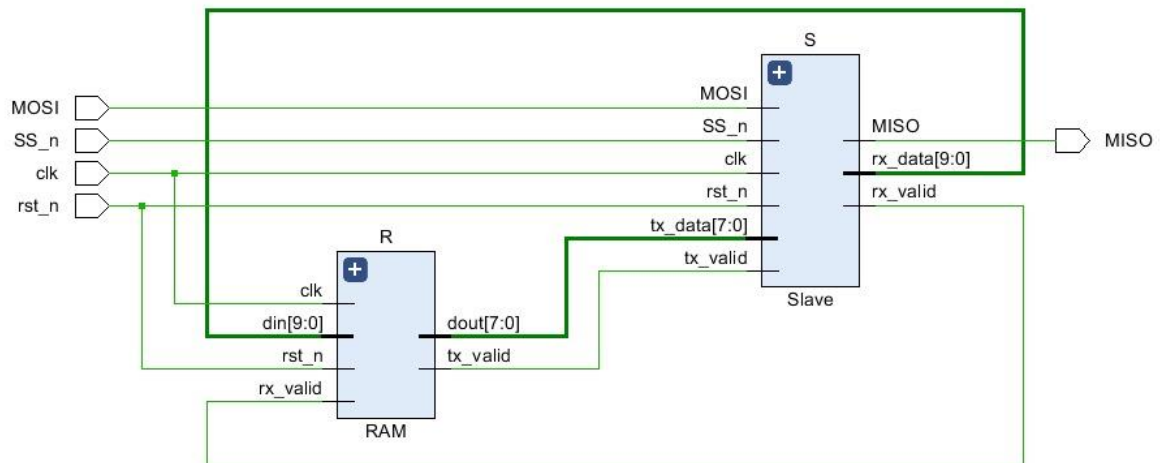
Hierarchy									
Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER		29	39	13	29	16	0.5	5	1
R (RAM)		3	17	5	3	0	0.5	0	0
S (Slave)		26	22	10	26	14	0	0	0



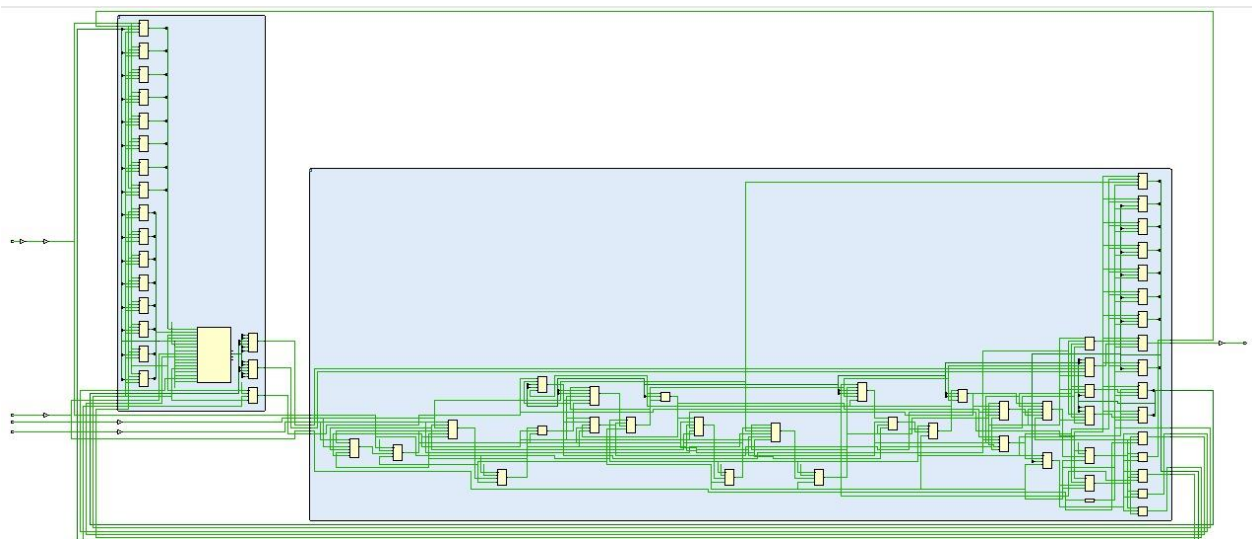
Last for sequential:

Elaboration:

- Elaborated Design (12 infos, 7 status messages)
      - General Messages (12 infos, 7 status messages)
        - [Synth 8-6157] synthesizing module 'WRAPPER' [SPI\_WRAPPER.v:1] (2 more like this)
        - [Synth 8-5534] Detected attribute (\* fsm\_encoding = "Sequential" \*) [SPI\_SLAVE.v:20]
        - [Synth 8-155] case statement is not full and has no default [SPI\_SLAVE.v:76]
        - [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
        - [Device 21-403] Loading part xc7a35ticpg236-1L
        - [Project 1-570] Preparing netlist for logic optimization
        - Processing XDC Constraints (6 more like this)
          - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
          - [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.



Synthesis:



- ① Command: synth\_design -top WRAPPER -part xc7a35tcpg236-1L (10 more like this)
  - ① [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- > ① [Synth 8-6157] synthesizing module 'WRAPPER' [SPL\_WRAPPER.v:1] (2 more like this)
  - ① [Synth 8-5534] Detected attribute (\* fsm\_encoding = "Sequential" \*) [SPL\_SLAVE.v:20]
  - ① [Synth 8-155] case statement is not full and has no default [SPL\_SLAVE.v:76]
- > ① [Synth 8-6155] done synthesizing module 'RAM' (1#1) [RAM.v:1] (2 more like this)
  - ① [Device 21-403] Loading part xc7a35tcpg236-1L
  - ① [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/lenovo/Desktop/spi/basys\_spi.xdc]. These constraints will xdc].
 

Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used\_in\_synthes
  - ① [Synth 8-802] inferred FSM for state register 'cs\_reg' in module 'Slave'
- > ① [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
- ① [Synth 8-3354] encoded FSM with state register 'cs\_reg' using encoding 'sequential' in module 'Slave'
- > ① [Synth 8-4480] The timing for the instance i\_0/R/mem\_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged
  - ① [Project 1-571] Translating synthesized netlist
  - ① [Netlist 29-17] Analyzing 5 Unisim elements for replacement
  - ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ① [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  - ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ① [Project 1-111] Unisim Transformation Summary:
  - No Unisim elements were transformed. (1 more like this)
  - ① [Common 17-83] Releasing license: Synthesis
  - ① [Constraints 18-5210] No constraint will be written out.
  - ① [Common 17-1381] The checkpoint 'C:/Users/lenovo/Desktop/vivado work/project\_9/project\_9.runs/synth\_1/WRAPPER.dcp' has been generated.
  - ① [runtcl-4] Executing : report\_utilization -file WRAPPER\_utilization\_synth.rpt -pb WRAPPER\_utilization\_synth.pb
  - ① [Common 17-206] Exiting Vivado at Fri Mar 14 22:07:56 2025...
- ✖ Synthesized Design (6 infos, 2 status messages)
  - ✖ General Messages (6 infos, 2 status messages)
    - ① [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - ① [Project 1-479] Netlist was created with Vivado 2018.2
    - ① [Project 1-570] Preparing netlist for logic optimization
    - > ① Parsing XDC File [basys\_spi.xdc] (1 more like this)

```

92 |-----|
93 |           State |           New Encoding |           Previous Encoding
94 |-----|-----|-----|
95 |           IDLE |           000 |           000
96 |        CHK_CMD |           001 |           001
97 |          WRITE |           010 |           100
98 |        READ_ADD |           011 |           010
99 |        READ_DATA |           100 |           011
100 |-----|-----|-----|
101 | INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'Slave'

```

## Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 94	Total Number of Endpoints: 94	Total Number of Endpoints: 40

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER	25	37	0.5	5	1
R (RAM)	2	17	0.5	0	0
S (Slave)	23	20	0	0	0

## Implementation:

☒ Warning (1)
☒ Info (239)
☒ Status (477)

Implementation (98 infos, 228 status messages)

Design Initialization (11 infos, 7 status messages)

Command: open\_checkpoint {C:/Users/lenovo/Desktop/vivado work/project\_9/project\_9.runs/impl\_1/WRAPPER.dcp} (6 more like this)

[Netlist 29-17] Analyzing 5 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

[Project 1-479] Netlist was created with Vivado 2018.2

[Device 21-403] Loading part xc7a35t1cp236-1L

[Project 1-570] Preparing netlist for logic optimization

[Timing 38-478] Restoring timing data from binary archive.

[Timing 38-479] Binary timing data restore complete.

[Project 1-856] Restoring constraints from binary archive.

[Project 1-853] Binary constraint restore complete.

[Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.

[Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

Opt Design (30 infos, 54 status messages)

Command: opt\_design (53 more like this)

[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'

[Project 1-461] DRC finished with 0 Errors

[Project 1-462] Please refer to the DRC report (report\_drc) for more information.

[Opt 31-49] Retargeted 0 cell(s).

[Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)

[Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)

[Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

[Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

[Pwropt 34-91] Applying IDT optimizations



## Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.373 ns	Worst Hold Slack (WHS): 0.101 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 95	Total Number of Endpoints: 95	Total Number of Endpoints: 40

All user specified timing constraints are met.

Q % Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
WRAPPER		26	37	13	26	11	0.5	5	1
R (RAM)		3	17	6	3	0	0.5	0	0
S (Slave)		23	20	9	23	11	0	0	0

