SAP-1 RTL

Fetching cycle "Fixed for all instructions"

T0: Mar <= Pc #Pc out, Mar load

T1: Pc <= PC+1 #Pc increment

T2: IR <=MEM[Mar] #Memory read , IR load

Execution cycle "Depend on the instruction itself"

LDA: T3: Mar <= IR (3-0) #Mar load, IR Out.

OP-CODE T4: AC <= MEM[Mar] #Memory read, AC load.

0000 T5: Nothing #Nothing.

ADD: T3: Mar <= IR (3-0) #Mar load, IR out.

OP-CODE T4: B <= MEM[Mar] #Memory read , B load.

0001 T5: AC <= AC + B #AC load, Alu add, Alu out.

SUB: T3: Mar <= IR (3-0) #Mar load, IR out.

OP-CODE T4: B <= MEM[Mar] #Memory read, B load.

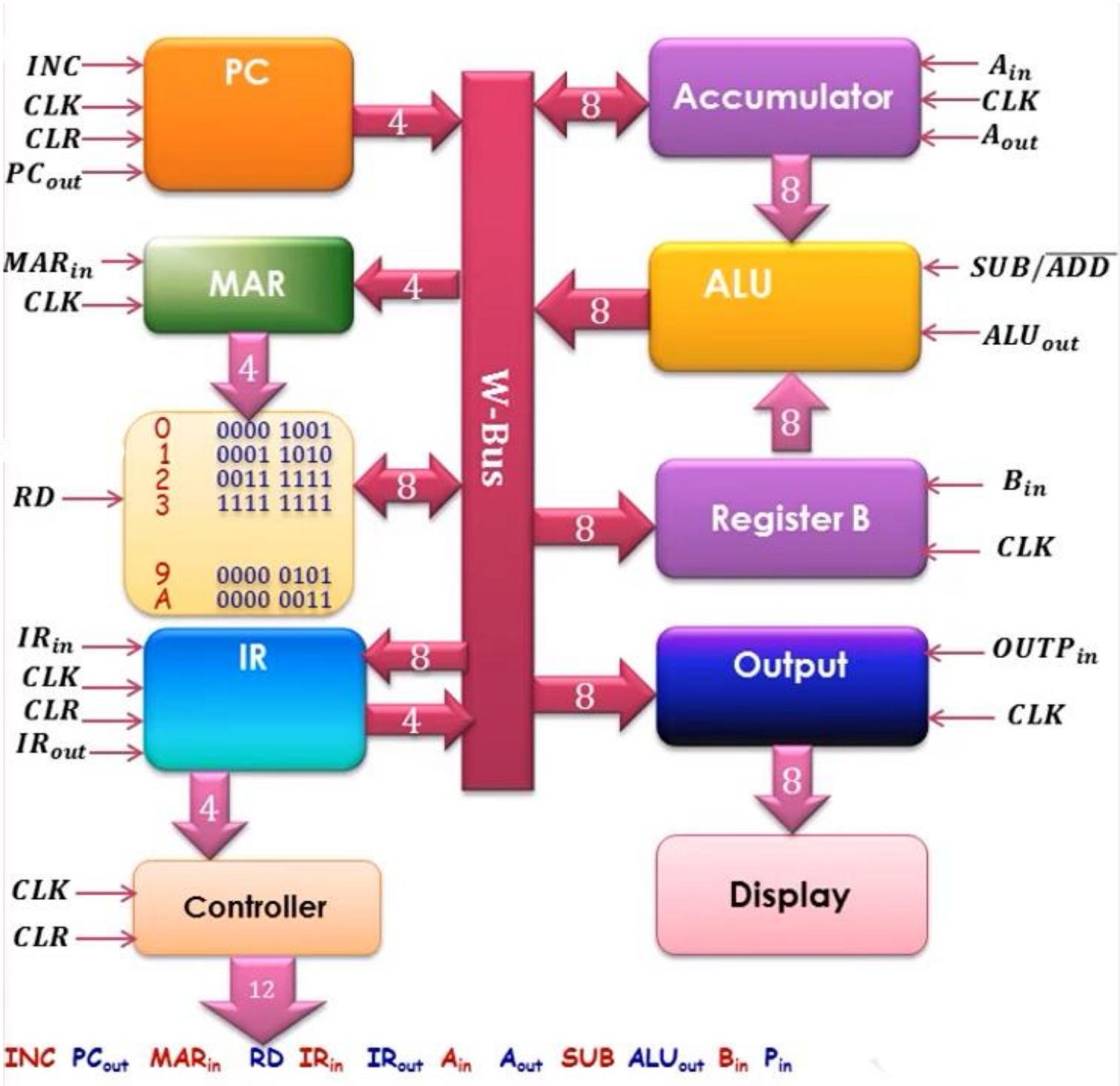
0010 T5: AC <= AC – B #AC load, Alu sub, Alu out.

OUT: T3: P <= AC #AC Out, P load.

OP-CODE T4: Nothing #Nothing.

0011 T5: Nothing #Nothing.

HLT : OP-CODE => 1111


INC
CLK
CLR
PC_out
PC
4
W-Bus
8
Accumulator
A_in
CLK
A_out
8
MAR_in
CLK
MAR
4
4
ALU
SUB/ADD
ALU_out
8
8
0 0000 1001
1 0001 1010
2 0011 1111
3 1111 1111
9 0000 0101
A 0000 0011
RD
8
8
Register B
B_in
CLK
IR_in
CLK
CLR
IR_out
IR
8
4
8
Output
OUTP_in
CLK
4
8
CLK
CLR
Controller
Display
12
INC PC_out MAR_in RD IR_in IR_out A_in A_out SUB ALU_out B_in P_in