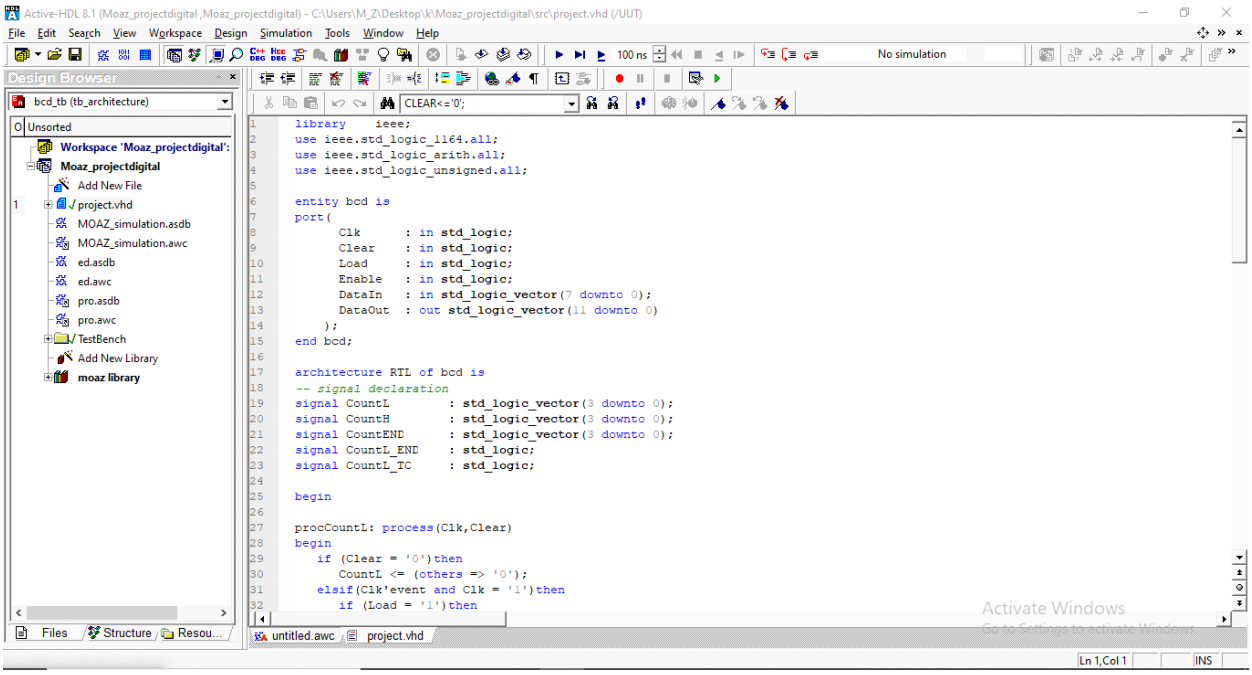
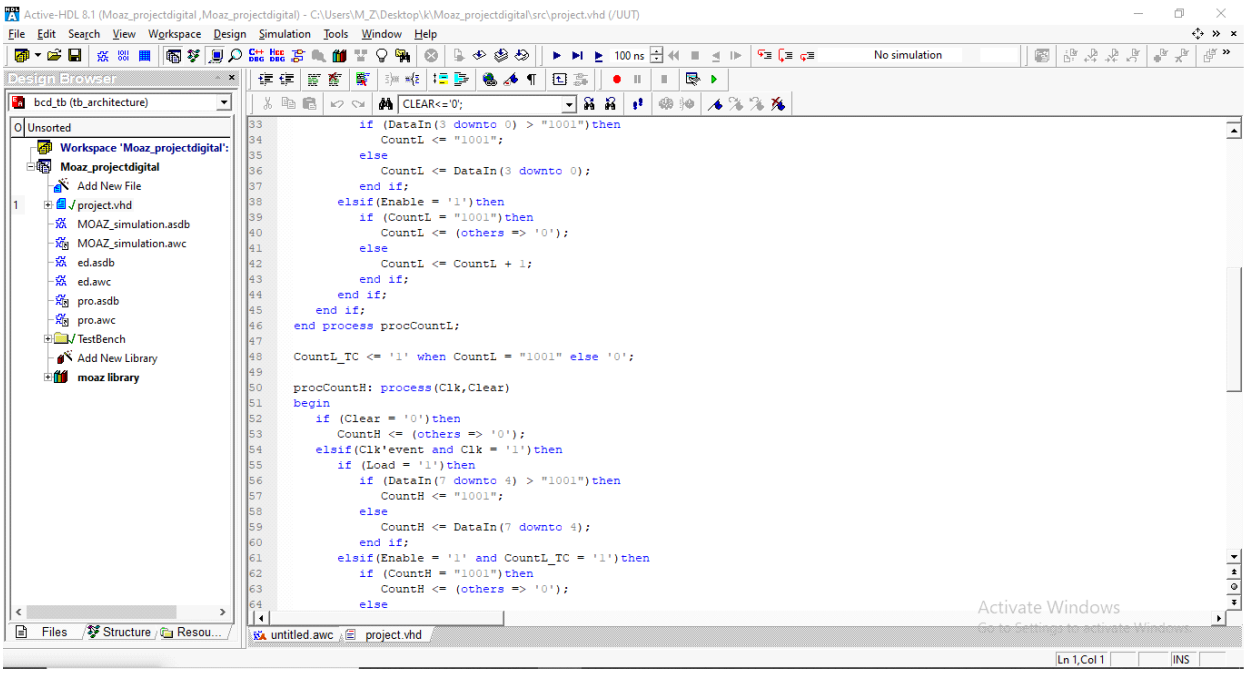
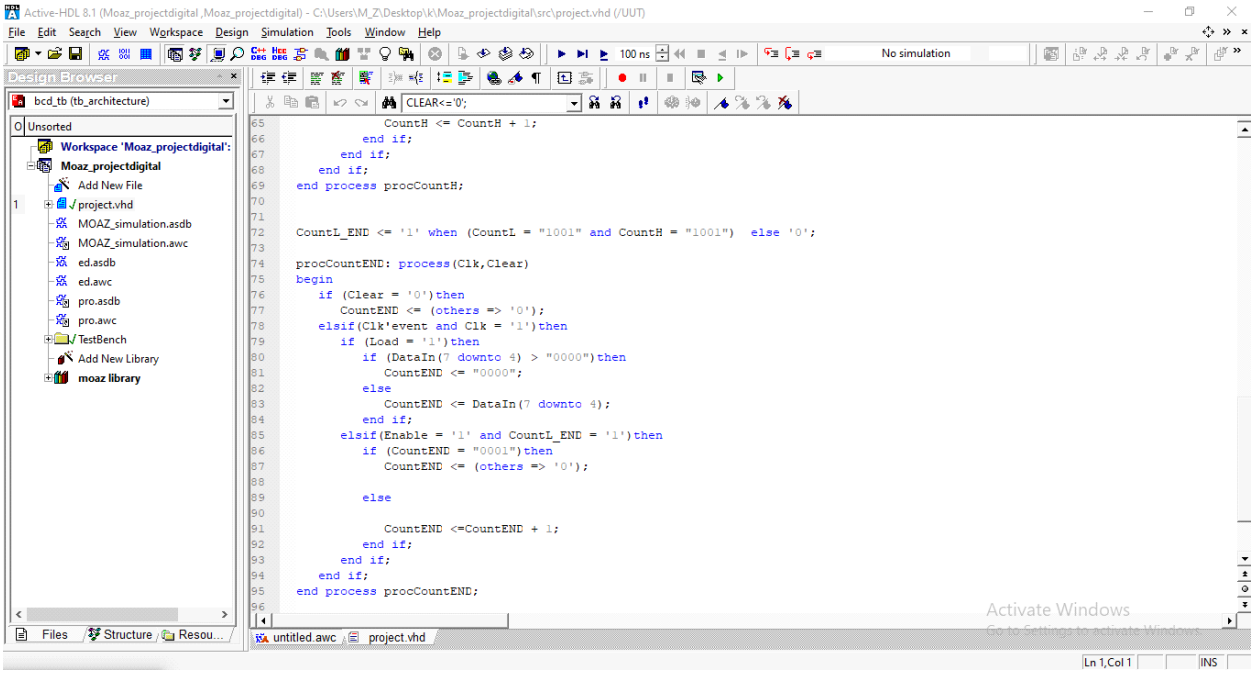
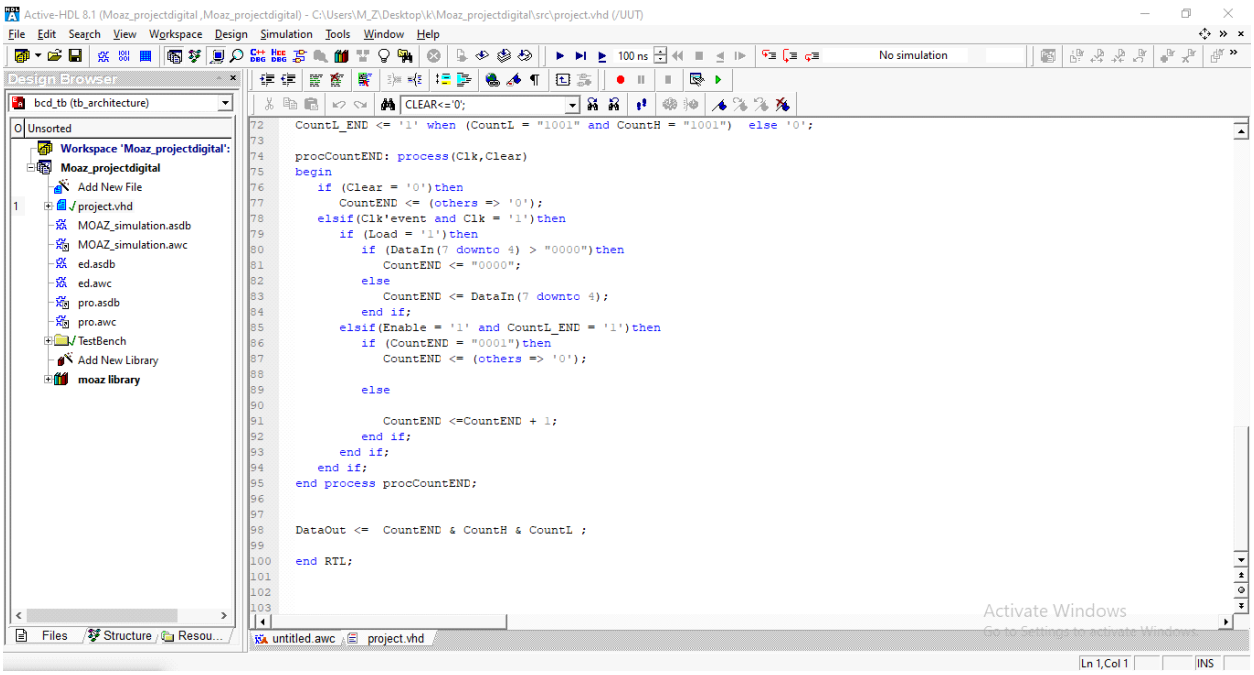
CODE:


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\project.vhd (/UUT)
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
Add New Library
moaz library
Files Structure Resou...
untitled.awc project.vhd
Ln 1,Col 1 INS
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4 use ieee.std_logic_unsigned.all;
5
6 entity bcd is
7 port(
8 Clk : in std_logic;
9 Clear : in std_logic;
10 Load : in std_logic;
11 Enable : in std_logic;
12 DataIn : in std_logic_vector(7 downto 0);
13 DataOut : out std_logic_vector(11 downto 0)
14);
15 end bcd;
16
17 architecture RTL of bcd is
18 -- signal declaration
19 signal CountL : std_logic_vector(3 downto 0);
20 signal CountH : std_logic_vector(3 downto 0);
21 signal CountEND : std_logic_vector(3 downto 0);
22 signal CountL_END : std_logic;
23 signal CountL_TC : std_logic;
24
25 begin
26
27 procCountL: process(Clk,Clear)
28 begin
29 if (Clear = '0')then
30 CountL <= (others => '0');
31 elsif(Clk'event and Clk = '1')then
32 if (Load = '1')then


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\project.vhd (/UUT)
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
Add New Library
moaz library
Files Structure Resou...
untitled.awc project.vhd
Ln 1,Col 1 INS
33 if (DataIn(3 downto 0) > "1001")then
34 CountL <= "1001";
35 else
36 CountL <= DataIn(3 downto 0);
37 end if;
38 elsif(Enable = '1')then
39 if (CountL = "1001")then
40 CountL <= (others => '0');
41 else
42 CountL <= CountL + 1;
43 end if;
44 end if;
45 end if;
46 end process procCountL;
47
48 CountL_TC <= '1' when CountL = "1001" else '0';
49
50 procCountH: process(Clk,Clear)
51 begin
52 if (Clear = '0')then
53 CountH <= (others => '0');
54 elsif(Clk'event and Clk = '1')then
55 if (Load = '1')then
56 if (DataIn(7 downto 4) > "1001")then
57 CountH <= "1001";
58 else
59 CountH <= DataIn(7 downto 4);
60 end if;
61 elsif(Enable = '1' and CountL_TC = '1')then
62 if (CountH = "1001")then
63 CountH <= (others => '0');
64 else


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\project.vhd (/UUT)
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
CountH <= CountH + 1;
end if;
end if;
end if;
end process procCountH;
CountL_END <= '1' when (CountL = "1001" and CountH = "1001") else '0';
procCountEND: process(Clk,Clear)
begin
if (Clear = '0')then
CountEND <= (others => '0');
elsif(Clk'event and Clk = '1')then
if (Load = '1')then
if (DataIn(7 downto 4) > "0000")then
CountEND <= "0000";
else
CountEND <= DataIn(7 downto 4);
end if;
elsif(Enable = '1' and CountL_END = '1')then
if (CountEND = "0001")then
CountEND <= (others => '0');
else
CountEND <=CountEND + 1;
end if;
end if;
end if;
end process procCountEND;
untitled.awc project.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\project.vhd (/UUT)
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
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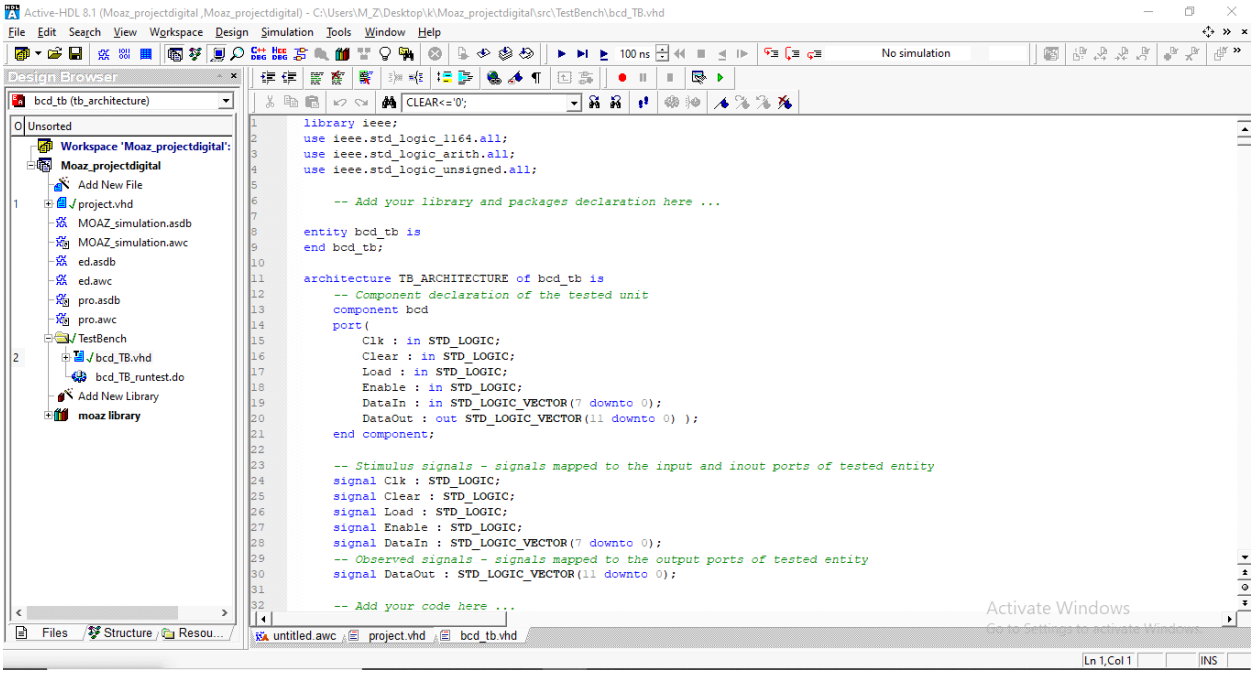
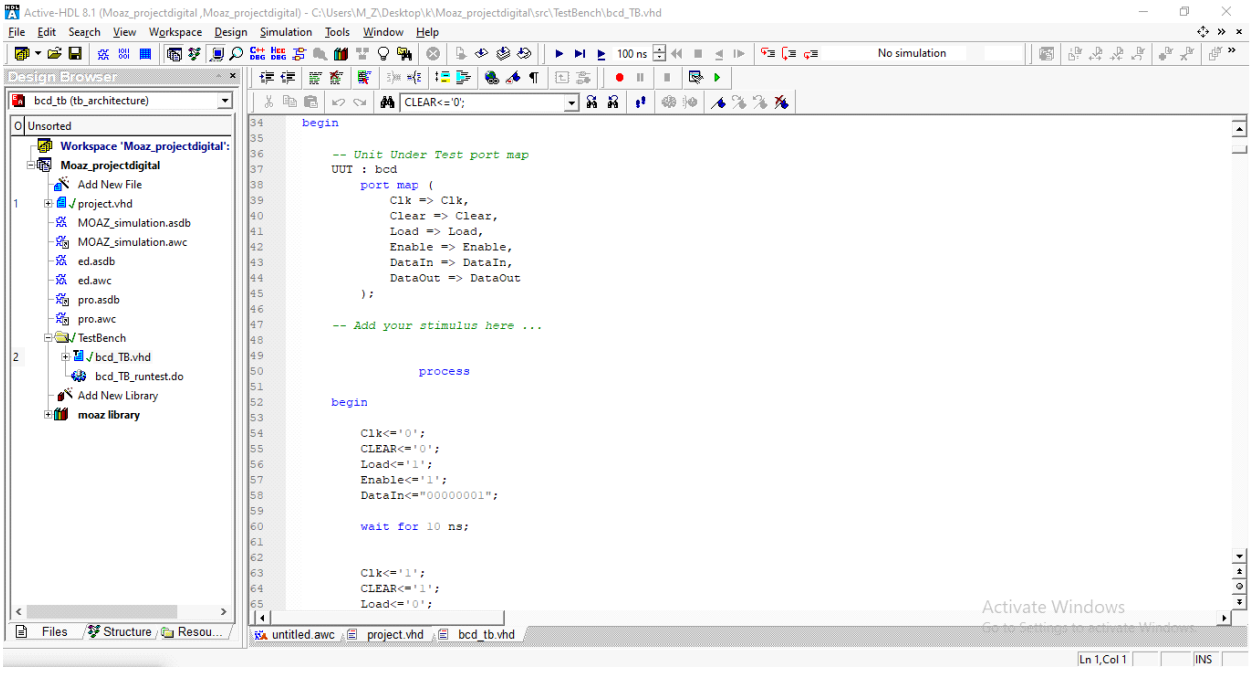
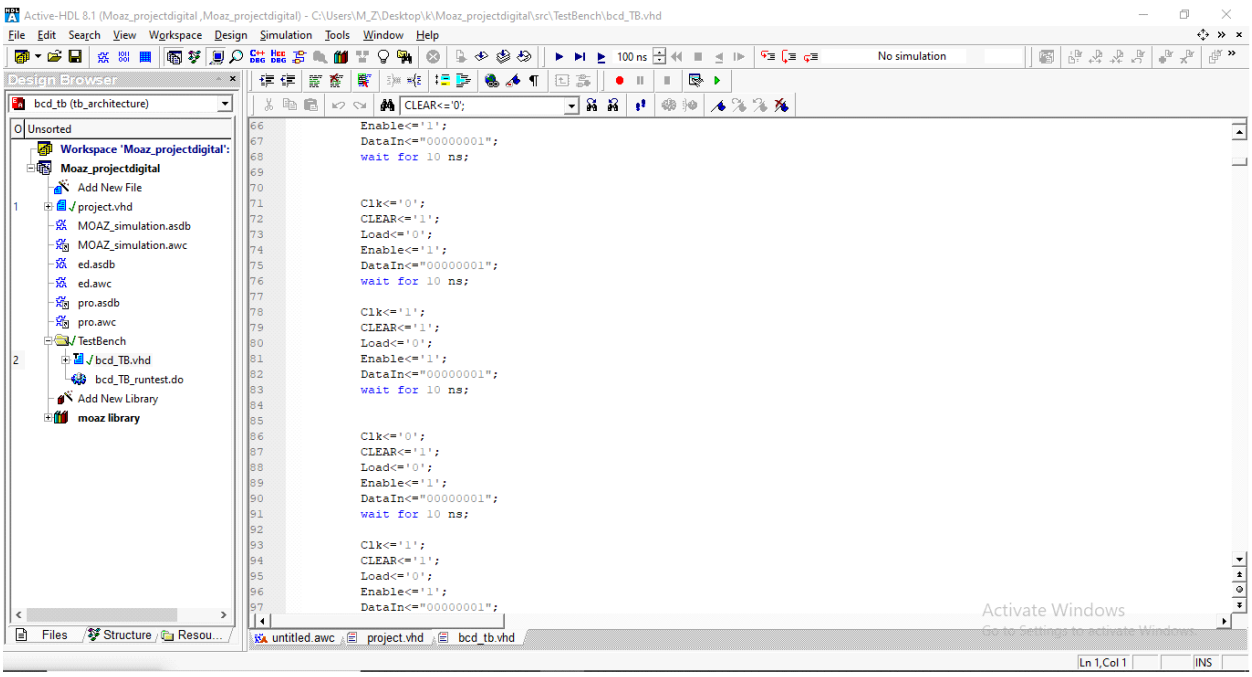
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
CountL_END <= '1' when (CountL = "1001" and CountH = "1001") else '0';
procCountEND: process(Clk,Clear)
begin
if (Clear = '0')then
CountEND <= (others => '0');
elsif(Clk'event and Clk = '1')then
if (Load = '1')then
if (DataIn(7 downto 4) > "0000")then
CountEND <= "0000";
else
CountEND <= DataIn(7 downto 4);
end if;
elsif(Enable = '1' and CountL_END = '1')then
if (CountEND = "0001")then
CountEND <= (others => '0');
else
CountEND <=CountEND + 1;
end if;
end if;
end if;
end process procCountEND;
DataOut <= CountEND & CountH & CountL ;
end RTL;
untitled.awc project.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS

TEST_BENCH:


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\TestBench\bcd_TB.vhd
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
bcd_TB.vhd
bcd_TB_runtest.do
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
-- Add your library and packages declaration here ...
entity bcd_tb is
end bcd_tb;
architecture TB_ARCHITECTURE of bcd_tb is
-- Component declaration of the tested unit
component bcd
port(
Clk : in STD_LOGIC;
Clear : in STD_LOGIC;
Load : in STD_LOGIC;
Enable : in STD_LOGIC;
DataIn : in STD_LOGIC_VECTOR(7 downto 0);
DataOut : out STD_LOGIC_VECTOR(11 downto 0));
end component;
-- Stimulus signals - signals mapped to the input and inout ports of tested entity
signal Clk : STD_LOGIC;
signal Clear : STD_LOGIC;
signal Load : STD_LOGIC;
signal Enable : STD_LOGIC;
signal DataIn : STD_LOGIC_VECTOR(7 downto 0);
-- Observed signals - signals mapped to the output ports of tested entity
signal DataOut : STD_LOGIC_VECTOR(11 downto 0);
-- Add your code here ...
untitled.awc project.vhd bcd_tb.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\TestBench\bcd_TB.vhd
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
bcd_TB.vhd
bcd_TB_runtest.do
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
begin
-- Unit Under Test port map
UUT : bcd
port map (
Clk => Clk,
Clear => Clear,
Load => Load,
Enable => Enable,
DataIn => DataIn,
DataOut => DataOut
);
-- Add your stimulus here ...
process
begin
Clk<='0';
CLEAR<='0';
Load<='1';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='1';
CLEAR<='1';
Load<='0';
untitled.awc project.vhd bcd_tb.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\TestBench\bcd_TB.vhd
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
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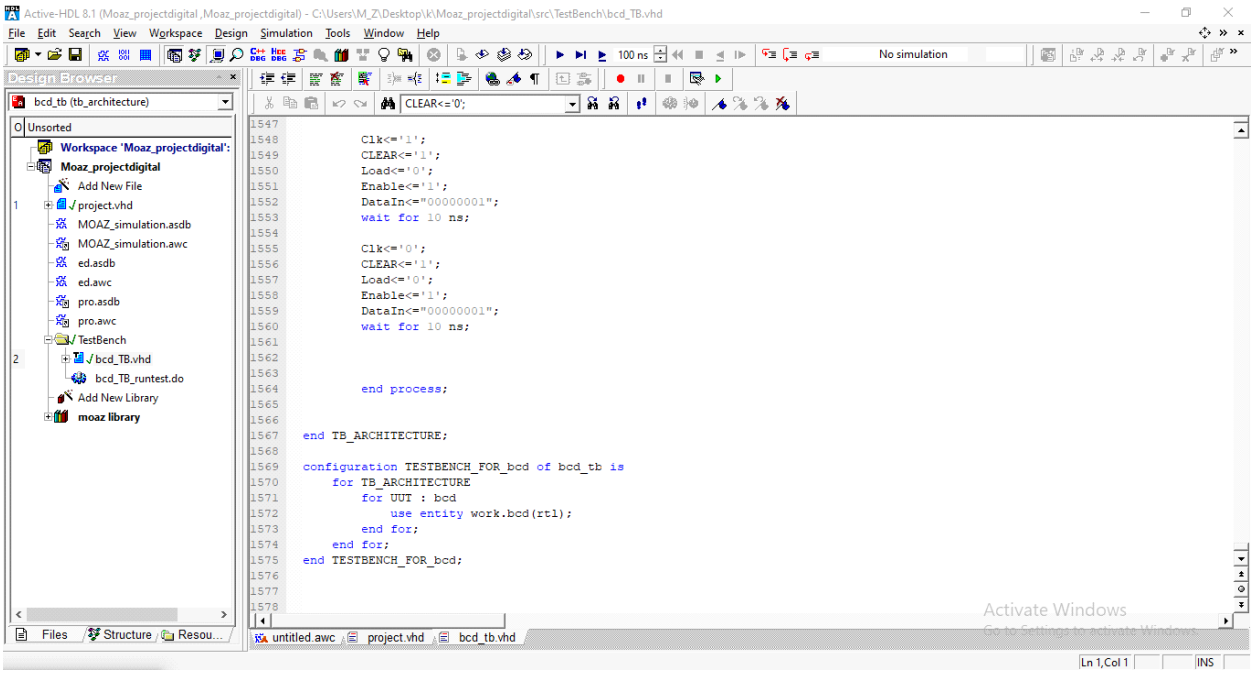
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
bcd_TB.vhd
bcd_TB_runtest.do
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='0';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='1';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='0';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='1';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
untitled.awc project.vhd bcd_tb.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - C:\Users\M_Z\Desktop\k\Moaz_projectdigital\src\TestBench\bcd_TB.vhd
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
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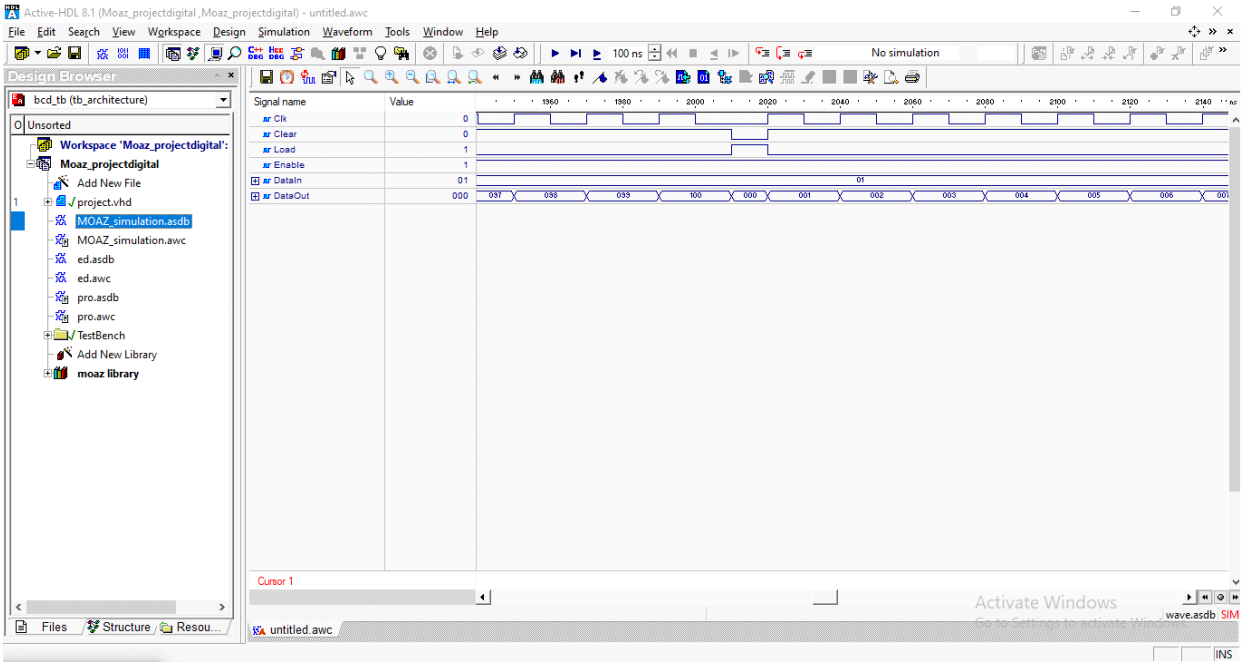
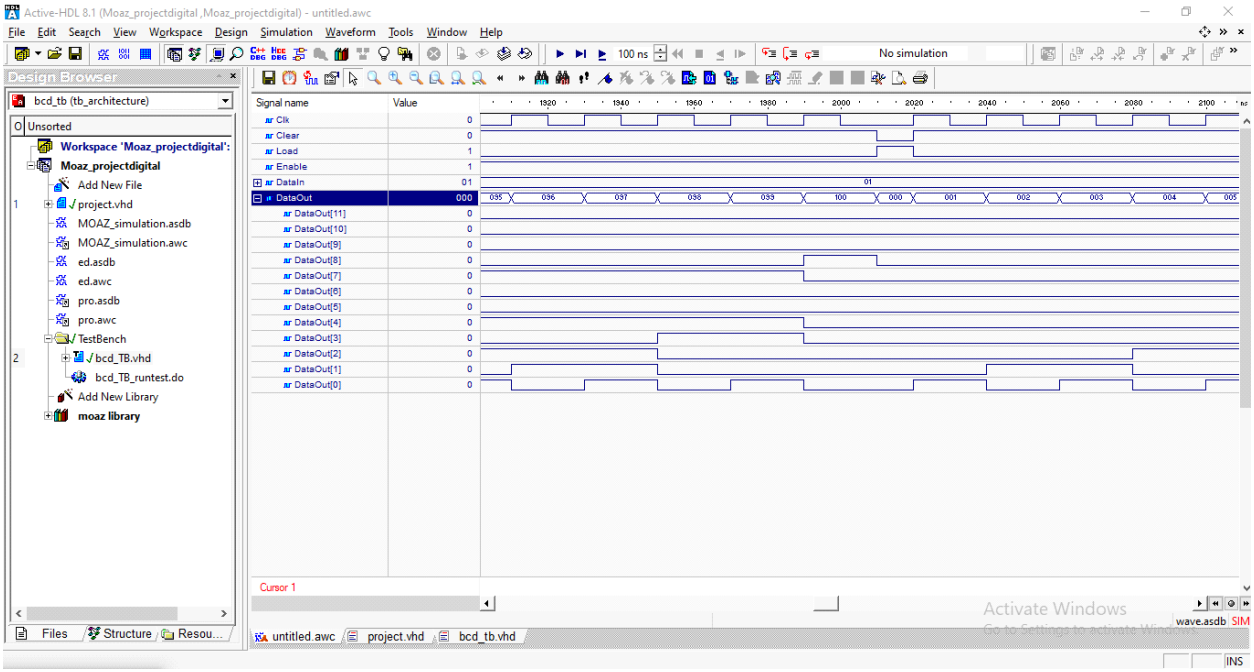
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
bcd_TB.vhd
bcd_TB_runtest.do
Add New Library
moaz library
Files Structure Resou...
CLEAR<='0';
Clk<='1';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
Clk<='0';
CLEAR<='1';
Load<='0';
Enable<='1';
DataIn<="00000001";
wait for 10 ns;
end process;
end TB_ARCHITECTURE;
configuration TESTBENCH_FOR_bcd of bcd_tb is
for TB_ARCHITECTURE
for UUT : bcd
use entity work.bcd(rtl);
end for;
end for;
end TESTBENCH_FOR_bcd;
untitled.awc project.vhd bcd_tb.vhd
Activate Windows
Go to Settings to activate Windows.
Ln 1,Col 1
INS

SIMULATION:


Active-HDL 8.1 (Moaz_projectdigital ,Moaz_projectdigital) - untitled.awc
File Edit Search View Workspace Design Simulation Waveform Tools Window Help
Design Browser
bcd_tb (tb_architecture)
Unsorted
Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
MOAZ_simulation.asdb
MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
Add New Library
moaz library
Signal name
Value
Clk
Clear
Load
Enable
DataIn
DataOut
Cursor 1
Files
Structure
Resou...
untitled.awc
wave.asdb
SIM
INS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bcd_tb (tb_architecture)
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Workspace 'Moaz_projectdigital':
Moaz_projectdigital
Add New File
project.vhd
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MOAZ_simulation.awc
ed.asdb
ed.awc
pro.asdb
pro.awc
TestBench
bcd_TB.vhd
bcd_TB_runtest.do
Add New Library
moaz library
Signal name
Value
Clk
Clear
Load
Enable
DataIn
DataOut
DataOut[11]
DataOut[10]
DataOut[9]
DataOut[8]
DataOut[7]
DataOut[6]
DataOut[5]
DataOut[4]
DataOut[3]
DataOut[2]
DataOut[1]
DataOut[0]
Cursor 1
Files
Structure
Resou...
untitled.awc
project.vhd
bcd_tb.vhd
wave.asdb
SIM
INS