SYSC 4001 Operating Systems Fall 2025

Assignment 1 - L1-14

Mark Bowerman 101272081
Joshua Heinze 101272848

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Github Link: https://github.com/MobDude/SYSC4001_A1/tree/main

Design and Implementation of an Interrupts Simulator

The objective of this section is to build a small simulator of an interrupt system, which could be used for performance analysis of different parts of the interrupt process. This simulator will also be used in Assignment 2 and 3.

All test executions can be found in the github in the executions folder. Test case executions are named execution_trace_x-y.txt where x denotes the variable configurations and y denotes the trace used.

Variable configurations:

1. save/restore context time 10ms, ISR activity time 40ms
2. save/restore context time 20ms, ISR activity time 40ms
3. save/restore context time 30ms, ISR activity time 40ms
4. save/restore context time 10ms, ISR activity time 100ms
5. save/restore context time 10ms, ISR activity time 200ms

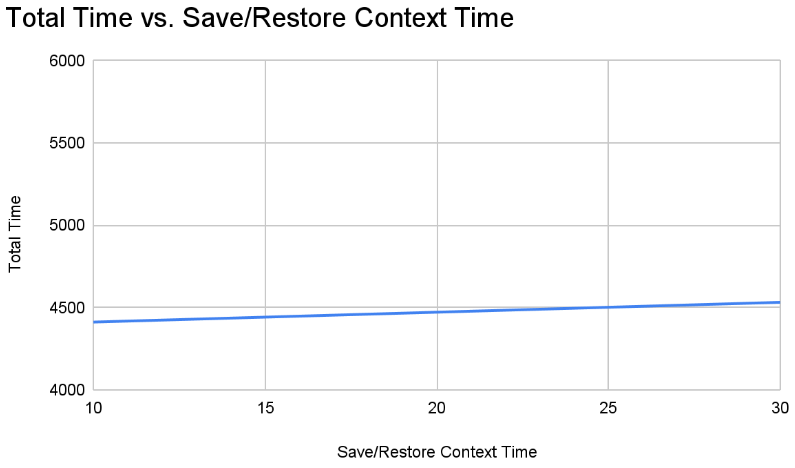
Trace 1		
Save/Restore Context Time	ISR Activity Time	Total time
10	40	3802
20	40	3902
30	40	4002
10	100	4702
10	200	6202

Trace 2		
context_save_time	ISR_time	Total ime
10	40	4412
20	40	4472
30	40	4532
10	100	4952
10	200	5852

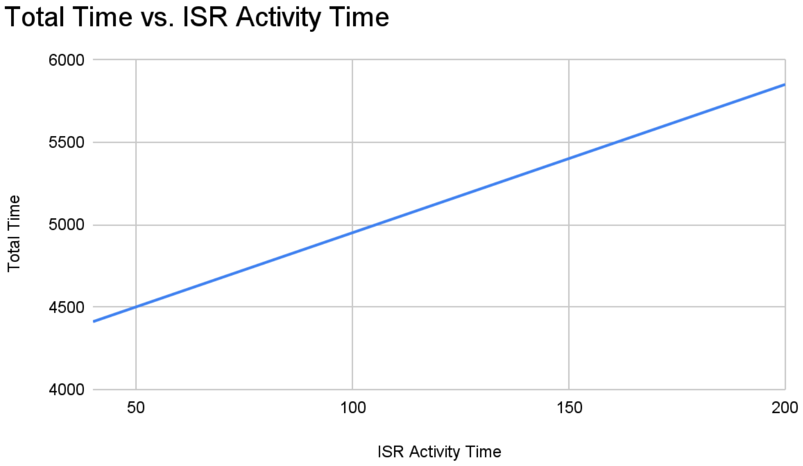
Trace 3		
context_save_time	ISR_time	Total time
10	40	32090
20	40	32750
30	40	33410
10	100	38030
10	200	47930

Trace 4		
context_save_time	ISR_time	Total time
10	40	37607
20	40	38287
30	40	38967
10	100	43727
10	200	53927

Trace 5		
context_save_time	ISR_time	Total time
10	40	32124
20	40	32844
30	40	33564
10	100	38604
10	200	49404



Total Time vs. Save/Restore Context Time



Total Time vs. ISR Activity Time

Based on the test cases, we can see that increasing the save/restore context time and the ISR activity time increases the total execution time on a linear scale. The slope of the scale is the same for both. ISR time tends to affect total execution time much more because it takes much longer and varies by much wider margins.

In the case of having addresses of 4 bytes instead of 2, the number of possible addresses would drastically increase. This has a side effect of every memory reference, interrupt vector fetch and I/O access having 4 bytes instead of just 2. This would increase the context save/restore time because more memory has to be read/written for each operation. By extension the total execution time will also increase slightly for every step that involves addresses.
If the CPU were faster, every CPU burst would take less time and thus a higher percentage of the computer's runtime would be spent on interrupts. This would make CPU bound processes run faster, but would have little to no effect on I/O bound processes.