Project Report for Electronic 2

Design and Simulation of a Complete Power Amplifier

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1 Introduction

In many electronic applications, it is necessary to design amplifiers that not only provide adequate voltage gain but are also capable of delivering sufficient power to the load. This project aims to offer hands-on experience with the design process of a **power amplifier**, covering the stages of analysis, design, simulation, and performance optimization of a bipolar junction transistor (BJT) circuit with a class AB output stage.

The target circuit includes a high-gain differential input stage and a power output stage capable of operating in class AB to deliver a large voltage swing to the load. The main design goals are achieving suitable gain, ensuring a specified quiescent power consumption, providing a wide voltage swing (greater than 16.6 Vp-p), and maintaining total harmonic distortion (THD) below 0.05% at the specified signal level (16.4 Vp-p).

In this project, the DC analysis and bias point determination will be performed first to ensure that all transistors operate in their active regions with appropriate linearity. The output stage (class AB) will be designed to minimize the "dead zone" problem and deliver the required power to the load. Additionally, AC analysis, verification of the Input Common Mode Range (ICMR), and enhancement of the output voltage swing range will be key parts of the design process.

The entire circuit will then be simulated using LTspice to extract expected performance parameters including closed-loop gain, quiescent power consumption, output swing range, and total harmonic distortion (THD). The obtained results will be compared against the design specifications and, if necessary, the circuit will be modified to meet the targets. Finally, the project report will include the final schematic, component values, simulation results, and the relevant analyses.

The main goal of this project is to practice the **complete design process of a practical power amplifier**—from conceptual analysis and topology selection to component sizing and validation via simulation—helping students gain familiarity with real-world circuit design challenges and practical considerations.

2 Analysis of the Given Circuit

Part 1

First, as requested, we simulate the input stage:

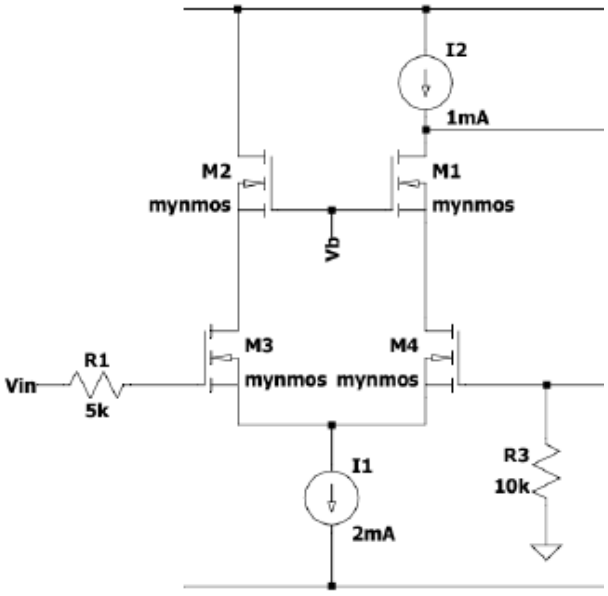

Figure 1: Input stage

Next, we present the output stage:

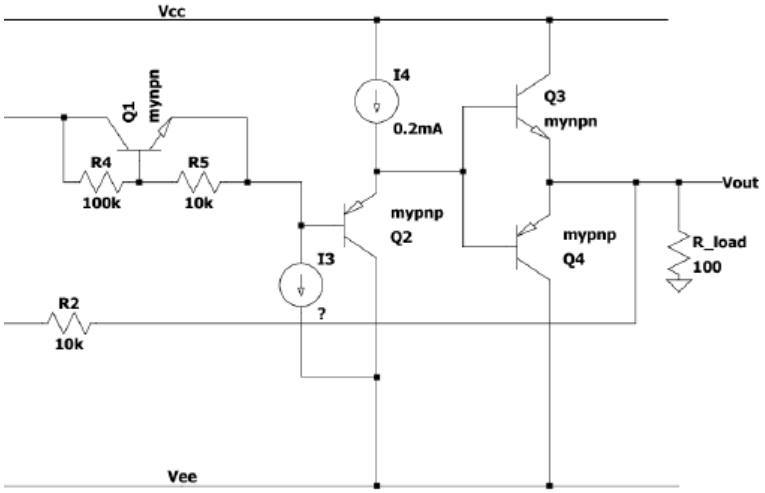

Figure 2: Output stage

We also take into account that the output stage is connected to the input stage through feedback.

Part 2

Functions of the Current Source

- **Precise and stable biasing of Q1 (Vbe multiplier):** Q1 defines the output bias voltage and must operate in the active region. Current source I3 supplies its required current. Because I3 provides a stable current, it improves the stability of Q1's bias voltage against variations in temperature or supply voltage.
- **Controlling the Vbe-multiplier output:** The output voltage of the Vbe multiplier depends on the bias current. Adjusting I3 allows fine control of the overall output stage bias, reducing crossover distortion.
- **Preventing Q1 shutdown:** If I3 provides too little current, Q1 may enter cutoff. I3 ensures that Q1 remains active at all times.
- **Enhancing linearity:** A constant current yields a more accurate Vbe voltage, reducing distortion and improving overall performance.

Summary: The current source acts as a precise bias circuit that ensures Q1 remains in the active region and keeps the output stage properly biased.

Functions of Transistor

- **Emitter-follower (Voltage buffer):** Q2 acts as an emitter follower, transferring the bias voltage with only a small Vbe drop. This provides high input and low output impedance, useful for driving the output stage.
- **Isolation:** Q2 decouples the Vbe multiplier (Q1) from the output stage. It prevents variations in load current from affecting Q1, reducing loading effects.
- **Supplying base current to the output NPN transistor:** In Class B stages, Q2 provides the necessary base current to the output NPN transistor, ensuring correct biasing and reducing crossover distortion.
- **Improving linearity:** As a buffer, Q2 ensures that the bias voltage is accurately delivered to the output pair, resulting in less crossover distortion and cleaner signal output.

Note: In low-power circuits, Q1 might directly bias the output stage. For higher-power or precision designs, Q2 is added to deliver bias voltage with low impedance.

Regarding the minimum current that the current source I_3 must have so that transistor Q_1 remains always ON, it can be determined through simulation that this value is approximately 0.13 or 0.14 mA. However, to be completely confident, we set this value in the circuit to about 0.2 mA.

Next, we observe the simulation results:

First, we implement the circuit as shown below:

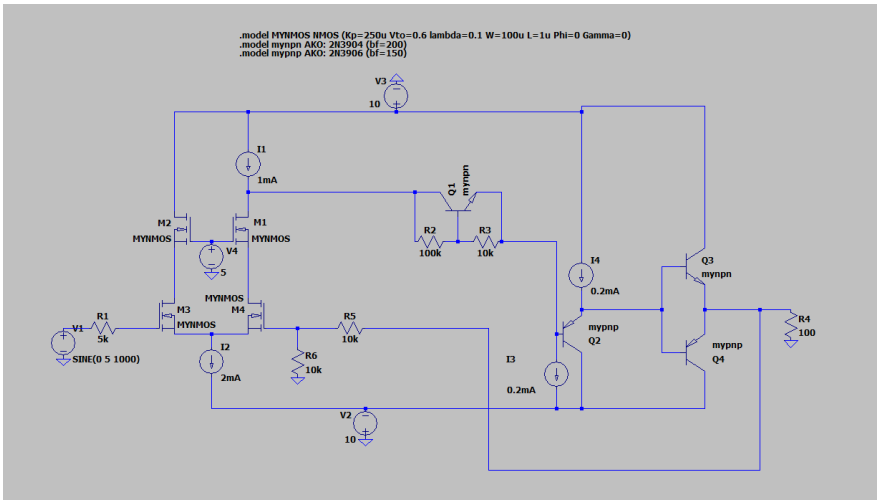

Figure 3: Circuit

Now, for different values of the current source I_3, we observe the collector current of transistor Q_1:

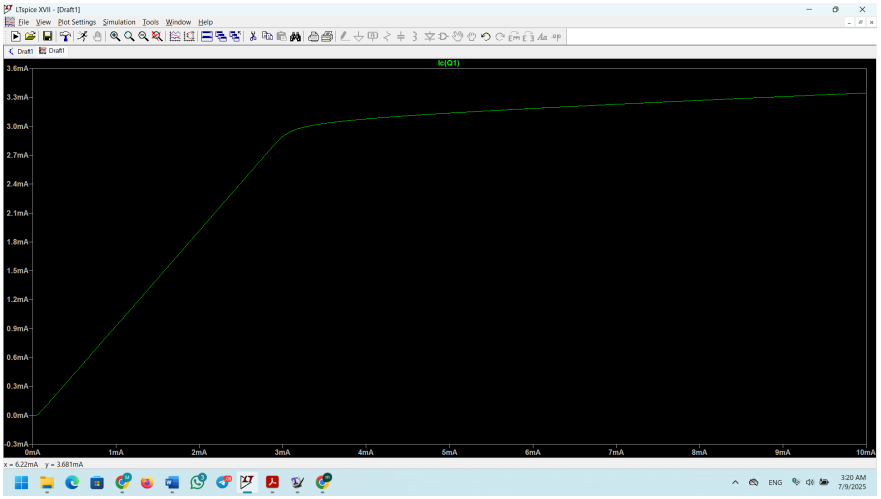

Figure 4: Simulation result

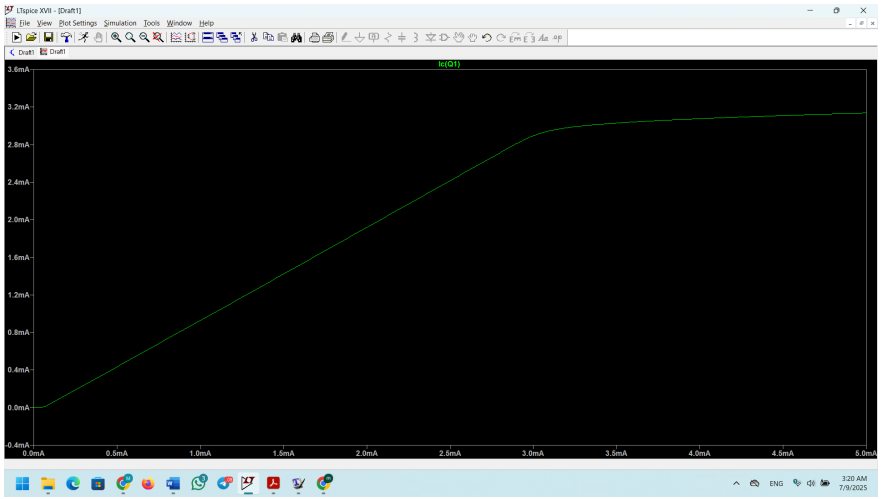

Figure 5: Simulation result

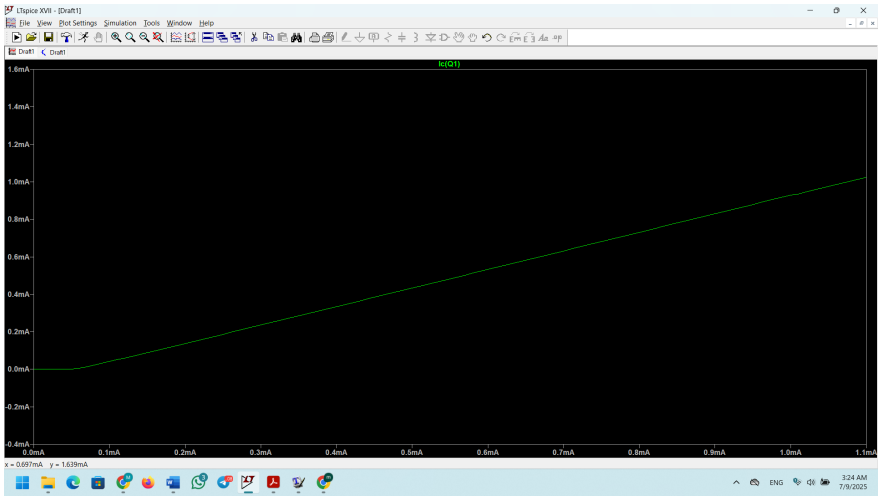

Figure 6: Simulation result

Part 3

	M1	M2	M3	M4	Q1	Q2	Q3	Q4
I(mA)	0.8	1.2	1.2	0.8	0.2	0.2	0	0.8
V	2.88	5.22	5	5.04	7.7	9.3	10	10

Table 1: Operating point

Obtaining the bias currents of transistors M1 to M4 and Q1 and Q2 is straightforward.

To determine the bias currents of Q3 and Q4, we rely on simulation.

We know that our circuit is a ZIZO (zero-in zero-out), but strictly speaking, when the input is 0, the output is not exactly zero—it is a very small value.

Furthermore, we proceed to calculate the gate and source voltages of each MOS transistor, since we already have their bias currents and other parameters.

After finding the gate voltage of M4, we observe that it is a very small value, approximately $-40\,\mathrm{mV}$, and due to a resistive voltage divider, twice that voltage appears at the output, which is about $-80\,\mathrm{mV}$.

Therefore, the current flowing through resistor R is about $-0.8\,\mathrm{mA}$, which suggests that the circuit is in the negative half-cycle, Q3 is off, and the entire current flows through transistor Q4.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \quad , \quad V_{OD} = V_{GS} - Vth$$

$$M1 \quad \Rightarrow \quad 0.8 = \frac{1}{2} \times 0.25 \times 200 \times (V_{OD})^2$$

$$V_{OD} = 0.18V \Rightarrow V_G = 5V \Rightarrow V_S = 4.82V \Rightarrow V_D = 11V_{BE} = 7.7V \Rightarrow V_{DS} = 2.88V$$

$$M2 \quad \Rightarrow \quad 1.2 = \frac{1}{2} \times 0.25 \times 200 \times (V_{OD})^2$$

$$V_{OD} = 0.22V \Rightarrow V_G = 5V \Rightarrow V_S = 4.78V \Rightarrow V_D = 10V \Rightarrow V_{DS} = 5.22V$$

$$M3 \quad \Rightarrow \quad 1.2 = \frac{1}{2} \times 0.25 \times 200 \times (V_{OD})^2$$

$$V_{OD} = 0.22V \Rightarrow V_G = 0V \Rightarrow V_S = -0.22V \Rightarrow V_D = 4.78V \Rightarrow V_{DS} = 5V$$

$$M4 \quad \Rightarrow \quad 0.8 = \frac{1}{2} \times 0.25 \times 200 \times (V_{OD})^2$$

$$V_{OD} = 0.18V \Rightarrow V_G = -0.04V \Rightarrow V_S = -0.22V \Rightarrow V_D = 4.82V \Rightarrow V_{DS} = 5.04V$$

The biasing of the BJT transistors is also relatively simple. The only important point regarding the emitter voltage of transistor Q2 is that, since in the biasing we assumed the circuit is operating in the negative half-cycle, the voltage at this point is $-0.7\,\mathrm{V}$.

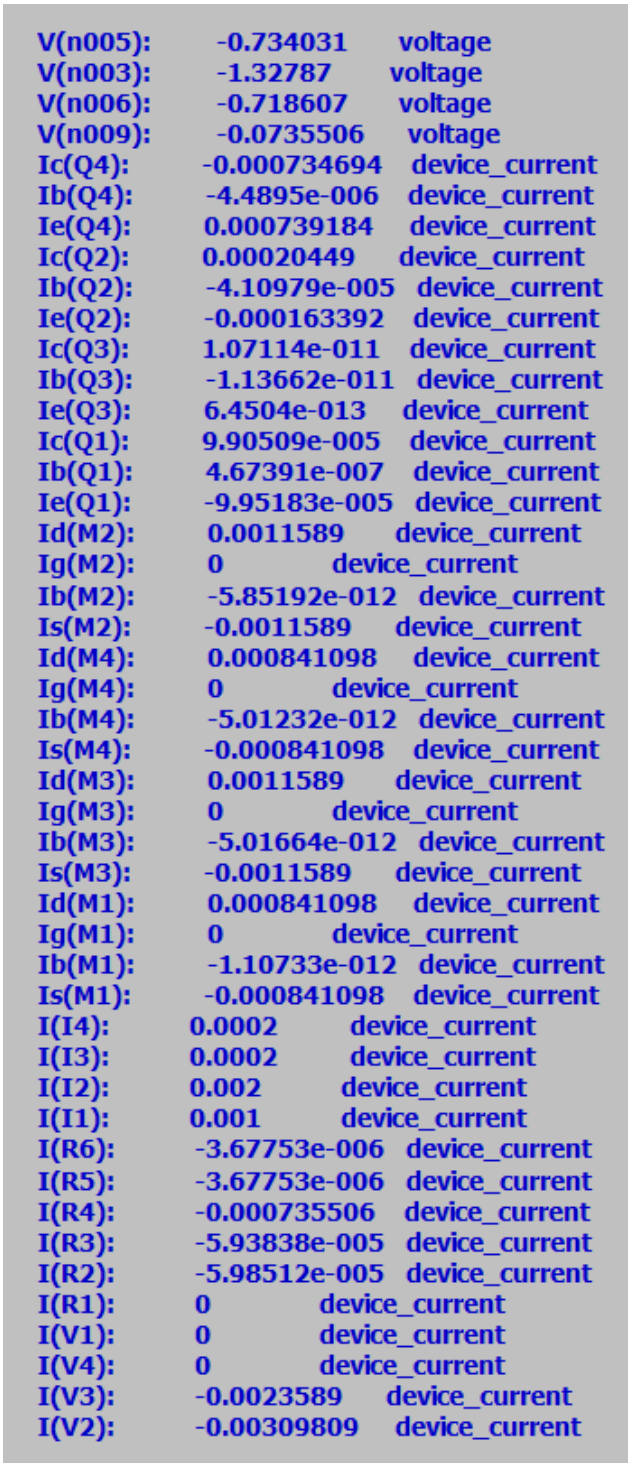

Figure 7: Simulation result

Part 4

As requested, we draw the output stage without feedback and observe that a dead zone exists in it:

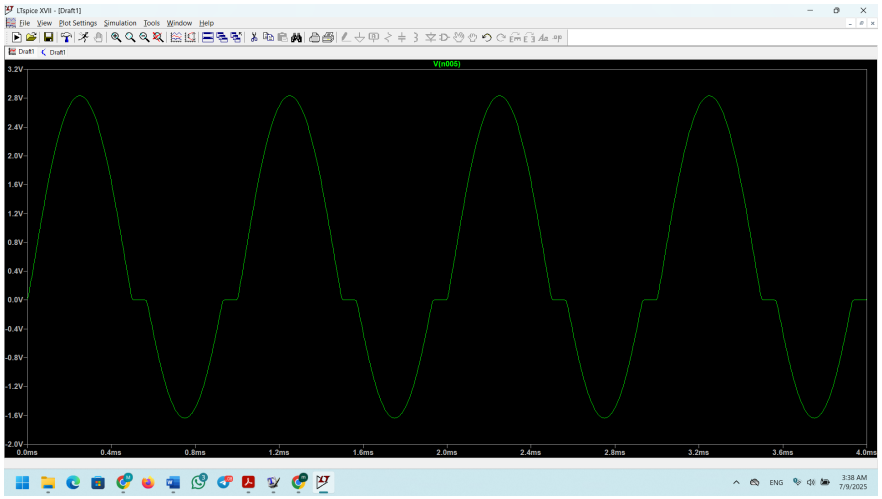

Figure 8: Simulation result

However, the normal output is as shown below, and there is no dead zone:

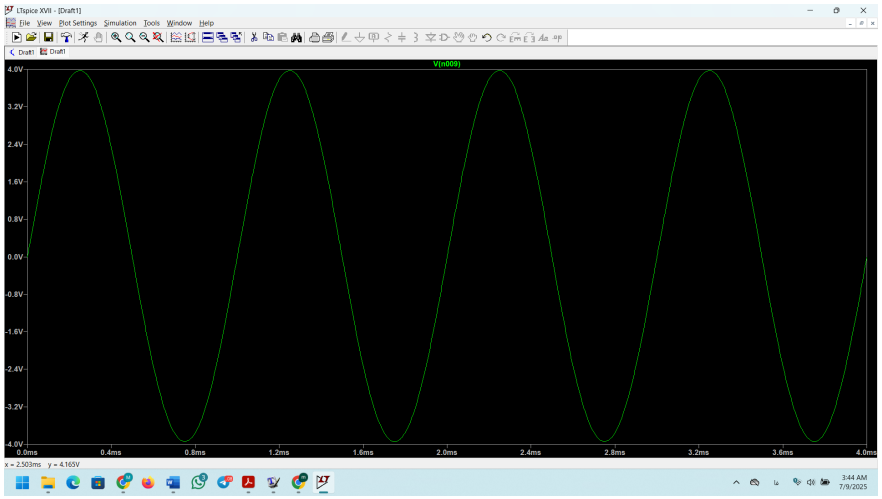

Figure 9: Simulation result

As mentioned in Part 2, the presence of the multiplier circuit and the feedback eliminates the dead zone.

Part 5

Positive Output Swing Analysis

To assess the maximum achievable positive output voltage, both voltage drop limitations and current sourcing capacity must be evaluated:

- **Voltage Limitation:** The NPN output transistor (Q3) must remain outside saturation. Given a supply voltage of $V_{CC} = 10\,\mathrm{V}$ and a saturation voltage of approximately $0.2\,\mathrm{V}$, the theoretical upper bound on output voltage is:
$$V_{\text{max,volt}} = V_{CC} - V_{CE,sat} = 9.8\,\mathrm{V}$$
- **Current Limitation:** The maximum output current depends on the current that can be injected into the base of Q3. Assuming source I_4 delivers its full current and Q3 has a conservative current gain of $\beta = 200$, the practical limit becomes:
$$V_{\text{max,current}} = 4\,\mathrm{V}$$

Hence, the effective positive output swing is limited to:

$$V_{\text{out,max}} = \min(9.8\,\mathrm{V}, 4\,\mathrm{V}) = 4\,\mathrm{V}$$

Negative Output Swing Determination

Unlike the positive direction, the negative output swing is predominantly constrained by voltage levels rather than current delivery:

- **From PNP Saturation:** The lower bound set by the PNP output transistor (Q4), considering $V_{SS} = -10\,\mathrm{V}$ and $V_{CE,sat} \approx -0.2\,\mathrm{V}$, is:
$$V_{\text{min,sat}} = V_{SS} + |V_{CE,sat}| = -9.8\,\mathrm{V}$$

The final bound for the negative swing is thus:

$$V_{\text{out,min}} = -9.8\,\mathrm{V}$$

Input Common Mode Range (ICMR)

The range of allowable input common-mode voltages is determined by both upper and lower boundaries imposed by the operating regions of the differential pair:

- **Upper Limit:** For transistor M3 to remain in saturation, $V_{DS} \geq V_{GS} - V_{th}$ must hold. At the boundary of this condition, and with $V_{D(M3)} = 4.103\,\mathrm{V}$, the highest allowed input level becomes:
$$V_{\text{ICMR,high}} = 4.7\,\mathrm{V}$$
- **Lower Limit:** Considering the minimum required voltage drop across the tail current source and gate-bias conditions:
$$V_{\text{ICMR,low}} = -8.9\,\mathrm{V}$$

Thus, the total ICMR is calculated as:

$$\text{ICMR} = V_{\text{ICMR,high}} - V_{\text{ICMR,low}} = 13.6\,\mathrm{V}$$

Part 6

To concisely summarize the swing limitations discussed in the previous section:

- The **positive swing** is primarily restricted by current driving ability:

$$V_{\text{out,max}} = 4\,\text{V}$$

- The **negative swing** is limited by the PNP Saturation:

$$V_{\text{out,min}} = -9.8\,\text{V}$$

These asymmetrical swing boundaries highlight the need for careful biasing and feedback compensation to maintain signal integrity across the full range of operation.

To evaluate the real-world behavior of the amplifier's output swing, a transient simulation was carried out using LTspice. The goal was to measure the maximum achievable positive output voltage and compare it with the theoretical estimate.

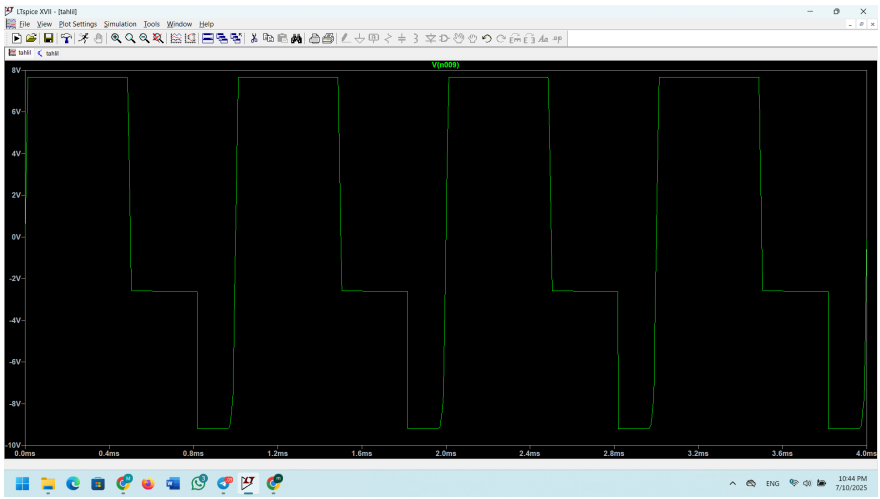

Figure 10: LTspice simulation result showing the output waveform near its upper swing limit.

As shown in Figure, the output voltage reaches approximately 4.5 V, which exceeds the analytically calculated limit of 4 V. This discrepancy can be attributed to the use of ideal current sources in the simulation environment. Unlike real-world implementations, where current mirrors and transistor β impose strict constraints on base drive currents, LTspice treats current sources as ideal, with zero output impedance and infinite compliance voltage.

Consequently, the simulated circuit provides more current to the base of the output-stage transistor (Q_3) than what would be feasible in a practical design, leading to an optimistic swing limit. This highlights the importance of replacing ideal elements with realistic biasing networks (e.g., Wilson current mirrors or diode-connected loads) in future simulations to achieve more accurate results aligned with physical limitations.

Part 7

Relevant simulation results are presented in each respective part.

Part 8

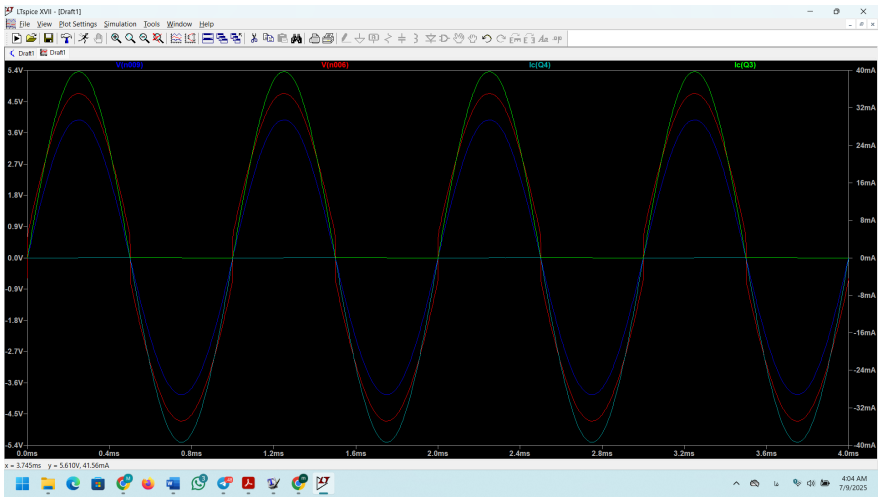

Figure 11: Simulation result

As expected, everything is correct and working perfectly. Transistor Q_3 turns on during the positive half-cycle, and transistor Q_4 turns on during the negative half-cycle. Furthermore, at node X, the voltage in the dead zone region is shifted by the base-emitter voltage, which results in a completely sinusoidal output. This behavior fully matches what was described in Part 4 as well as all the previous sections.

Part 9

In contrast to the original analysis, our modified design achieves a substantially wider output swing through revised biasing strategies. Specifically, by increasing the current source I_4 up to 0.49 mA, the output stage provides sufficient base drive to the NPN transistor (Q_3), enabling the output to reach the full upper voltage limit defined by the power supply rail:

$$V_{\text{out,max}} = V_{CC} - V_{CE,sat} = 10\,\text{V} - 0.2\,\text{V} = 9.8\,\text{V}$$

On the negative side, the circuit demonstrates no significant current or voltage bottleneck. The output swing reaches the lower bound imposed by the saturation of the PNP output transistor (Q_4), which results in:

$$V_{\text{out,min}} = V_{SS} + |V_{CE,sat}| = -10\,\text{V} + 0.2\,\text{V} = -9.8\,\text{V}$$

Therefore, the total achievable output swing is symmetrically extended to nearly the full range between the supply rails:

$$V_{\text{out,swing}} = [-9.8\,\text{V}, +9.8\,\text{V}]$$

This enhancement is attributed to the aggressive bias point engineering, particularly the upscaled base drive current in the output stage. It is important to note that the simulation environment still assumes ideal current sources; however, the chosen current levels remain within practical boundaries for implementation using current mirrors or reference biasing networks.

Such symmetric and maximized swing ensures high dynamic range and improved linearity, especially under large-signal conditions, and is validated through transient simulations.

Part 10

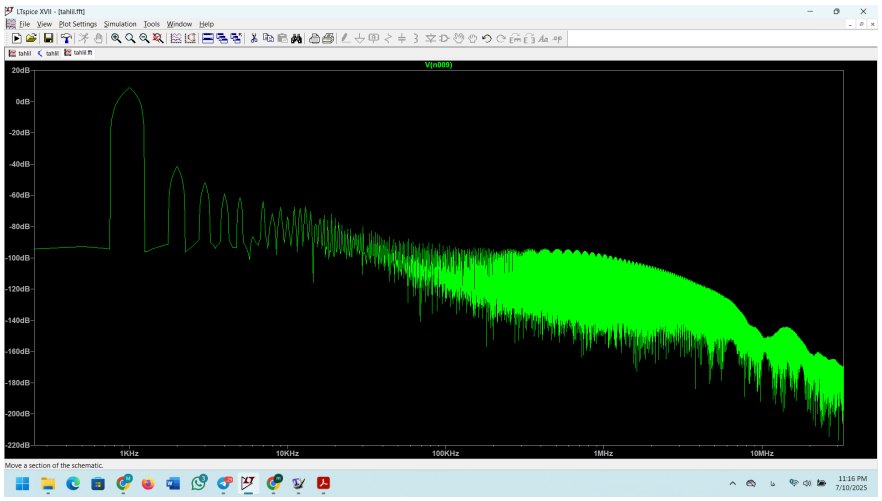

Figure 12: The plot of the Fourier series coefficients of the output voltage for an input signal with a 2 V amplitude

$a_1 = 8.92\,\text{dB} \rightarrow a_1 = 2.79, a_2 = -41.6\,\text{dB} \rightarrow a_2 = 0.0083, a_3 = -51.6\,\text{dB} \rightarrow a_3 = 0.0026, a_4 = -59.1\,\text{dB} \rightarrow a_4 = 0.0011$

To quantitatively assess the linearity of the amplifier output, we compute the Total Harmonic Distortion (THD) using the fundamental and harmonic amplitudes obtained from the Fourier series of the output signal. The THD is defined as:

$$\text{THD} = \frac{\sqrt{a_2^2 + a_3^2 + a_4^2 + \cdots}}{a_1}$$

where:

- a_1 is the amplitude of the fundamental harmonic,
- $a_2, a_3, a_4, \ldots$ are the amplitudes of the higher-order harmonics.

Based on the measured or simulated data, we use the following values:

$$\begin{aligned} a_1 &= 2.79 \\ a_2 &= 0.0083 \\ a_3 &= 0.0026 \\ a_4 &= 0.0011 \end{aligned}$$

Substituting into the THD formula:

$$\text{THD} = \frac{\sqrt{(0.0083)^2 + (0.0026)^2 + (0.0011)^2}}{2.79}$$

Calculating each term individually:

$$\text{THD} = \frac{0.00877}{2.79} \approx 0.00314 \Rightarrow 0.314\%$$

$$\boxed{\text{THD} \approx 0.314\%}$$

This low THD value indicates that the amplifier exhibits excellent linearity with minimal harmonic distortion in the output signal.

Part 11

The total power consumption of the circuit is:

$$P_{\text{total}} = 54.6\,\text{mW}$$

There is a significant trade-off between power consumption and linearity in analog circuit design. To reduce distortion and improve the linearity of the circuit, a higher bias current is usually required so that the transistors operate in their active (linear) region. However, this leads to increased static power consumption.

On the other hand, reducing the bias current to lower power consumption may push the transistors toward cutoff or saturation regions, resulting in increased non-linear distortion.

Conclusion: Improving linearity comes at the cost of higher power consumption. Therefore, the designer must carefully balance these two parameters depending on the application requirements.

Part 6

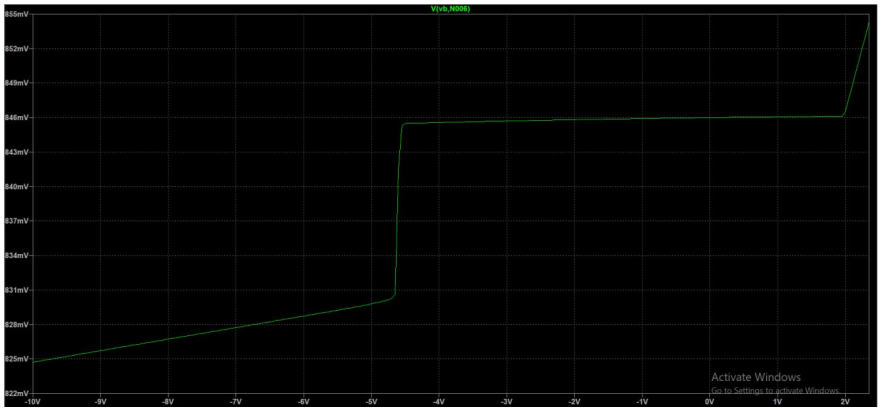

Figure 13: ICMR

3 Design of the Requested Circuit

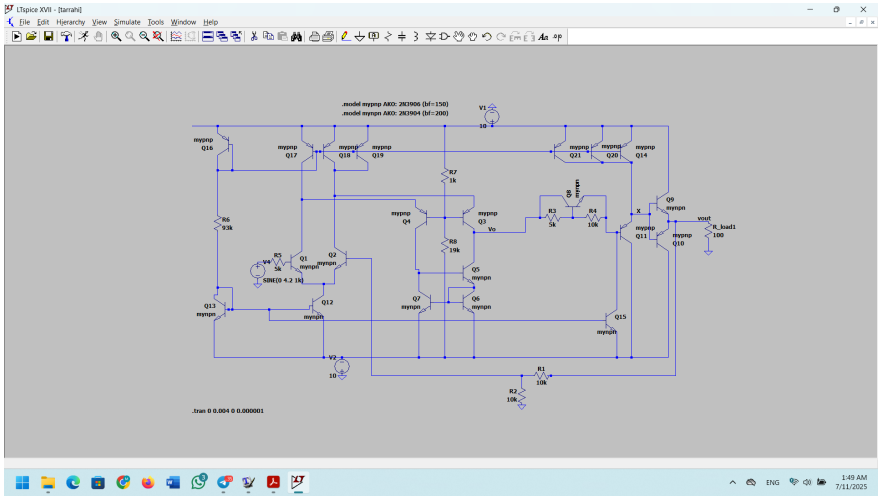

Figure 14: The implemented circuit meets the specified requirements

Advantages of Using Folded Cascode over Traditional Cascode (BJT)

In the implemented amplifier, the input stage was redesigned by replacing the conventional differential cascode with a folded cascode configuration. Since all transistors in the circuit are BJTs, the comparison is based on bipolar behavior. The folded cascode topology offers several advantages over the standard cascode structure, particularly in terms of gain, output swing, and bias flexibility.

1. Increased Output Swing

In a traditional BJT cascode, the output swing is limited due to the series stacking of transistors and the resulting voltage headroom constraints. Each transistor requires a minimum $V_{CE,sat}$ to remain in the active region, thus reducing the available output range. In contrast, the folded cascode separates the signal and bias paths, allowing the output to swing closer to the supply rails, resulting in a significantly wider dynamic range.

2. Separation of Bias and Signal Paths

The folded cascode structure allows the signal current path and the biasing path to be decoupled. This architectural separation facilitates more precise bias point control and greater stability, as the biasing does not directly interfere with the signal amplification process.

3. Improved Voltage Gain

The voltage gain in BJT circuits is given by:

$$A_v = g_m \cdot R_{out} = \frac{I_C}{V_T} \cdot R_{out}$$

Since the folded cascode enables the use of higher effective output resistance (due to current mirror or high-impedance loads), the overall gain increases. This makes the folded configuration particularly attractive for high-gain applications.

4. Reduced Emitter Degeneration Effects

In standard cascode designs, the emitter of the upper transistor is connected to the collector of the lower one, introducing a low output impedance. Folded cascode avoids this configuration, leading to less degeneration and better signal transfer characteristics.

5. Easier Bias Design

Because of the topological separation between the input differential pair and the current path to the output node, folded cascode makes it easier to independently control current sources and bias voltages, especially in low-voltage environments.

6. Enhanced Symmetry in Differential Designs

Folded cascode topologies are well-suited for differential amplifiers due to their high symmetry and layout flexibility. They allow for balanced signal paths without stacking transistors vertically, making them ideal for integrated circuit implementations.

Comparison Table

Table 2: Comparison Between Traditional Cascode and Folded Cascode (BJT)

Feature	**Traditional Cascode**	**Folded Cascode (BJT)**
Output Swing	Limited (due to $V_{CE,sat}$ stacking)	Extended (closer to rails)
Voltage Gain	Moderate	Higher (due to R_{out} increase)
Bias Control	Complex	Easier and more stable
Symmetry	Harder to maintain	Naturally symmetric
Voltage Headroom	Higher required	Lower required
Low-Voltage Operation	Less suitable	More suitable

Table 3: Operating Points

Transistor	I_C **(mA)**	**V**
Q1	0.11757	–
Q2	0.09779	–
Q3	0.28529	–
Q4	0.07449	–
Q5	0.07411	–
Q6	0.07372	–
Q7	0.07415	–
Q8	0.14983	–
Q9	0.0000106	–
Q10	0.10427	–
Q11	0.63312	–
Q12	0.21635	–
Q13	0.19889	–
Q14	0.21212	–
Q15	0.21506	–
Q16	0.19287	–
Q17	0.19248	–
Q18	0.19241	–
Q19	0.19241	–
Q20	0.21212	–
Q21	0.21212	–

The currents can be easily calculated using the concept of current mirror and its error.

I have specified the currents for each transistor, and calculating the voltages is not difficult either. Some of the transistors are diode-connected, so their voltages can be easily obtained, and the voltages of the remaining transistors can be derived based on those. However, since it was not requested, we have not performed this calculation.

Gain

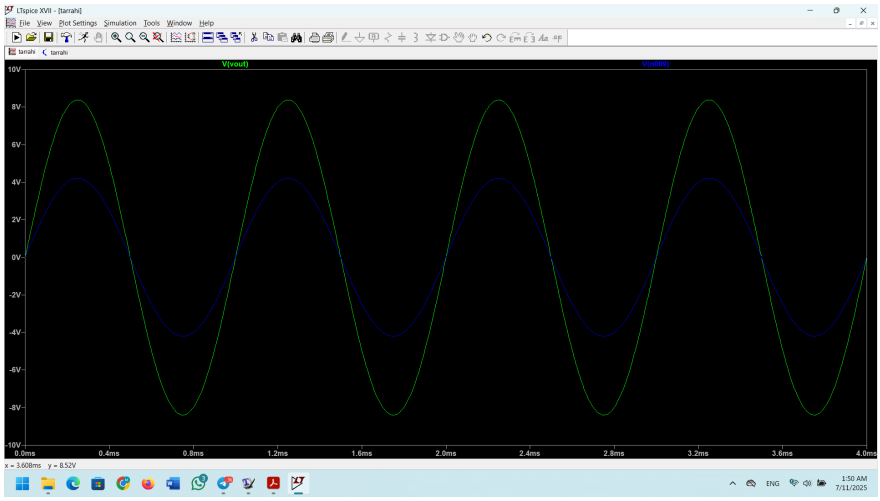

Figure 15: Gain=2

Swing

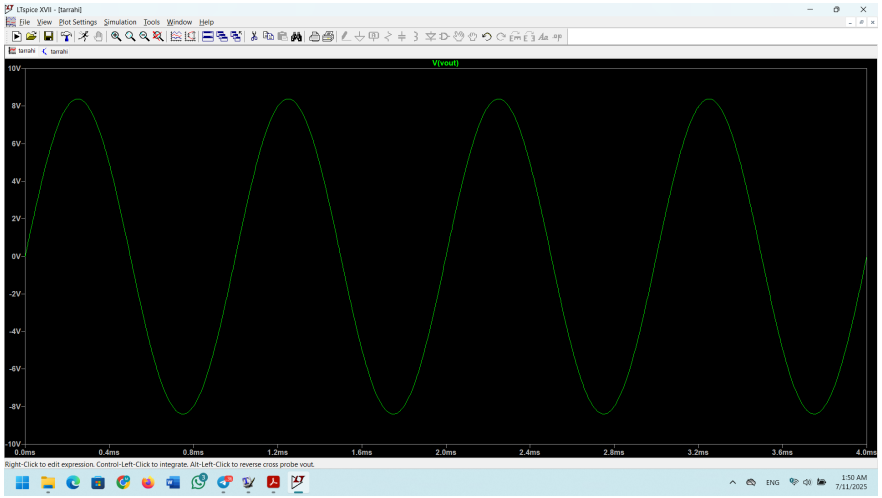

Figure 16: Symmetrical 8.2 V swing

Power

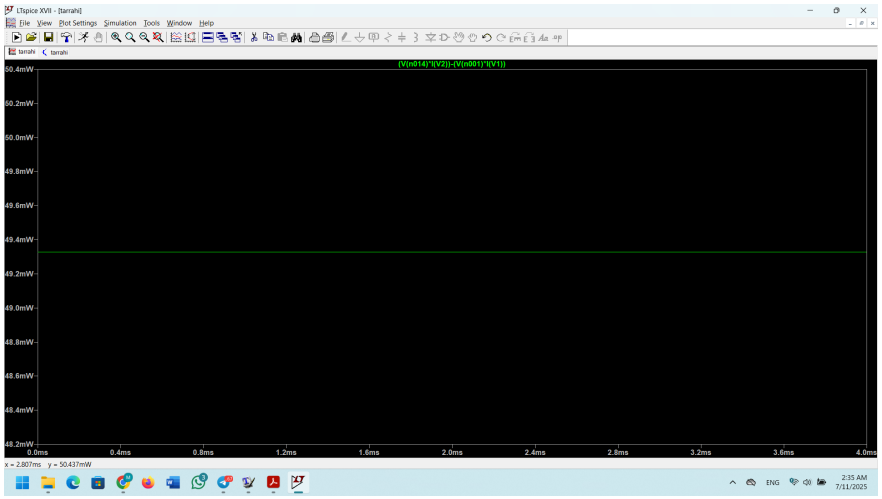

Figure 17: 49.33mW

THD

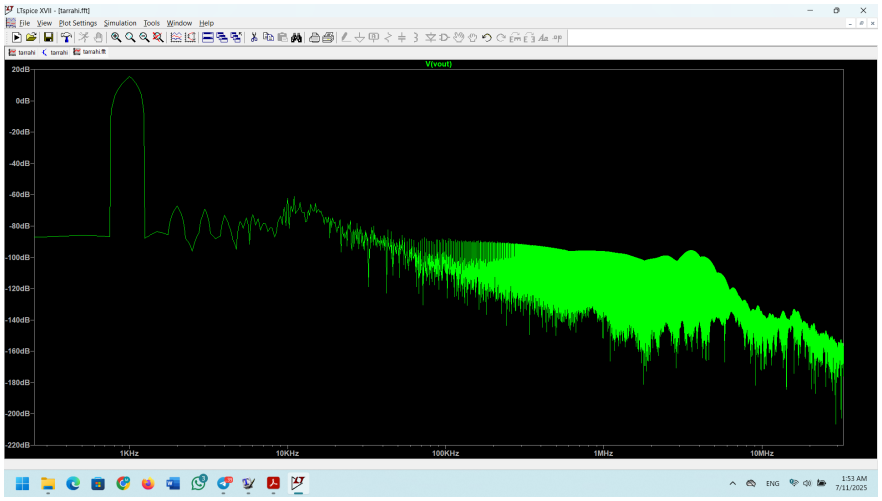

Figure 18: Fourier series coefficients

Given:

$$a_1 = 5.96, \quad a_2 = 0.00044, \quad a_3 = 0.00035, \quad a_4 = 0.00022$$

The Total Harmonic Distortion (THD) is calculated as:

$$\text{THD} = \frac{\sqrt{a_2^2 + a_3^2 + a_4^2}}{a_1}$$

Calculating the numerator:

$$\sqrt{(0.00044)^2 + (0.00035)^2 + (0.00022)^2} = \sqrt{1.936 \times 10^{-7} + 1.225 \times 10^{-7} + 4.84 \times 10^{-8}} = \sqrt{3.645 \times 10^{-7}} = 0.0006037$$

Therefore:

$$\text{THD} = \frac{0.0006037}{5.96} \approx 0.0001013 = 0.01013\%$$

Replacing the 10 kΩ resistor with a 50 kΩ resistor

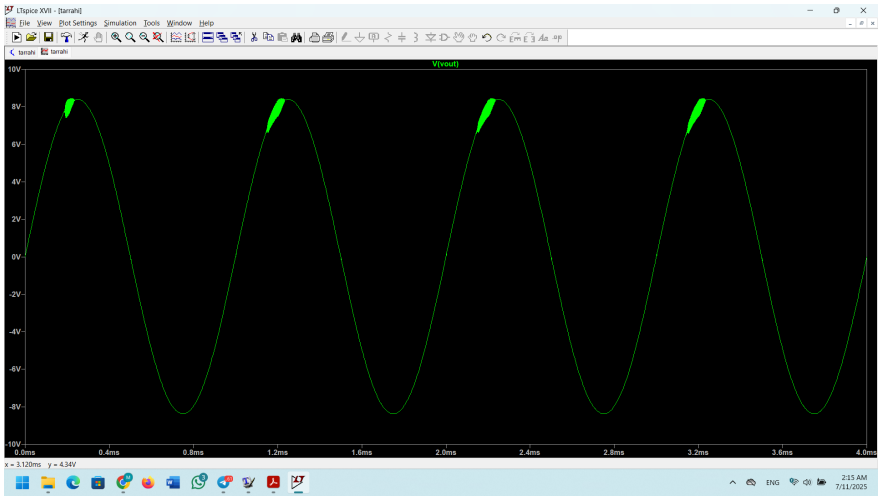

Figure 19: As anticipated, distortion occurs

If we replace the 10 kΩ resistors with 50 kΩ ones, the base of the transistor tends toward an open-circuit condition, and its voltage becomes undefined. This can lead to convergence issues in LTspice simulations and may result in distortion in the output voltage.

When a transistor's base is left in a high-impedance state due to large bias resistors, the base current becomes extremely small. As a result, the base-emitter voltage may not reach a stable or meaningful value. This makes the transistor's operating point unstable and can cause the DC operating point solver in LTspice (or other simulators) to fail to converge.

Moreover, in transient analysis, an undefined base voltage can lead to unpredictable switching behavior or improper linear region operation, which ultimately causes distortion in the output waveform.

To avoid these issues, it is recommended to use base bias resistors that ensure a reasonable bias current—typically on the order of tens to hundreds of microamperes—depending on the expected collector current and the specific transistor used.