Project Report for Electronic 2

Project Title: Differential amplifier

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Contents

1 Introduction

Design and Enhancement of a Differential Amplifier Using MOSFETs

Differential amplifiers are among the most important and widely used analog circuits, playing a crucial role in **signal processing systems, analog filters, operational circuits, and communication systems**. These amplifiers are widely utilized due to their ability to **reject common-mode noise and enhance the signal-to-noise ratio (SNR)**. One of their key advantages is their capability to **amplify the difference between two input signals while minimizing the effects of common-mode interference**.

In this project, the objective is to design and enhance a **differential amplifier based on MOSFET transistors**. The process is carried out in **four stages**, where in each step, key circuit parameters are analyzed and optimized. Initially, a **basic differential amplifier circuit** is designed and simulated to examine its primary characteristics, including **gain, bandwidth, input and output impedance**, and frequency response. In subsequent stages, by implementing **optimization techniques such as active loads, improved current sources, and cascode current mirrors**, the circuit performance is enhanced, increasing gain, improving input impedance, and reducing the effect of external noise.

One of the main challenges in designing this circuit is **managing common-mode gain while maximizing differential gain**. This will be optimized using various techniques, including **increasing the output resistance of current sources and employing more symmetrical structures**. Furthermore, through **AC analysis and frequency response evaluation**, the impact of each modification on the overall amplifier performance will be assessed.

At the conclusion of this project, different versions of the circuit will be compared to evaluate their performance improvements. **This project serves as an opportunity to gain a deeper understanding of analog circuit design concepts and the practical application of MOSFET transistors in amplifier circuits**. The expected results will provide valuable insights into designing more efficient circuits for future electronic systems.

2 Section One

Theoretical Calculation

$$Av_d = -g_m(r_o||R_D) \Rightarrow R_D \uparrow \Rightarrow Av_d \uparrow$$

$$V_{GS} \geq V_{th}$$

$$V_S = -0.8V, \quad V_G = 0$$

$$V_{GS} = 0.8V, \quad V_{th} = 0.6V$$

$$V_{DS} \geq V_{GS} - V_{th} \Rightarrow V_{DS} \geq 0.2V$$

$$V_D \geq -0.6V \Rightarrow V_{R_D} \leq 1.6V$$

$$R_D I_D \leq 1.6V$$

$$R_D = 3.2K\Omega$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

$$0.5 = \frac{1}{2} \times 0.25 \times \left(\frac{W}{L}\right) \times (0.2)^2$$

$$\Rightarrow \frac{W}{L} = 100$$

	M_1	M_2
I_D	0.5 mA	0.5 mA
V_{DS}	0.2 V	0.2 V
$r_o = \frac{1}{\lambda I_D}$	$40K$	$40K$

$$Av_d = -g_m(r_o||R_D)$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

$$g_m = \sqrt{2 \times 0.25 \times 100 \times 0.5} = 5m\frac{1}{\Omega}$$

$$Av_d = (-5m\frac{1}{\Omega})(2.96k\Omega) = -14.7$$

$Av_c = 0 \quad \Rightarrow \quad$ Because the current source is ideal, in AC mode the circuit is open

$$R_{in} = \infty$$

$$R_{out} = r_o||R_D = 40k\Omega||3.2k\Omega = 2.96k\Omega$$

$$V_{o_{max}} = 1V$$

$$V_{o_{min}} = V_{bias} = -0.4V$$

$$\text{Swing} = 0 \quad (P - P)$$

$$P = (V_{DD} - VSS)I_D = (1 - (-1))V \times 1mA = 2mW$$

$$\text{Upper limit} = 0V$$

$$\text{Lower limit} = -0.2V$$

$$\Rightarrow \quad CMR = 0.2V$$

Simulation results

First, we perform DC analysis, the results of which are as follows:

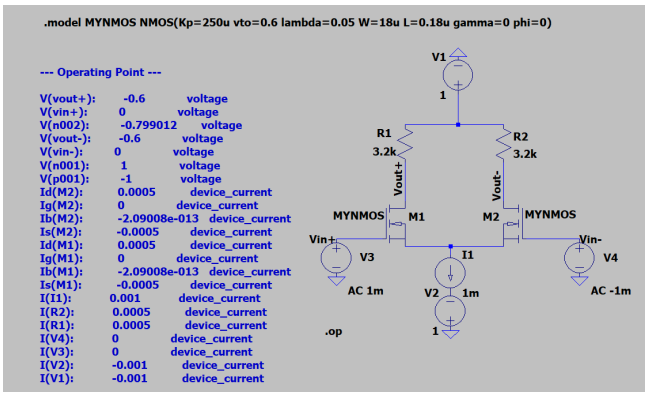

Figure 1: Circuit operating points with simulationt

Now we obtain the differential gain and common gain by simulation:

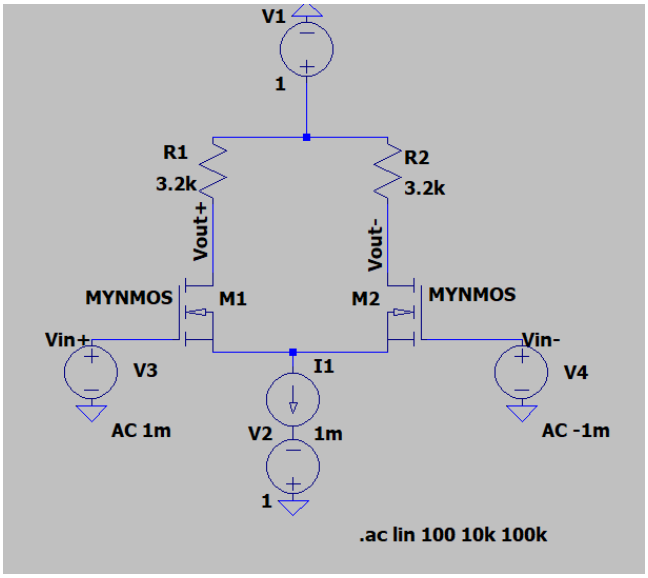

Figure 2: Circuit for obtaining differential gain

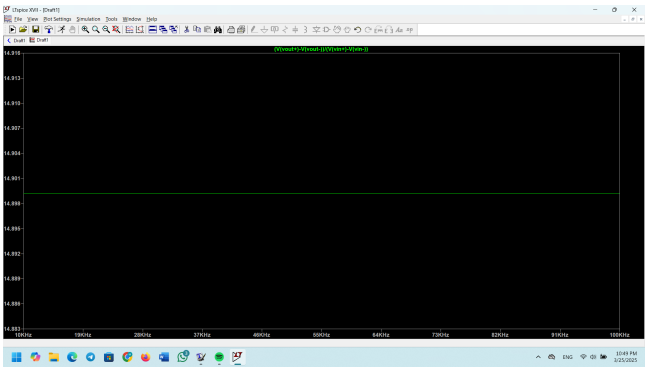

Figure 3: differential gain

In this step, we simulate the common gain:

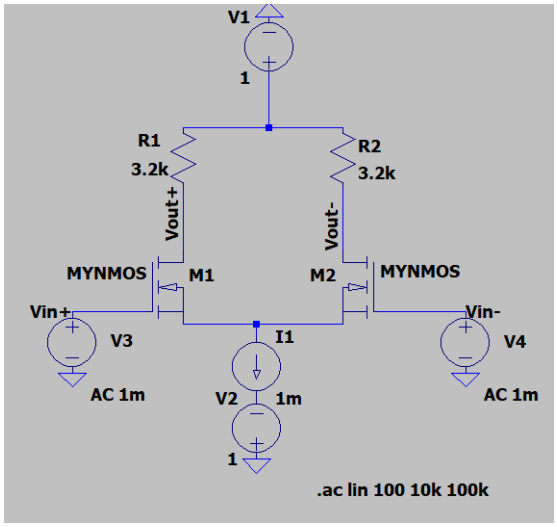

Figure 4: Circuit for obtaining common gain

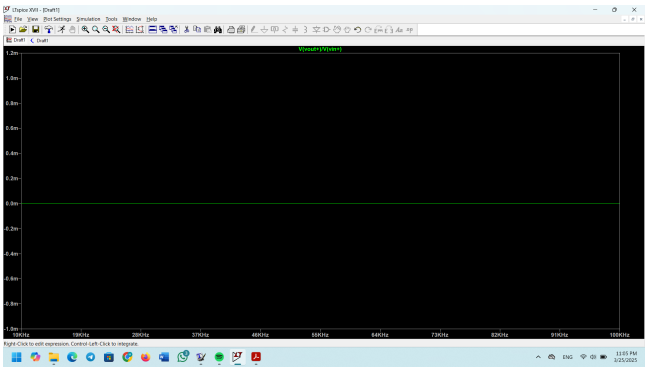

Figure 5: common gain(Due to the existence of an ideal current source)

we simulate the power consumption of the circuit:

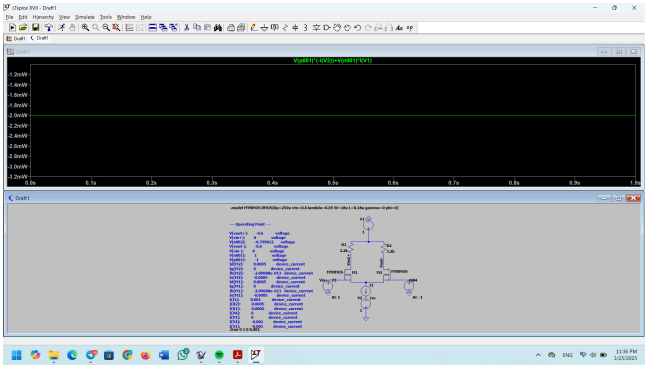

Figure 6: Circuit power

After calculating the differential gain and common gain, it is now time to calculate the input and output resistance:

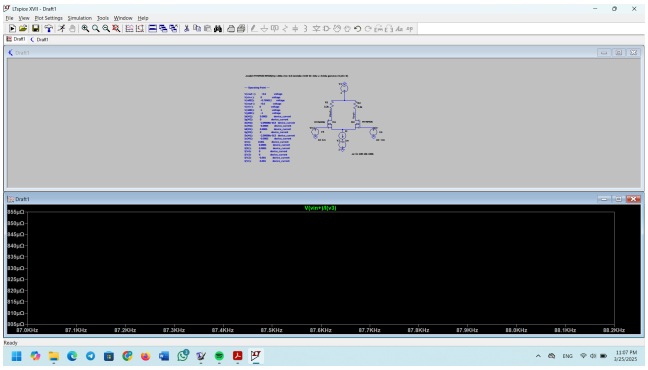

Figure 7: Input resistance (no number shown in the simulation because it is infinite, in fact because the source current is zero)

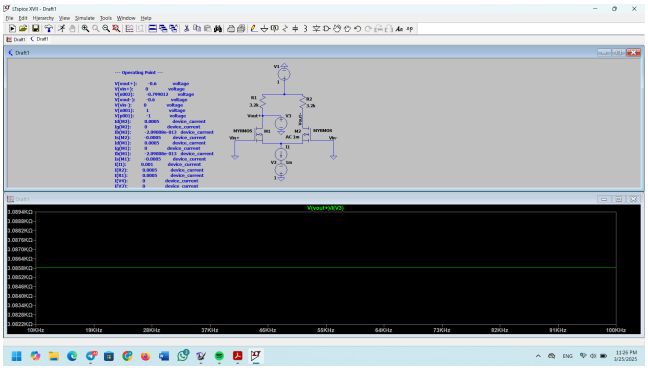

Figure 8: output resistance

It's time to simulate the swing. To calculate the swing, we consider the sources as sinusoids and increase their amplitude so that they are cut off from the top and bottom. In fact, this is how we understand the upper and lower limits:

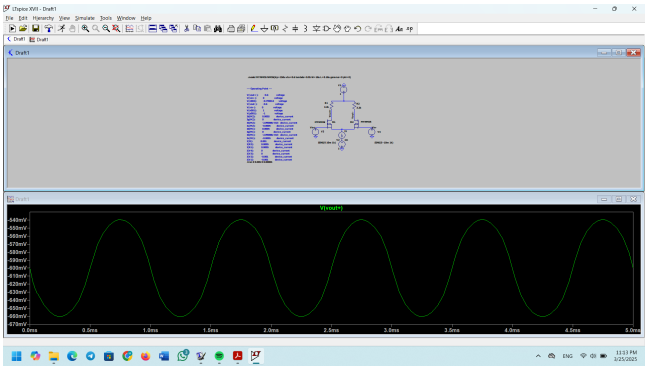

Figure 9: amplitude 10mV

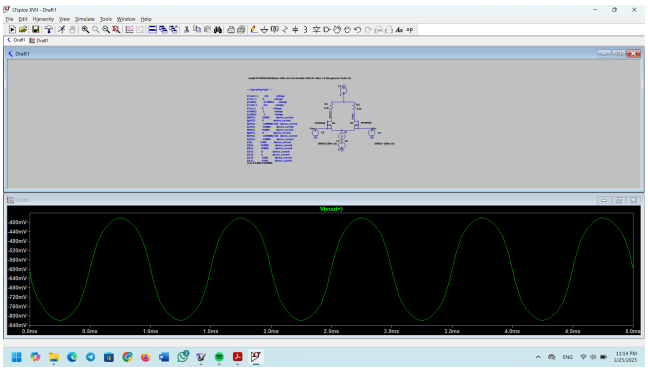

Figure 10: amplitude 100mV

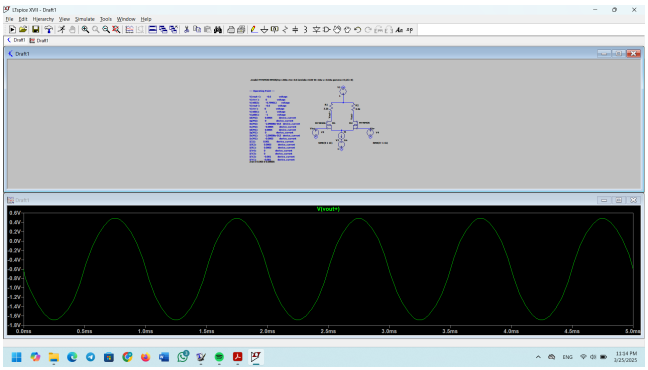

Figure 11: amplitude 1V

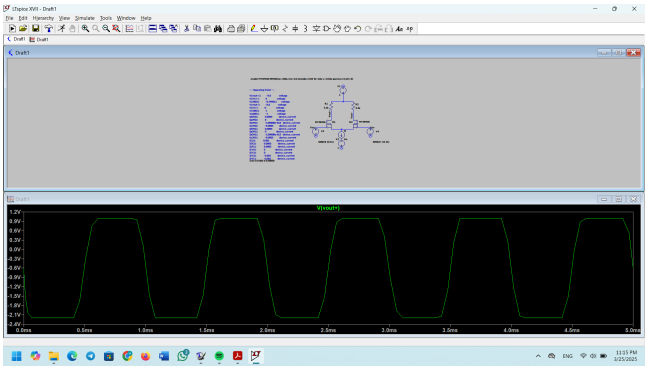

Figure 12: amplitude 10V

As can be seen, in this section, the theoretical calculations are consistent with the simulations, except for the lower swing limit, which is due to the ideal nature of the current source. The ideality of the current source causes our lower limit to not have a specific value and can decrease to any negative number.

3 Section Two

Theoretical Calculation

$$V_{DD} - V_D \geq V_{DD} - V_{b1} - V_{th}, \quad V_D - V_{S1} \geq V_{in} - V_{S1} - V_{th}$$
$$\Rightarrow V_{in} = 1.113V \Rightarrow V_D = 0.513V \Rightarrow V_{b1} = -0.087V$$
$$V_{in} = 0 \Rightarrow -0.6V \leq V_D \leq 0.513V$$

According to the course assistants, there is no need to calculate the third question.

$$\frac{W}{L} = 50$$
$$R_{in} = \infty$$
$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05 \times 0.0005} = 40k\Omega$$
$$r_{o_d} = r_o || 3r_0 = 30k\Omega$$
$$V_{o_{max}} = 1V, \quad V_{o_{min}} = -0.6V, \quad V_{bias} = 0.513V$$
$$\text{Swing} = 0.974V \quad (P - P)$$

$$P = (V_{DD} - VSS)I_D = (1 - (-1))V \times 1mA = 2mW$$
$$\text{Upper limit} = 1.113V$$
$$\text{Lower limit} = -0.12V$$
$$\Rightarrow \quad CMR = 1.125V$$

Simulation results

First, we perform DC analysis, the results of which are as follows:

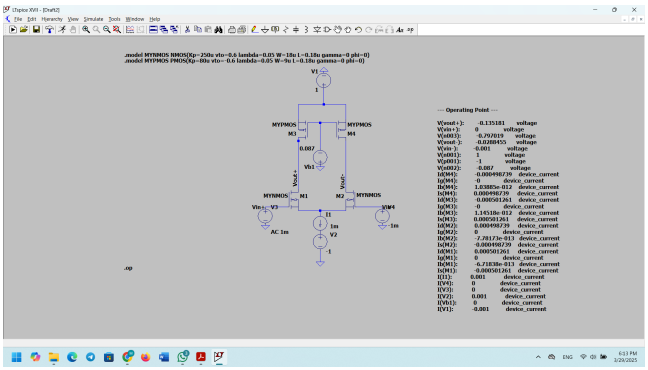

Figure 13: Circuit operating points with simulationt

Now we move on to simulating the input resistance and output resistance:

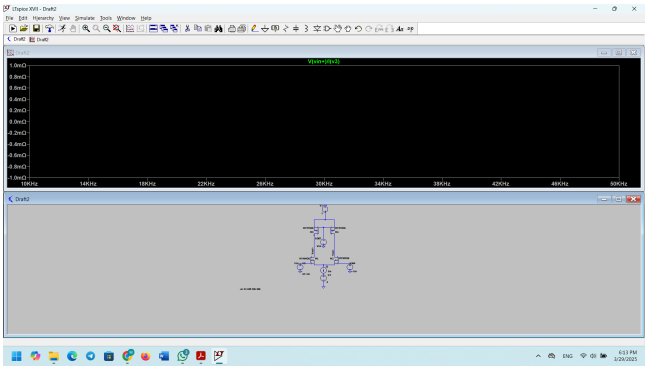

Figure 14: Input resistance (no number shown in the simulation because it is infinite, in fact because the source current is zero)

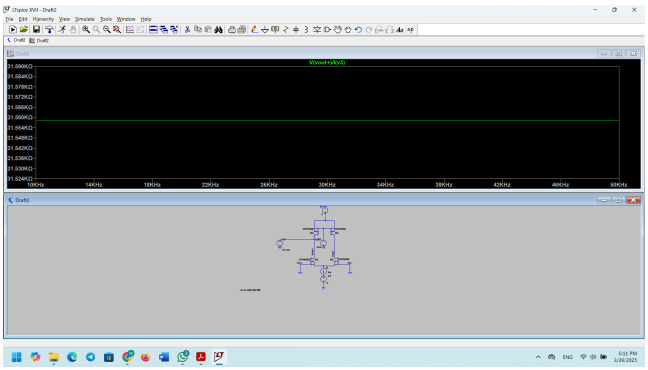

Figure 15: output resistance

we simulate the power consumption of the circuit:

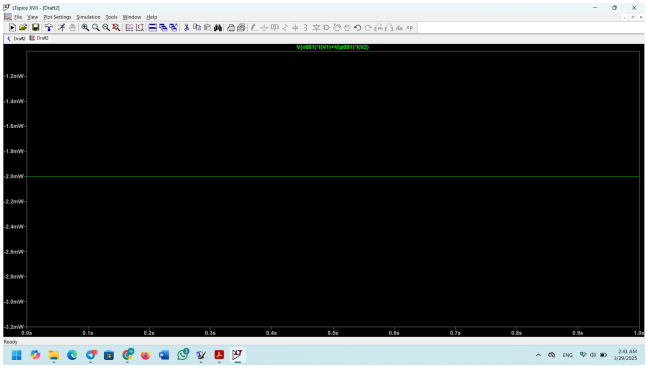

Figure 16: Circuit power

It's time to simulate the swing. To calculate the swing, we consider the sources as sinusoids and increase their amplitude so that they are cut off from the top and bottom. In fact, this is how we understand the upper and lower limits:

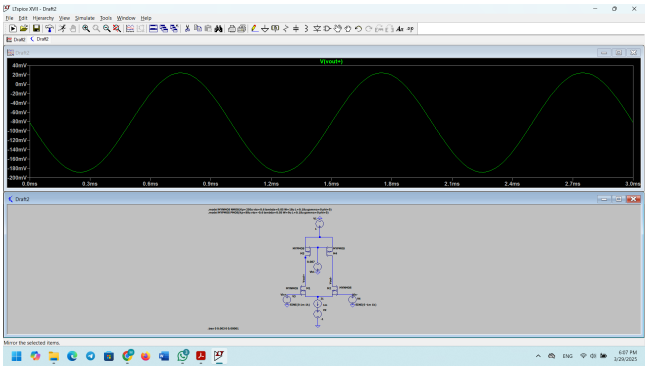

Figure 17: amplitude 1mV

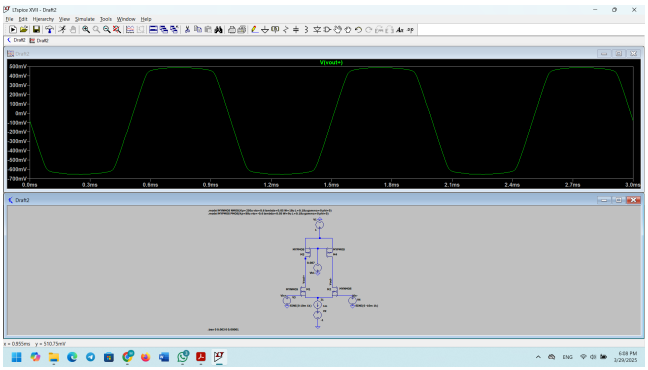

Figure 18: amplitude 10mV

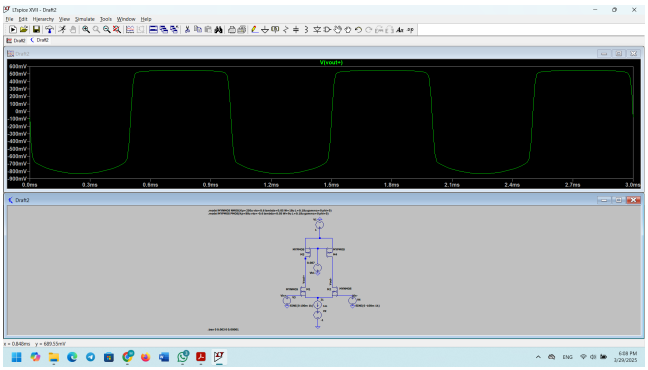

Figure 19: amplitude 100mV

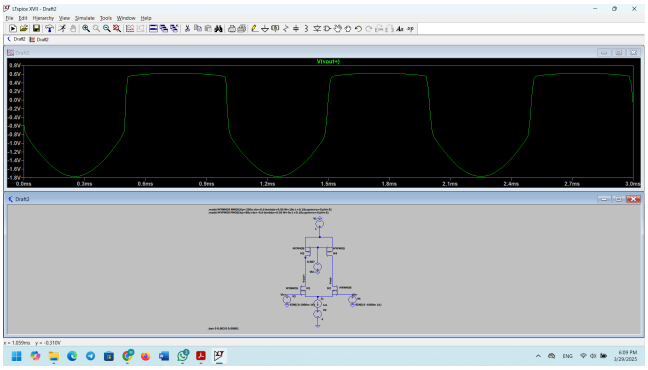

Figure 20: amplitude 1V

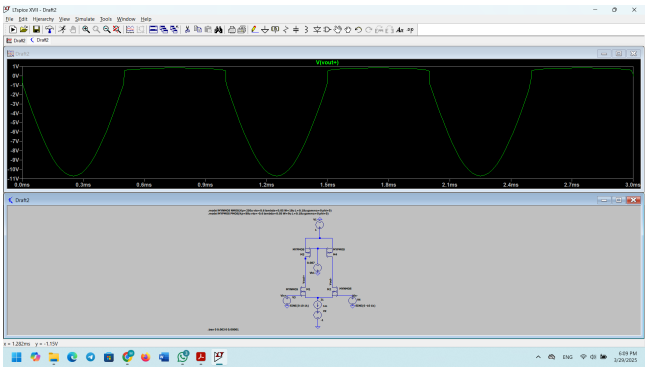

Figure 21: amplitude 10V

As we can see, in this section, the theoretical results are quite consistent with the simulations.Aside from the lower swing limit, the reason for which was explained in the previous section.

4 Section Three

Theoretical Calculation

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}| - |V_{th}|)^2$$

$$\text{for } M_3 \quad \Rightarrow \quad \frac{1}{2} = \frac{1}{2} \times 0.08 \times 50(|V_{GS}| - |V_{th}|)^2$$

$$\Rightarrow |V_{GS}| - |V_{th}| = 0.5V \quad \Rightarrow \quad V_{G_5} = -0.1V$$

$$\text{for } M_5 \quad \Rightarrow \quad 1 = \frac{1}{2} \times 0.08 \times \frac{W}{L} \times \frac{1}{4}$$

$$\Rightarrow \frac{W}{L} = 100$$

$$A_{v_d} = -g_m R_D \Rightarrow R_D = r_o$$

$$g_m = \sqrt{2\mu_p C_{ox}\frac{W}{L}I_D}$$

$$g_m = \sqrt{2 \times 0.08 \times 100 \times 0.5} = \sqrt{10}m\frac{1}{\Omega}$$

$$A_{v_d} = -3.16m\frac{1}{\Omega} \times 40k\Omega = -126.4$$

$$R_{in} = \infty$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05 \times 0.0005} = 40k\Omega$$

$$r_{o_d} = r_o||3r_0 = 30k\Omega$$

$$P = (2V_{DD} - VSS)I_D = (2 - (-1))V \times 1mA = 3mW$$

Simulation results

First, we perform DC analysis, the results of which are as follows:

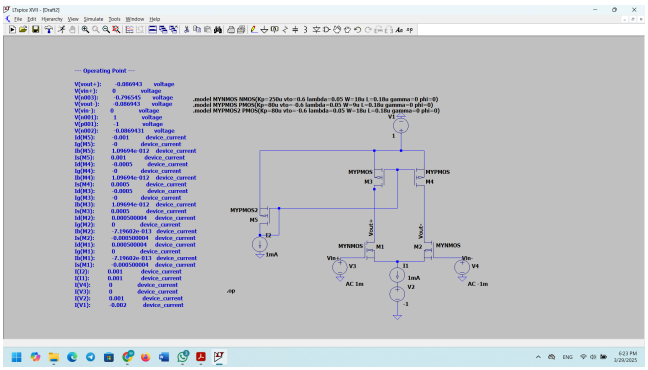

Figure 22: Circuit operating points with simulationt

Now we obtain the differential gain by simulation:

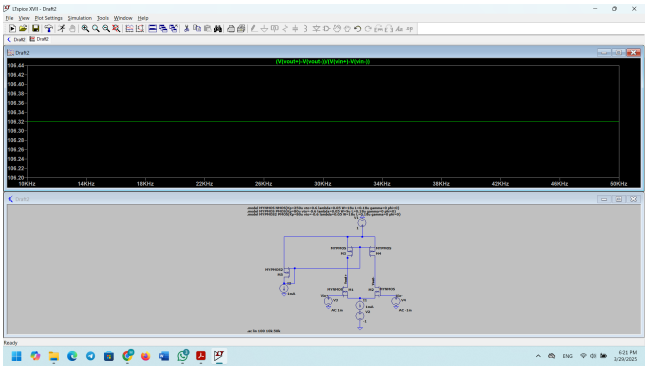

Figure 23: Circuit for obtaining differential gain

Now we move on to simulating the input resistance and output resistance:

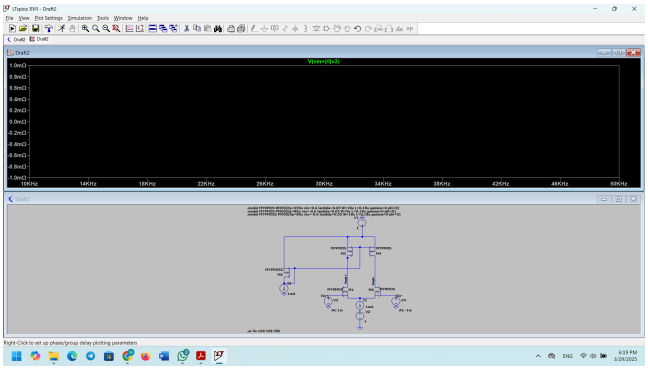

Figure 24: Input resistance (no number shown in the simulation because it is infinite, in fact because the source current is zero)

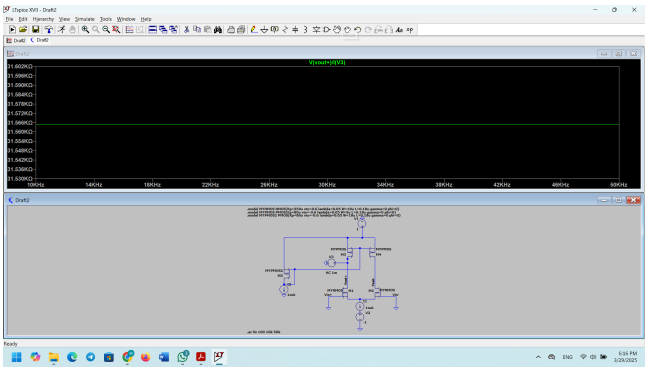

Figure 25: output resistance

And finally, we simulate the power consumption of the circuit:

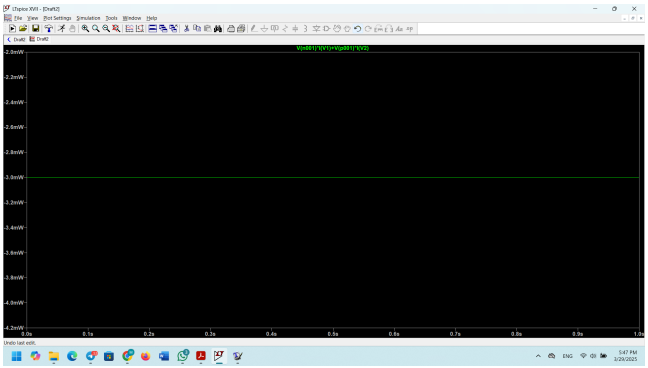

Figure 26: Circuit power

Question

What are the advantages and disadvantages of using an active load instead of a resistor in a differential amplifier?

Answer

In a differential amplifier, using an **active load** (such as an active current source) instead of a **resistor** significantly impacts circuit performance. Below are the advantages and disadvantages of this choice:

Advantages

- **Increased Voltage Gain:** The voltage gain of a differential amplifier is given by:

$$A_v = g_m R_{out}$$

  where g_m is the transistor transconductance and R_{out} is the load resistance. An active load provides a much higher R_{out} compared to a simple resistor, leading to a significantly higher gain.

- **Higher Output Impedance:** An active load typically behaves like a current source with very high impedance, which increases the output impedance of the circuit.

- **Lower Power Consumption:** Using an active load can reduce power consumption since it provides controlled current rather than dissipating power as a large resistor would.

- **Better Compatibility with CMOS Technology:** In integrated circuits (ICs), implementing large resistors is impractical, whereas using transistors as active loads is more space-efficient and compatible with semiconductor fabrication processes.

Disadvantages

- **Increased Design Complexity:** Designing an active load (such as a current mirror) requires careful transistor selection, biasing, and stability considerations.
- **Dependence on Transistor Parameters:** The behavior of an active load depends on transistor parameters (e.g., V_{BE} or V_{GS}, β, λ), which may vary with temperature and manufacturing processes.
- **Higher Noise and Distortion:** Some active load configurations may introduce additional noise or distortion into the signal.
- **Reduced Circuit Stability:** The high impedance of an active load may lead to instability at high frequencies, requiring frequency compensation.

Conclusion

If high gain and CMOS compatibility are required, an active load is the preferred choice. However, if circuit simplicity and stability are more critical, using a resistor might be a better option.

As we can see, in this section, the theoretical results are quite consistent with the simulations.

5 Section Four

Theoretical Calculation

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}| - |V_{th}|)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

$$\text{for } M_5 \quad \Rightarrow \quad 1 = \frac{1}{2} \times 0.08 \times 100(|V_{GS}| - |V_{th}|)^2$$

$$\Rightarrow |V_{GS}| - |V_{th}| = 0.5V \quad \Rightarrow \quad V_{G_5} = -0.1V = V_{D_5}$$

$$\text{for } M_6 \quad \Rightarrow \quad 1 = \frac{1}{2} \times 0.25 \times 280(V_{GS} - V_{th})^2$$

$$\Rightarrow V_{GS} - V_{th} = 0.169V \quad \Rightarrow \quad V_{G_6} = -0.231V = V_{D_6}$$

$$V_{R_x} = I_D R_x = 0.131V \Rightarrow R_x = 0.131k\Omega$$

$$\text{for } M_7 \quad \Rightarrow \quad 1 = \frac{1}{2} \times 0.25 \times \frac{W}{L} \times \frac{8}{280}$$

$$\Rightarrow \frac{W}{L} = 280$$

$$A_{v_d} = -g_m R_D \Rightarrow R_D = r_o$$

because ...

$$g_m = \sqrt{2\mu_p C_{ox}\frac{W}{L}I_D}$$

$$g_m = \sqrt{2 \times 0.08 \times 100 \times 0.5} = \sqrt{10}m\frac{1}{\Omega}$$

$$A_{v_d} = -3.16m\frac{1}{\Omega} \times 40k\Omega = -126.4$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05 \times 0.0005} = 40k\Omega$$

$$r_{o_2} = \frac{1}{\lambda I_D} = \frac{1}{0.05 \times 0.001} = 20k\Omega$$

$$A_{v_c} = \frac{-R_D}{R_S + \frac{1}{g_m}} \Rightarrow R_S = 2r_{o_2} \Rightarrow A_{v_c} = \frac{-40k\Omega}{40k\Omega + 0.316k\Omega} = 0.992$$

$$R_{in} = \infty$$

$$r_{o_d} = r_o||3r_o = 30k\Omega$$

$$r_{o_c} = r_o||(r_o + 2r_{0_2}) = \frac{80}{3}k\Omega$$

$$P = (2(V_{DD} - VSS))I_D = (2(1 - (-1)))V \times 1mA = 4mW$$

Simulation results

First, we perform DC analysis, the results of which are as follows: Now we move

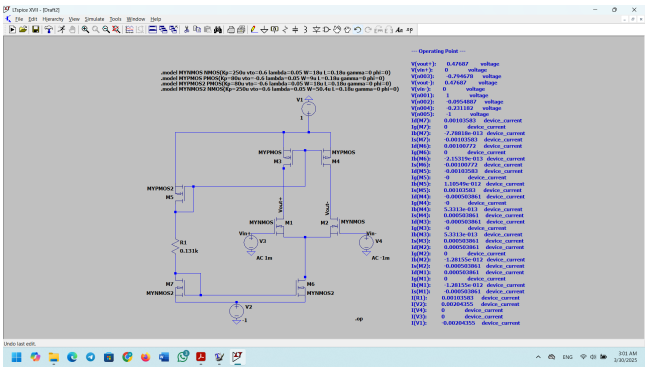

Figure 27: Circuit operating points with simulationt

on to the differential and common gain simulation:

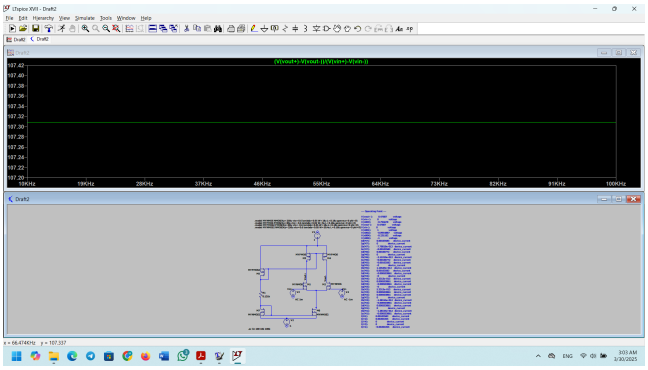

Figure 28: differential gain

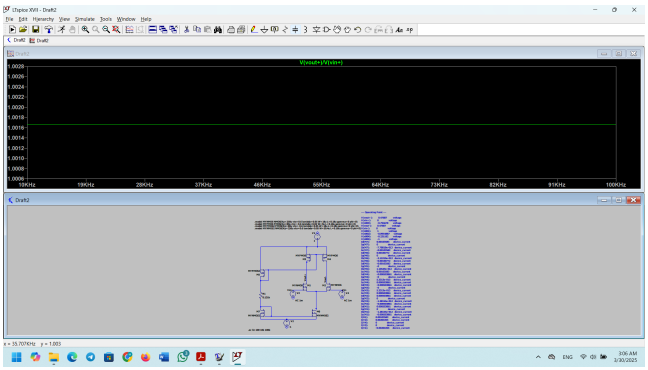

Figure 29: common gain

Now we move on to simulating the input resistance and output resistance:

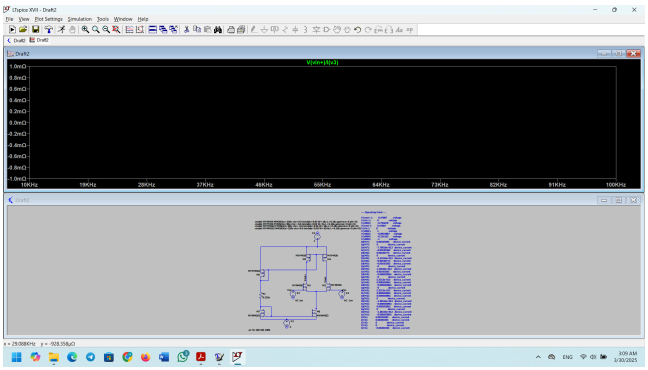

Figure 30: Input resistance (no number shown in the simulation because it is infinite, in fact because the source current is zero)

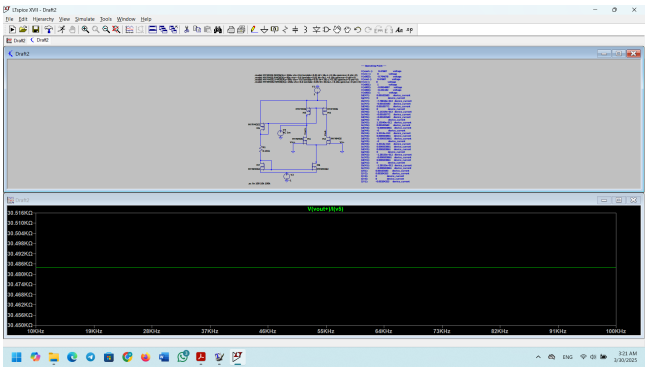

Figure 31: output resistance

And finally, we simulate the power consumption of the circuit:

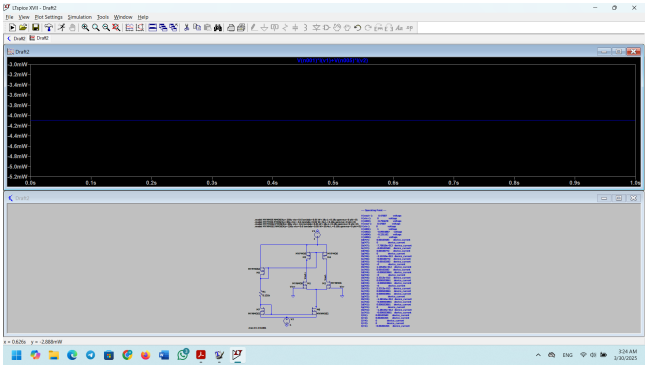

Figure 32: Circuit power

Question

Ultimately, it is observed that despite the good differential gain provided by this circuit, the common-mode gain has significantly increased compared to the case where an ideal current source was used, which is undesirable. Assuming that all transistors remain in saturation, explain how we can make a slight modification to the circuit to reduce the common-mode gain.

Answer

In this circuit, an **ideal current source** is used to bias the differential amplifier, which is provided by transistor M_7. This current source increases the **differential gain** of the circuit, but at the same time, the **common-mode gain** has also increased, which can be problematic.

How to Reduce Common-Mode Gain?

The common-mode gain arises when both inputs of the circuit (i.e., V_{in1} and V_{in2}) experience the same voltage variation, causing the output to respond accordingly. The following methods can be used to reduce this effect:

1. **Increase the Output Impedance of the Current Source (M_7):**
   - Keeping M_7 in the saturation region and **increasing the channel length (L)** will increase its output impedance. This increased impedance makes the current source behave more ideally, reducing the common-mode gain.
2. **Use a Current Mirror Instead of a Single Transistor for the Current Source:**
   - Replacing M_7 with a **cascode current mirror** increases the output resistance of the current source, thereby reducing the common-mode gain.
3. **Add a Capacitor Between the Source of M_7 and Ground (V_{SS}):**
   - Adding a **bypass capacitor** helps suppress voltage variations at the common-mode node, thereby reducing the common-mode gain.
4. **Balance the Input Resistances (If Possible):**
   - Adjusting the input resistances to balance common-mode noise effects can help in reducing the common-mode gain.

Conclusion

To reduce the common-mode gain in this circuit, the best approaches include **increasing the impedance of the current source, using a cascode current mirror, adding a bypass capacitor, and balancing the input resistances**. These modifications make the circuit less sensitive to common-mode noise while maintaining differential gain.