

**DESIGN AND ANALYSIS OF AN AREA EFFICIENT AND LOW
POWER VCO BASED ADC FOR BIOMEDICAL APPLICATIONS**

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B.Sc. ENGINEERING THESIS



**DEPARTMENT OF ELECTRICAL, ELECTRONIC AND
COMMUNICATION ENGINEERING
MILITARY INSTITUTE OF SCIENCE AND TECHNOLOGY
DHAKA, BANGLADESH**

MAY 2025

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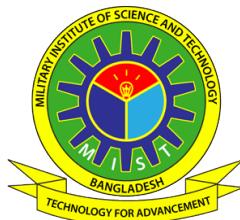
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**A Thesis Submitted in Partial Fulfillment of the Requirements for the
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Communication Engineering**



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DECLARATION

I hereby declare that the study reported in this thesis entitled as above is my own original work and has not been submitted before anywhere for any degree or other purposes. Further, I certify that the intellectual content of this thesis is the product of my own work and that all the assistance received in preparing this thesis and sources have been acknowledged and cited in the reference section.

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Dedicated to my parents for supporting and encouraging
me to believe in myself.

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ABSTRACT

DESIGN AND ANALYSIS OF AN AREA EFFICIENT AND LOW POWER VCO BASED ADC FOR BIOMEDICAL APPLICATIONS

This thesis focuses on the development of compact and power efficient VCO based ADC for implantable biomedical devices. Voltage-Controlled Oscillator (VCO)-based ADCs offer a promising avenue for these applications due to their inherent compatibility with scaled CMOS technologies and digital-friendly operation, though achieving high linearity and low phase noise remains challenging. This thesis details the design, comprehensive analysis, and post-layout verification of an area-efficient, low-power 4-bit VCO-based ADC tailored for biomedical applications, implemented in 90nm CMOS technology. The core of the converter is a novel five-stage current-starved ring oscillator (CSRO) which incorporates a diode-connected NMOS source degeneration technique to enhance voltage-to-frequency (V-F) linearity and an embedded charge pump mechanism within alternating delay stages to mitigate phase noise. Post-layout simulations demonstrate the VCO's robust performance under a 1.8V supply, achieving a wide tuning range from 38 MHz to 619 MHz (93.86%) for control voltages between 0.53V and 1.6V. It exhibits a phase noise of -88.63 dBc/Hz at a 1MHz offset from a 323 MHz carrier, while consuming 354.6 μ W. This translates to a Figure of Merit (FOM) of -141.15 dBc/Hz within a compact layout area of 292.94 μ m². The ADC architecture further employs a Frequency-to-Digital Converter (FDC) stage, for which both asynchronous (ripple) and synchronous 4-bit counter implementations, along with a D-Flip-Flop based output register, were designed and comparatively evaluated. The complete 4-bit ADC system utilizing the synchronous counter demonstrates superior dynamic performance, achieving an Effective Number of Bits (ENOB) of 3.64 bits (600KHz) and more better at lower frequency. Static characterization reveals a Differential Non-Linearity (DNL) within ± 0.6 LSB and an Integral Non-Linearity (INL) between -0.04 and +0.72 LSB, ensuring monotonicity. The overall ADC consumes 328.3 μ W, resulting in an FOM of 0.642 pJ/Conversion-step. Extensive simulations, including process, voltage, and temperature (PVT) variations and Monte Carlo analyses, validate the design's functionality and robustness. The comparative investigation of FDC architectures provides crucial insights for optimizing performance based on specific application priorities.

সারসংক্ষেপ

DESIGN AND ANALYSIS OF AN AREA EFFICIENT AND LOW POWER VCO BASED ADC FOR BIOMEDICAL APPLICATIONS

এই থিসিসটি ইমপ্লান্টেবল বায়োমেডিক্যাল ডিভাইসের জন্য কম্প্যাক্ট এবং বিদ্যুৎ-সাশ্রয়ী VCO ভিত্তিক ADC উন্নয়নে কেন্দ্রিত। ভোল্টেজ-কন্ট্রোল অসিলেটর (VCO) ভিত্তিক ADC গুণগতভাবে CMOS প্রযুক্তির সাথে স্বাভাবিক সামঞ্জস্য এবং ডিজিটাল-ফ্রেন্ডলি অপারেশনের কারণে এই ধরনের অ্যাপ্লিকেশনের জন্য একটি সন্তোষজনক পথ প্রদান করে, যদিও উচ্চ লিনিয়ারিটি এবং কম ফেজ নয়েজ অর্জন করা চালেঙ্গ। এই থিসিসে ৯০ ন্যানোমিটার CMOS প্রযুক্তিতে বাস্তবায়িত, বায়োমেডিক্যাল অ্যাপ্লিকেশনের জন্য বিশেষভাবে তৈরি একটি এরিয়া-সাশ্রয়ী ও কম শক্তি খরচকারী 8-বিট VCO ভিত্তিক ADC-এর ডিজাইন, বিস্তারিত বিশ্লেষণ এবং পোস্ট-লে-আউট যাচাই তুলে ধরা হয়েছে। কনভার্টারের মূল অংশ হিসেবে ব্যবহৃত হয়েছে একটি নতুন পাঁচ-স্টেজ কারেন্ট-স্টার্ভড রিং অসিলেটর (CSRO), যা ভোল্টেজ-টু-ফ্রিকোয়েন্সি (V-F) লিনিয়ারিটি বাড়ানোর জন্য বায়াস-কানেক্টেড NMOS কারেন্ট মিনিমাইজেশন প্রযুক্তি এবং ফেজ নয়েজ কমানোর জন্য অপারেটিং সিগন্যাল কারেন্টগুলোর মধ্যে অ্যাস্টিভ চার্জ পাস্প মেকানিজম অন্তর্ভুক্ত করে। পোস্ট-লে-আউট সিমুলেশন অনুযায়ী, ১.৮ ভোল্ট সাপ্লাইয়ে এই VCO শক্তিশালী পারফরম্যান্স প্রদর্শন করে: ০.৫২ থেকে ১.৬ ভোল্টের মধ্যে ভোল্টেজের মাধ্যমে ৩৮ MHz থেকে ৬১৯ MHz পর্যন্ত বিস্তৃত টিউনিং রেঞ্জ (৯৩.৮৬%) অর্জন করে। এটি ৩২৩ MHz ক্যারিয়ারে ১ MHz অফসেটে -৮৮.৬৩ dBc/Hz ফেজ নয়েজ এবং ৩৫৪.৬ মাইক্রোওয়াট শক্তি খরচ প্রদর্শন করে, যা ২৯২.৯৪ মাইক্রোমিটার বর্গের কোর লেআউট এরিয়াতে -১৪১.১৫ dBc/Hz এর চমৎকার ফিগার অফ মেরিট (FOM) প্রদান করে। ADC আর্কিটেকচারে ফ্রিকোয়েন্সি-টু-ডিজিটাল কনভার্টার (FDC) ধাপ অন্তর্ভুক্ত রয়েছে, যেখানে অ্যাসিঙ্ক্রোনাস (রিপল) ও সিনক্রেনাস 8-বিট কাউন্টার এবং D-ফ্লিপ-ফ্লপ ভিত্তিক আউটপুট রেজিস্টারের ডিজাইন ও তুলনামূলক মূল্যায়ন করা হয়েছে। সিনক্রেনাস কাউন্টার ব্যবহার করে প্রস্তাবিত 8-বিট ADC সিস্টেম ইনপুট সিগন্যালে ৮০০ kHz পর্যন্ত ইফেক্টিভ নাম্বার অফ বিটস (ENOB) ৩.৬৪ বিট অর্জন করে উচ্চ গতিশীলতা প্রদর্শন করে। স্ট্যাটিক ক্যারেন্টারাইজেশনে ± 0.6 LSB এর মধ্যে ডিফারেনশিয়াল নন-লিনিয়ারিটি (DNL) এবং -0.08 থেকে +0.72 LSB এর মধ্যে ইন্টিগ্রাল নন-লিনিয়ারিটি (INL) নিশ্চিত করে মনোযোগযোগ্য স্থিতিশীলতা। সমগ্র ADC-র শক্তি খরচ ৩২৮.৩ মাইক্রোওয়াট এবং FOM ০.৬৪২ pJ/কনভার্সন-স্টেপ। প্রসেস, ভোল্টেজ এবং তাপমাত্রার (PVT) পরিবর্তন এবং মটে কার্লো সিমুলেশনের মাধ্যমে ব্যাপকভাবে ডিজাইনের কার্যকারিতা ও মজবুততা যাচাই করা হয়েছে। FDC আর্কিটেকচারের তুলনামূলক গবেষণা নির্দিষ্ট অ্যাপ্লিকেশন অগ্রাধিকার অনুসারে ভবিষ্যৎ পারফরম্যান্স অপটিমাইজেশনের গুরুত্বপূর্ণ দিক-নির্দেশনা প্রদান করে।

LIST OF NOTATIONS

V_{in}	Analog input voltage to the ADC
V_{ctrl}, V_{con}	Control voltage for the VCO
V_{DD}	Supply voltage
V_{TH}, V_t	Threshold voltage of a transistor
V_{SP}	Inverter's switching threshold voltage
V_{FS}	Full-scale voltage of the ADC
V_{out}	Output voltage (general)
D_{out}	Multi-bit digital output of the ADC
f_{osc}, f_{VCO}	Oscillation frequency of the VCO
Φ_1, F_{out}	Alternative notations for VCO output frequency
ω_0	Oscillation angular frequency ($\omega_0 = 2\pi f_{osc}$)
T_{period}	Oscillation period of the VCO ($T_{period} = 1/f_{osc}$)
t_d, t_{delay}	Propagation delay per inverter stage in the VCO
t_{LH}	Low-to-high transition time of a stage
t_{HL}	High-to-low transition time of a stage
N_{stages}	Number of stages in the ring oscillator
$C_{tot}, C_{L,total}$	Total load capacitance at an inverter output node
C'_{ox}, C_{ox}	Gate oxide capacitance per unit area
C_L	Load capacitance (general)
C_{par}	Parasitic capacitance
C_{ext}	External capacitance
W_p, L_p	Width and length of a PMOS transistor
W_n, L_n	Width and length of an NMOS transistor
(W/L)	Aspect ratio of a transistor
I_D	Net current through an inverter stage / Drain current
$I_{D,charge}$	Starved current available for charging
$I_{D,discharge}$	Starved current available for discharging
I_{REF}	Reference current in a current mirror
I_{out}	Output current from a current mirror
I_{bias}	Bias current
I_p	Charge pump current / Bias current in pump stages
I_{CP}	Injected current from charge pump

μ_n, μ_p, μ	Carrier mobility (electron, hole, general)
β	Device transconductance parameter ($\frac{1}{2}\mu C_{ox} \frac{W}{L}$)
$\mathcal{L}(\Delta\omega), \mathcal{L}(\Delta f)$	Single-sideband phase noise density at offset frequency $\Delta\omega$ (rad/s) or Δf (Hz)
F	Noise factor of active devices (in phase noise context)
T_{temp}	Absolute temperature
P_{sig}, P_s	Oscillator's signal power
Q_{factor}	Loaded quality factor of a resonator (in phase noise context)
ω_c, W_c	Flicker-noise (1/f noise) corner frequency
$\Delta\omega, \Delta f$	Offset frequency from the carrier (rad/s or Hz)
$\Gamma(\theta)$	Impulse Sensitivity Function (ISF)
θ	Oscillation phase
$\sigma_{\phi, rms}^2$	RMS phase deviation squared (variance of phase jitter)
$\sigma_{\tau, rms}$	RMS timing jitter
K_{VCO}	VCO sensitivity or gain (e.g., Hz/V)
$S_\phi(f)$	Phase noise spectral density
$S_{V_{ctrl}}(f)$	Noise spectral density of the control voltage
T_s, T_{meas}	Sampling interval or measurement time for FDC
N_{bits}	Number of bits (resolution of ADC or counter)
Q	Output of a flip-flop (e.g., Q_A, Q_B, \dots)
\bar{Q}	Complemented output of a flip-flop
D	Data input of a D-flip-flop (e.g., D_A, D_B, \dots)
Δ	Quantization step size (LSB value)
$x(t)$	True (analog) signal
$x_q(t)$	Quantized version of the signal
$e(t)$	Quantization error ($e(t) = x_q(t) - x(t)$)
σ_q^2	Quantization noise power
M_{OSR}	Oversampling factor/ratio

LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
AFE	Analogue Front End
AI	Artificial Intelligence
BMI	Brain-Machine Interface
CLF	Loop-Filter Capacitance
CLK	Clock Signal
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
CNT	Counter
CS	Common Source (for CS Stage); Current-Starved (for CS-VCO)
CSRO	Current-Starved Ring Oscillator
CSRVCO	Current-Starved Ring Voltage-Controlled Oscillator
CSVCO	Current-Starved Voltage-Controlled Oscillator
dB	Decibel
dBc	Decibels relative to carrier
dBc/Hz	Decibels relative to carrier per Hertz
dBFS	Decibels relative to Full Scale
DC	Direct Current
DFF, D-FF	D-type Flip-Flop (Delay Flip-Flop)
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
FDC	Frequency-to-Digital Converter
FF	Fast PMOS, Fast NMOS (Process Corner)
FFT	Fast Fourier Transform
FOM	Figure of Merit
FS	Fast PMOS, Slow NMOS (Process Corner)
IA	Instrumentation Amplifier
IC	Integrated Circuit
INL	Integral Non-Linearity
IoT	Internet of Things
ISF	Impulse Sensitivity Function

LSB	Least Significant Bit
LTV	Linear Time-Varying
MSB	Most Significant Bit
N-bit CNT	N-bit Counter
NMOS	N-channel Metal-Oxide-Semiconductor
OSR	Oversampling Ratio
PGA	Programmable Gain Amplifier
pJ/Conv.step	picoJoules per Conversion step
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide-Semiconductor
PPG	Photoplethysmography
PSRR	Power Supply Rejection Ratio
PSS	Periodic Steady State
PVT	Process, Voltage, and Temperature
PWV	Pulse Wave Velocity
REG	Register
RMS	Root Mean Square
SF	Slow PMOS, Fast NMOS (Process Corner)
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise and Distortion Ratio (also SNDR)
SNDR	Signal-to-Noise and Distortion Ratio (also SINAD)
SNR	Signal-to-Noise Ratio
SS	Slow PMOS, Slow NMOS (Process Corner)
Std Dev	Standard Deviation
THD	Total Harmonic Distortion
ULV	Ultra-Low-Voltage
VCO	Voltage-Controlled Oscillator
VFC	Voltage-to-Frequency Converter

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Analog-to-Digital Converters (ADCs) are essential components bridging the analog physical world and digital processing systems, enabling diverse applications from communication to biomedical instrumentation [1]. The ongoing miniaturization and power efficiency demands, particularly for wearable and implantable devices, have driven the evolution of ADC architectures that balance low power consumption with acceptable accuracy and speed[2, 3]. Among these, Voltage-Controlled Oscillator (VCO)-based ADCs have emerged as a compelling solution due to their inherent compatibility with modern CMOS scaling and favorable power-area trade-offs[4, 5].

The core concept of a VCO-based ADC is to translate the input analog voltage into a frequency-modulated signal through a Voltage-Controlled Oscillator. This time-domain representation allows the analog information to be processed by digital counting circuits, effectively converting voltage into a digital code with relatively simple hardware. This approach contrasts with traditional voltage-domain ADCs, which often rely on complex comparator trees and precise analog components, thereby increasing power consumption and chip area [6]. The frequency-to-digital conversion strategy, therefore, lends itself to efficient, compact, and scalable designs suitable for integration into sensor front-ends requiring ultra-low power, such as Photoplethysmography (PPG) and Brain-Machine Interface (BMI) systems.

Historically, VCO-based ADCs leverage ring oscillators, especially Current-Starved Ring Oscillators (CSROs), for their wide tuning range and ease of CMOS implementation[7]. These oscillators control frequency by modulating the current available to their delay stages, thereby adjusting oscillation frequency in response to input voltage variations. However, conven-

tional CSROs face inherent challenges including non-linear voltage-to-frequency conversion characteristics, phase noise limitations, and susceptibility to environmental variations, all of which degrade the effective resolution and performance of the ADC [8]. Various circuit-level techniques have been explored to mitigate these drawbacks, such as source degeneration and charge pump integration, aimed at improving linearity and reducing phase noise [9].

Complementing the VCO is the Frequency-to-Digital Converter (FDC), responsible for quantifying the frequency output into a digital word. The FDC typically includes a counter and output register, which count oscillator cycles over a defined time window. The design of the FDC must carefully consider resolution, speed, and power, as well as synchronization and quantization noise, to maintain overall ADC accuracy.

This thesis focuses on developing a compact and power-efficient 4-bit VCO-based ADC architecture that addresses the fundamental limitations of conventional designs. By improving VCO linearity and phase noise performance at the circuit level, and by analyzing different FDC counter architectures, this work aims to enhance the effective resolution and robustness of VCO-based ADCs for biomedical applications.

1.1.1 ADC Architecture

The VCO-based ADC architecture employed in this work follows a two-stage conversion process. Initially, the analog input voltage V_{in} is applied to a Voltage-Controlled Oscillator (VCO). The VCO converts this input voltage into a frequency-modulated signal whose oscillation frequency varies linearly with V_{in} . This frequency signal forms the time-domain representation of the analog information, enabling digital-friendly processing.

Subsequently, the Frequency-to-Digital Converter (FDC) quantizes the VCO's output frequency by counting the number of oscillation cycles within a defined sampling interval T_s . The counter accumulates these pulses, and the count is latched by an output register synchronized to the system clock, producing a stable multi-bit digital output D_{out} corresponding to

the input voltage level.

In this work, a 4-bit FDC is employed, with both asynchronous (ripple) and synchronous counter architectures implemented and systematically compared. The asynchronous counter offers simplicity and reduced hardware overhead, but suffers from cumulative propagation delays that can limit counting speed and accuracy at higher frequencies. In contrast, the synchronous counter utilizes a common clock signal across all flip-flops, getting faster and more predictable operation at the expense of increased circuit complexity.

Our comparative analysis evaluates the trade-offs between these architectures in terms of speed, power consumption, timing accuracy, and overall ADC performance. This investigation aims to identify the optimal FDC design for integration with the proposed VCO, balancing conversion and power efficiency for low-power biomedical applications.

Figure 1.1 illustrates the block diagram of the complete VCO-based ADC system, highlighting the interaction between the VCO front-end and the FDC back-end.

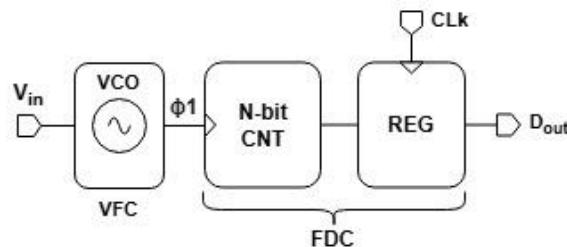


Figure 1.1: ADC Block Diagram.

This ADC architecture benefits from minimized analog complexity and leverages predominantly digital counting techniques, making it well-suited for compact, low-power integrated biomedical systems. The combined use of VCO frequency modulation and digital frequency counting provides a robust, scalable framework that is compatible with modern CMOS process technologies.

1.2 Literature Review

The increasing demand for advanced biomedical monitoring systems, such as those used in Photoplethysmography (PPG) and Brain-Machine Interfaces (BMI) for peak detection, has spurred significant technological advancements in integrated circuit design [10, 11]. However, in modern scaled CMOS technologies, the performance of traditional analog circuits is often constrained by shrinking supply voltages and reduced intrinsic transistor gain. This necessitates innovative architectures that can efficiently bridge the analog and digital worlds[12]. Among these, Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converters (ADCs) have gained considerable traction. Their time-domain operation and amenability to circuit-level implementation in digital-friendly styles make them highly compatible with technology scaling, often outperforming conventional voltage-domain ADCs in this regard. Furthermore, VCO-based ADCs inherently benefit from first-order noise shaping due to the integrating nature of the VCO’s output phase, rendering them suitable for oversampling applications [5, 13, 14].

In this architectural paradigm, the VCO serves the crucial role of converting an analog input voltage into a frequency-modulated signal. This frequency is subsequently processed by a Frequency-to-Digital Converter (FDC) to yield a digital output value. A ring oscillator, a common VCO topology, typically consists of an odd number of inverting delay stages connected in a loop. The delay of these stages, and consequently the oscillation frequency, can be controlled by an input voltage, often through a current-starved biasing mechanism. This allows the VCO to function as a transducer, mapping voltage variations to frequency variations, which are then readily processed in the time domain[15].

A key challenge in deploying VCOs within ADCs is ensuring the linearity of this voltage-to-frequency conversion. Any non-linearity in the VCO’s transfer characteristic directly translates to distortion and the introduction of unwanted harmonics in the ADC’s output spectrum, thereby degrading the effective number of bits (ENOB) [12] . While system-level calibration

or feedback mechanisms can compensate for VCO non-linearity[16, 7] , these often introduce significant circuit complexity. Consequently, there is a strong impetus to address linearity at the circuit level within the VCO itself, as this can greatly simplify the overall ADC system design[17, 14, 18] .Within the realm of VCOs for ADCs, Current-Starved Ring Oscillators (CSROs) are a widely adopted topology due to their integrability, wide tuning range, and relatively low power consumption [13, 18, 19]. CSROs achieve frequency control by limiting the current available to charge or discharge the load capacitances of their constituent inverter stages, a mechanism directly modulated by a control voltage [17, 13, 7]. For instance, operating frequencies up to 3.5 GHz have been reported in 90nm CMOS technology using such oscillators[18].

Various techniques have been explored to enhance the linearity of CSROs. One prominent approach involves careful design of the input control circuitry. [16] proposed a mixed-mode input structure incorporating resistive elements, where the combination of current and voltage control helps to cancel out opposing non-linear effects. Similarly,[12] employed a linearized current control mechanism using a resistive network to map the input voltage, followed by two linear V/I converters whose differential current output provides a highly linear bias for the CSRO over a wide input voltage range. Pre-weighted resistive networks have also been used to generate scaled versions of the input voltage, applied to different delay elements to maintain operation in more linear regions [12] . The VCO presented in [17] utilizes a diode-connected NMOS source degeneration technique to improve V/F linearity while also aiming for area reduction by replacing passive resistors with active devices. While conventional CSROs offer a wide tuning range, they can suffer from inherent linearity issues and are susceptible to increased phase noise [17]. To address these performance limitations, researchers have introduced several novel techniques. These include the employment of differential delay cells to suppress even-order distortions and common-mode noise[17]. Architectural simplifications, such as using only NMOS current sinks or PMOS current sources, have been explored to reduce circuit complexity and power consumption [14]. The introduction of symmetric loads

in parallel with current source/sink transistors has been shown to improve both linearity and stability [14]. Furthermore, output-switching schemes have been investigated to achieve an improved power-delay product and phase-noise bandwidth product [14].

Phase noise remains a critical consideration in VCO design for ADC applications, as it is generally more pronounced in ring oscillators compared to their LC-based counterparts [17]. This phase noise directly translates to jitter in the time domain, limiting the ADC's resolution. To mitigate this, techniques such as integrating charge pumps into the CSRO architecture have been proposed. The rationale, as explored in [17] and further detailed in [17], is that the sharper signal transitions produced by charge pump stages, when compared to conventional inverters, can lead to a reduction in overall phase noise. This approach, involving the replacement of alternate inverter stages in a multi-stage CSRO with charge pump circuits, is a key aspect of the VCO design presented in this work.

The subsequent stage, the Frequency-to-Digital Converter (FDC), is responsible for quantizing the VCO's frequency output. Its design involves trade-offs between accuracy, speed, power, and area. The FDC in [5] employed a D-flip-flop based reset counter, favoring hardware simplicity for power-constrained scenarios. A comparative study by [15] provided a more detailed analysis of different FDC structures, including those based on edge detectors and Gray counters, illustrating how design choices are influenced by specific VCO parameters. The demands on FDC design intensify in ultra-low-voltage (ULV) environments, where increased variability poses significant hurdles. The work by [20] thoroughly investigated FDC speed maximization strategies for 28nm CMOS operating at a mere 0.2V, employing techniques such as parallel XOR-based FDC units and sense-amplify phase samplers with hardware redundancy to ensure reliable operation in the deep-subthreshold regime. The influence of the underlying CMOS technology node is also a significant factor, with research spanning from mature processes like 180nm [13] to advanced nodes such as 16nm [14] and 28nm [20]. Each technology node presents a unique set of trade-offs regarding speed, power dissipation, inte-

gration density, and susceptibility to process variations. Collectively, the reviewed literature underscores a continuous and multifaceted research effort aimed at enhancing the capabilities of VCO-based ADCs. While substantial advancements have been achieved in optimizing individual aspects of the VCO (such as linearity, phase noise, and power efficiency) and the FDC (in terms of speed and accuracy), the development of architectures that holistically address the demanding requirements for wideband, power-efficient, and compact ADC front-ends, particularly suitable for biomedical applications, remains a pertinent and evolving field of study. This thesis seeks to contribute to this area by proposing and evaluating a VCO architecture tailored for such demanding ADC applications.

1.3 Research Motivation

The rapid advancement of miniaturized and low-power electronics, particularly in fields such as wearable health monitoring, implantable biomedical devices, and the broader Internet of Things (IoT) ecosystem, has created a persistent demand for efficient Analog-to-Digital Converters (ADCs). As highlighted in Section 1.1, applications like Photoplethysmography (PPG) for cardiovascular assessment and Brain-Machine Interfaces (BMIs) for neural signal acquisition often require ADCs that can operate with minimal power consumption while occupying a small silicon footprint, without unduly sacrificing performance.

Voltage-Controlled Oscillator (VCO)-based ADCs have emerged as a promising architecture for these scaled CMOS technologies. Their inherent time-domain operation offers advantages in terms of digital-friendliness and responsiveness to technology scaling compared to traditional voltage-domain ADCs. However, realizing high-performance VCO-based ADCs is not without its challenges. As will be detailed further in the literature review (Section 1.2) and Chapter 2, conventional VCOs, especially ring oscillators like Current-Starved VCOs (CSROs), often suffer from non-linear voltage-to-frequency (V-F) characteristics and relatively high phase noise. These non-idealities directly degrade the ADC's effective resolution (ENOB), introduce distortion, and limit its overall accuracy. While system-level calibration

can address some of these issues, such techniques often add complexity and power overhead.

Furthermore, the design of the Frequency-to-Digital Converter (FDC) stage, which quantizes the VCO's output, presents its own set of trade-offs concerning speed, power, and area, particularly when choosing between different counter architectures. For a complete ADC solution, optimizing both the VCO and the FDC is crucial.

This research is motivated by the need to develop a compact, power-efficient 4-bit VCO-based ADC architecture that specifically addresses these challenges at the circuit level. The primary goal is to enhance the V-F linearity and reduce the phase noise of the VCO core through novel design techniques, while also systematically evaluating the impact of different FDC counter implementations (asynchronous and synchronous) on the overall ADC performance. The development of such an ADC, suitable for integration into sensor front-ends for applications like those mentioned, could contribute to more robust and energy-efficient data acquisition in power-constrained biomedical and IoT systems. The specific aim is to explore a design that balances performance improvements with practical considerations of area and power, making it a viable candidate for real-world deployment.

1.4 Research Objectives

In light of the identified gap in developing compact and power-efficient Analog-to-Digital Converters (ADCs) suitable for biomedical applications, the research presented in this thesis sets its primary goal to design, implement, and comprehensively evaluate a 4-bit Voltage-Controlled Oscillator (VCO)-based ADC. This work aims to address inherent challenges in conventional VCO-based ADC architectures, particularly concerning VCO linearity and phase noise, and to investigate the impact of Frequency-to-Digital Converter (FDC) design choices on overall system performance. To carry out this project, the specific objectives of this work are outlined as follows.

- a) To design and analyze a novel five-stage current-starved Voltage-Controlled Oscillator (VCO) incorporating source degeneration for enhanced Voltage-to-Frequency (V-F) linearity and an integrated charge pump mechanism for reduced phase noise, suitable for a 4-bit ADC front-end.
- b) To design and comparatively investigate 4-bit Frequency-to-Digital Converter (FDC) architectures, specifically implementing and evaluating both asynchronous (ripple) and synchronous binary counter designs, along with an associated output register, to quantize the VCO's frequency output.
- c) To integrate the proposed VCO and selected FDC architectures to form a complete 4-bit VCO-based ADC system, and to comprehensively evaluate its performance through simulation, considering metrics such as linearity (DNL, INL), dynamic range (SNDR, SFDR, ENOB), power consumption, and robustness across process, voltage, and temperature (PVT) variations.
- d) To develop the physical layout for the core components of the VCO-based ADC, specifically the VCO and FDC blocks, and to perform post-layout simulations to assess the impact of parasitic effects on system performance and validate the design's suitability for practical implementation.

The expected outcome of this work is, therefore, a robust and well-characterized 4-bit VCO-based ADC architecture, demonstrating improved linearity and phase noise performance in the VCO, alongside a thorough understanding of the trade-offs associated with different FDC counter implementations. This will result in a design suitable for low-power biomedical applications, validated through extensive simulation and post-layout analysis, contributing to the advancement of energy-efficient data acquisition systems.

1.5 Organization of the Thesis

The remainder of this thesis is organized as follows.

Chapter 2 provides a comprehensive review of the foundational knowledge necessary for understanding VCO-based ADCs. It examines conventional architectures, operating principles, and critical design considerations for the primary building blocks: the VCO and the FDC. Furthermore, it situates the relevance of VCO-based ADCs within the expanding field of biomedical applications, highlighting existing limitations and thereby contextualizing the motivations for the proposed design.

Chapter 3 details the architecture and design elements of the proposed 4-bit VCO-based ADC. It describes the novel five-stage current-starved ring VCO, featuring diode-connected NMOS source degeneration for enhanced V-F linearity and an integrated charge pump technique for reduced phase noise. The chapter then elaborates on the design of the subsequent FDC stage, exploring two distinct counter architectures: asynchronous (ripple) and synchronous (binary), along with the 4-bit output register. Design considerations for interfacing these blocks and key trade-offs are also discussed.

Chapter 4 presents the simulation results and performance analysis of the proposed VCO and the complete 4-bit VCO-based ADC. This includes transient analysis, PSS analysis, phase noise evaluation, DC power consumption, and statistical analysis (Monte Carlo simulations) for the VCO, including post-layout results. Subsequently, the performance of the complete ADC system, utilizing both asynchronous and synchronous FDC counter implementations, is evaluated in terms of static (DNL, INL) and dynamic (SNDR, SFDR, ENOB) characteristics, along with comparisons.

Chapter 5 provides a comprehensive summary of the research conducted, highlighting the key findings and contributions of the thesis. It discusses the research outcomes in relation to the stated objectives, underscores the significance of the work, and outlines potential avenues for future investigation and enhancement of the proposed VCO-based ADC architecture.

CHAPTER 2

BACKGROUND AND RELATED WORKS

2.1 Introduction

This chapter focuses the foundational knowledge necessary to understand the proposed Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converter (ADC). It examines the conventional architectures, operating principles, and critical design considerations for the two primary building blocks: the VCO and the Frequency-to-Digital Converter (FDC). Furthermore, this chapter will situate the relevance of VCO-based ADCs within the expanding field of biomedical applications, thereby providing context for the specific design goals and performance metrics targeted in this thesis. This comprehensive review will help to explain the reasons for the new design approaches presented in the following chapters.

2.2 Introduction to VCO-Based Analog-to-Digital Converters

Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converters (ADCs) have emerged as a promising alternative to traditional voltage-domain ADCs, particularly in scaled CMOS technologies where designing high-performance analog circuits is increasingly challenging [21]. The core principle of a VCO-based ADC involves a two-step conversion: first, the analog input voltage is converted into a frequency-modulated signal by a VCO; second, this frequency is digitized by a Frequency-to-Digital Converter (FDC) [22]. This time-domain signal processing approach offers several advantages, including inherent digital-friendliness, amenability to technology scaling, and the potential for first-order noise shaping due to the integrating nature of the VCO's output phase [23]. These characteristics make them attractive for various applications, from sensor interfaces to communication systems, including the biomedical applications highlighted in Chapter 1.

Despite their benefits, the performance of VCO-based ADCs is critically dependent on the

characteristics of their core components. The VCO's linearity, phase noise, and tuning range directly impact the ADC's resolution, signal-to-noise ratio (SNR), and dynamic range [24]. Similarly, the FDC's architecture, speed, and quantization capabilities determine how accurately and efficiently the VCO's frequency output is translated into a digital word [20]. This chapter provides a review of the related work, application and established principles for these key components. It will delve into the common architectures, operational principles, inherent challenges, and reported improvement techniques for VCOs, with a focus on Current-Starved Ring Oscillators (CSROs). Subsequently, it will review FDC architectures, primarily focusing on counter-based approaches, and discuss their impact on overall ADC performance. This review aims to establish the context for the novel VCO design and FDC analysis presented in this thesis.

2.3 Voltage-Controlled Oscillators (VCOs) in ADC Front-End

The VCO is the heart of a VCO-based ADC, responsible for the crucial analog-to-time (or frequency) domain conversion. Its performance directly dictates the quality of the information passed to the subsequent digital processing stages.

2.3.1 Overview of VCO Topologies for ADCs

Various VCO topologies have been explored for ADC applications, each with its own set of trade-offs. LC-tank VCOs generally offer excellent phase noise performance but typically have a limited tuning range and consume significant silicon area due to the integrated inductors [25, 26]. Relaxation oscillators can provide wide tuning ranges but often suffer from higher phase noise and linearity challenges. Ring oscillators, particularly Current-Starved Ring Oscillators (CSROs), have gained considerable traction due to their compact size, wide tuning range, ease of integration in standard CMOS processes, and relatively low power consumption [27]. These attributes make CSROs highly suitable for applications with limited area and power, such as those found in portable biomedical devices and integrated sensor nodes [28], aligning with the motivations of this work. While CSROs traditionally shows higher phase

noise compared to LC-VCOs, their other advantages often make them a preferred choice when area and tuning range are priority.

2.4 Conventional Current-Starved Voltage-Controlled Oscillators (CSVCOs)

Voltage-Controlled Oscillators (VCOs) are fundamental components in modern electronic systems, serving to convert a DC input voltage into a periodic output signal whose frequency is a function of this input voltage. Their utility spans a wide range of applications, including phase-locked loops (PLLs), frequency synthesizers, clock generation circuits, and, relevantly to this work, as core elements in certain types of analog-to-digital converters (ADCs). Among the various VCO topologies, ring oscillators, particularly Current-Starved Ring Oscillators (CSVCOs), are frequently chosen for their ease of integration, wide tuning range, and suitability for CMOS implementation [19].

2.4.1 The Principle of Current Starvation in Ring Oscillators

A basic ring oscillator is constructed by cascading an odd number of inverting logic stages in a closed loop. For sustained oscillation, the circuit must satisfy the Barkhausen criteria, providing a total phase shift of 360° (or multiples thereof) around the loop and a loop gain greater than unity at the oscillation frequency. The oscillation frequency is inversely proportional to the total propagation delay around the ring.

The "current-starving" technique in a CSVCO offers a mechanism to control this propagation delay, and thereby the oscillation frequency, by deliberately limiting the current available to each inverter stage for charging and discharging its load capacitance. A reduction in the available current leads to slower charging and discharging processes, increasing the propagation delay per stage and consequently lowering the overall oscillation frequency. Conversely, increasing the available current speeds up these transitions, reducing the delay and increasing the frequency. This modulation of current is typically achieved through additional transistors

controlled by an external voltage, V_{ctrl} .

2.4.2 Architecture of a Conventional N-Stage CSVCO

A common architecture for an N-stage CSVCO is illustrated in Figure 2.1. This particular schematic depicts a five-stage ($N=5$) ring oscillator.

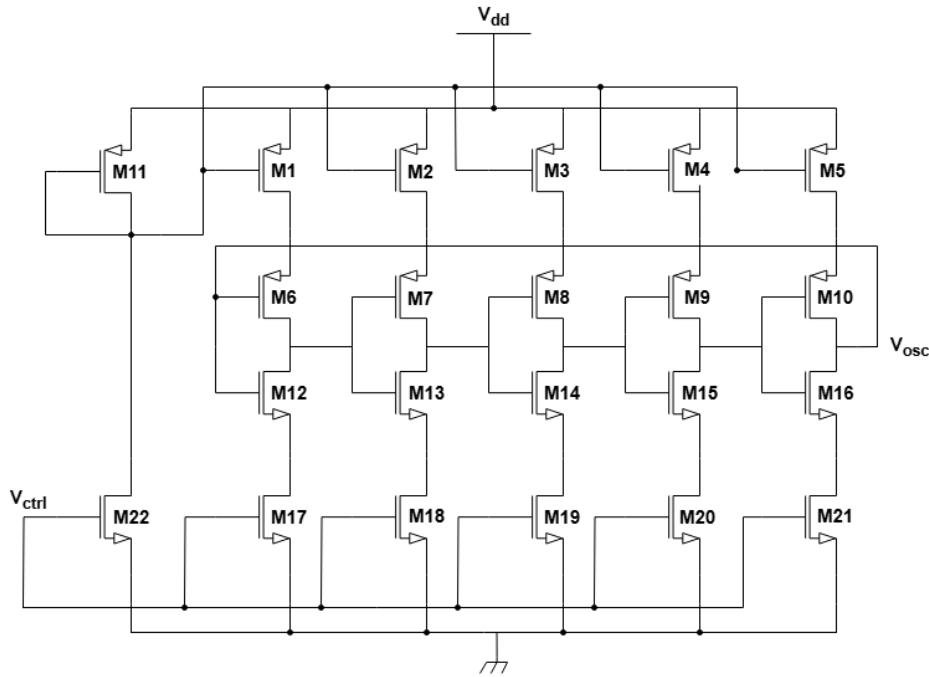


Figure 2.1: Conventional five-stage Current-Starved Ring Oscillator.

The circuit can be decomposed into several key functional blocks:

Inverter Delay Stages: The core of the oscillator comprises N identical inverter stages. In Figure 2.1, these are formed by PMOS transistors M6–M10 and NMOS transistors M12–M16. For instance, M6 (PMOS) and M12 (NMOS) constitute the first inverting stage, with its output feeding the input of the subsequent stage (M7/M13), and so on, until the output of the final stage (M10/M16) feeds back to the input of the first stage, closing the loop.

Current-Starving Transistors: Associated with each core inverter are two "starving" transistors: one PMOS and one NMOS. In the first stage, PMOS transistor M1 limits the current sourcing capability of M6 (the pull-up transistor of the inverter), and NMOS transistor

M17 limits the current sinking capability of M12 (the pull-down transistor of the inverter). This configuration is replicated across all stages (M1–M5 for PMOS starving, M17–M21 for NMOS starving). These starving transistors effectively act as variable resistors, whose conductance is modulated by their gate voltages.

Bias and Current Mirroring Circuitry: The gate voltages of the starving transistors are controlled by a bias circuit, which itself is governed by the external control voltage, V_{ctrl} . In Figure 2.1, transistors M11 and M22 play a central role in this bias generation. V_{ctrl} is applied to the gate of M22. M11, whose gate is also connected to V_{ctrl} , operates in conjunction with M22. Given that V_{ctrl} directly drives the gates of M11 (PMOS) and M22 (NMOS), as V_{ctrl} increases, the current through M22 ($I_{D(M22)}$) increases, while the current through M11 ($I_{D(M11)}$) typically decreases, assuming M11 remains in saturation.

The current established by M11 serves as a reference for the PMOS starving transistors M1–M5. The gates of M1–M5 are connected to the gate of M11. Since their sources are tied to V_{DD} , M1–M5 mirror the current flowing through M11 (scaled by their respective W/L ratios if different from M11). This is a fundamental application of a PMOS current mirror, where a reference current in one branch is replicated in other branches [29]. Specifically, as described by Razavi, for a basic current mirror, if M11 provides the reference current I_{REF} and M1–M5 are the output transistors, the output current I_{out} in each starving PMOS is given by:

$$I_{out} = I_{REF} \times \frac{(W/L)_{out}}{(W/L)_{REF}} \quad (2.1)$$

where (W/L) terms represent the aspect ratios of the respective transistors.

Similarly, the current through the NMOS starving transistors M17–M21 is influenced by V_{ctrl} via M22. As V_{ctrl} controls the current $I_{D(M22)}$, this current (or a related bias voltage) dictates the current sinking capability of M17–M21. These starving transistors thereby control the net

current I_D that flows through each inverter stage.

2.4.2.1 Stage Delay and Oscillation Frequency Analysis

The propagation delay (t_d) of each inverter stage is the primary determinant of the VCO's oscillation frequency. This delay is fundamentally the time required to charge or discharge the total load capacitance (C_{tot}) at the output node of an inverter stage. C_{tot} comprises the output capacitance of the driving inverter (primarily drain-to-bulk and drain-to-gate capacitances of its PMOS and NMOS devices) and the input capacitance of the subsequent stage (primarily gate-to-source and gate-to-drain capacitances of its PMOS and NMOS devices). This can be expressed as:

$$C_{\text{tot}} = C_{\text{out}} + C_{\text{in}} \quad (2.2)$$

For a CMOS inverter where C_{out} includes the parasitic capacitances of the driving stage and C_{in} represents the gate capacitances of the driven stage, a more detailed approximation, following the model presented in [30], can be written as:

$$C_{\text{tot}} = C'_{\text{ox}}(W_p L_p + W_n L_n) + \frac{3}{2} C'_{\text{ox}}(W_p L_p + W_n L_n) \quad (2.3)$$

where C'_{ox} is the gate oxide capacitance per unit area, and W_p, L_p, W_n, L_n are the widths and lengths of the PMOS and NMOS transistors of the core inverter stage, respectively. This expression simplifies to:

$$C_{\text{tot}} \approx \frac{5}{2} C'_{\text{ox}}(W_p L_p + W_n L_n) \quad (2.4)$$

The time taken to charge C_{tot} from logic low (approx. 0V) to the inverter's switching threshold (V_{SP} , often approximated as $V_{DD}/2$) is t_{LH} (low-to-high transition time), and the time to dis-

charge C_{tot} from logic high (approx. V_{DD}) to V_{SP} is t_{LH} (high-to-low transition time). Assuming the starved current available for charging (via PMOS path) is $I_{D,\text{charge}}$ and for discharging (via NMOS path) is $I_{D,\text{discharge}}$:

$$t_{LH} \approx \frac{C_{\text{tot}} \cdot V_{SP}}{I_{D,\text{charge}}} \quad (2.5)$$

$$t_{HL} \approx \frac{C_{\text{tot}} \cdot (V_{DD} - V_{SP})}{I_{D,\text{discharge}}} \quad (2.6)$$

If the design aims for symmetric rise and fall times, then $I_{D,\text{charge}} \approx I_{D,\text{discharge}} = I_D$ (the net starved current), and $V_{SP} \approx V_{DD}/2$. The oscillation period T for an N -stage ring oscillator is N times the sum of these transition times for one stage. A common expression for the oscillation frequency f_{osc} is:

$$f_{\text{osc}} = \frac{1}{T} \approx \frac{1}{N(t_{LH} + t_{HL})} \quad (2.7)$$

If $V_{SP} = V_{DD}/2$ and $I_{D,\text{charge}} = I_{D,\text{discharge}} = I_D$, then $t_{LH} + t_{HL} = (C_{\text{tot}} \cdot V_{DD})/I_D$. Thus,

$$f_{\text{osc}} \approx \frac{I_D}{N \cdot C_{\text{tot}} \cdot V_{DD}} \quad (2.8)$$

This equation clearly indicates that the oscillation frequency is directly proportional to the starved current I_D and inversely proportional to the number of stages N , the total load capacitance per stage C_{tot} , and the supply voltage V_{DD} . The control voltage V_{ctrl} modulates I_D , thus tuning f_{osc} .

2.4.2.2 Limitations of Conventional CSVCOs

Despite their simplicity and wide tuning range, conventional CSVCOs suffer from several inherent limitations that can degrade their performance in sensitive applications:

- **Non-Linearity:** A significant challenge is the non-linear relationship between the control voltage V_{ctrl} and the resulting oscillation frequency f_{osc} . This non-linearity primarily arises from the non-linear dependence of the starved current I_D on V_{ctrl} , as the starving transistors may transition between saturation and triode regions of operation over the V_{ctrl} range. The body effect in MOS transistors also contributes to this non-linearity. A non-linear V/f characteristic leads to harmonic distortion in systems where the VCO is part of a signal path, reducing the effective resolution (ENOB).
- **Phase Noise:** Ring oscillators, in general, exhibit higher phase noise compared to LC-tank based oscillators. Phase noise in CSVCOs originates from various sources, including thermal noise in the channel of the MOS transistors, flicker (1/f) noise which is upconverted to the oscillation frequency, and noise coupled from the power supply and substrate. The "starving" of current can lead to slower signal transitions, making the switching instants more susceptible to timing jitter induced by these noise sources, thereby degrading phase noise performance.
- **Power Supply Rejection Ratio (PSRR):** Equation (2.8) shows a direct dependence of f_{osc} on V_{DD} . Consequently, any fluctuations or noise on the power supply rail will directly modulate the output frequency, leading to poor Power Supply Rejection Ratio (PSRR). Furthermore, the starved current I_D itself can be sensitive to V_{DD} variations, especially if the starving transistors do not behave as ideal current sources.
- **Process, Voltage, and Temperature (PVT) Variations:** The performance of MOS transistors, particularly parameters like threshold voltage (V_{TH}) and carrier mobility (μ_n, μ_p), is highly susceptible to variations in manufacturing processes, operating voltage, and ambient temperature. These variations significantly affect I_D and C_{tot} , leading to substantial deviations in f_{osc} from its nominal value, often necessitating calibration or compensation schemes.

These limitations highlight the need for improved CSVCO architectures that can offer better linearity, lower phase noise, and enhanced robustness, which forms the motivation for the work presented in subsequent chapters of this thesis.

2.5 Frequency-to-Digital Converters (FDCs)

In the architecture of a Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converter (ADC), the Frequency-to-Digital Converter (FDC) plays a pivotal role. It serves as the interface between the analog domain, represented by the frequency-modulated output of the VCO, and the final digital output word.

2.5.0.1 Role of FDCs in VCO-Based ADCs

The fundamental operation of a VCO-based ADC involves two primary conversion steps,. Initially, an analog input voltage (V_{in}) is applied to a Voltage-to-Frequency Converter (VFC), which is typically the VCO itself. The VCO transforms this analog voltage into a signal whose frequency (Φ_1 or f_{VCO}) is proportional to V_{in} . Subsequently, the FDC processes this frequency-modulated signal to produce a corresponding multi-bit digital output (D_{out}). The FDC, therefore, quantifies the VCO's output frequency, effectively translating the information encoded in the time or frequency domain into a discrete numerical representation. The FDC typically consists of an N-bit counter (N-bit CNT) that counts the VCO pulses, and a register (REG) that latches the count as illustrated in the generic block diagram shown in Figure 2.2.

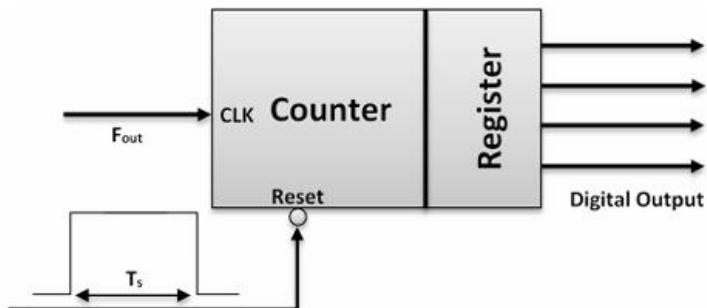


Figure 2.2: Frequency-to-digital converter FDC Block Diagram[5]

The core components and their operational principle within the FDC are as follows:

- **Counter:** This is the central processing unit of the FDC. It accumulates (counts) the number of pulses received from the VCO output (f_{VCO}) over a precisely defined time window, known as the sampling period (T_s).
- **Register:** At the conclusion of each sampling period T_s , the accumulated count from the counter is transferred to an output register. This register holds the digital value, providing a stable digital output (D_{out}) while the counter may be reset or engaged in a subsequent counting cycle.
- **Timing and Control Logic:** This circuitry manages the FDC's operation. It includes signals to Reset the counter before each new counting period and to define the sampling window T_s . The input signal f_{VCO} often serves as the clock for an asynchronous counter or is synchronized for synchronous designs.

The operational sequence involves initializing the counter via the Reset signal, enabling it to accumulate pulses from F_{out} for the duration of the sampling window T_s , and then latching the final count into the output register. This cycle repeats for continuous conversion. The digital output value (Count) obtained from the FDC is directly proportional to the average input frequency during the sampling window: Digital Output (Count) $\approx f_{VCO} \times T_s$.

2.5.1 Counter Implementation and Output Register

Digital counters are sequential logic circuits. D-type Flip-Flops (DFFs) are commonly used, often configured as T-type (Toggle) Flip-Flops by connecting the D input to the \bar{Q} output. An N-bit asynchronous ripple counter can be built by cascading N DFFs in toggle mode, as shown in Figure 2.3 (illustrating a 4-bit example). The VCO output clocks the first DFF (LSB), and each subsequent DFF is clocked by the Q output of the preceding stage. Although simple, ripple counters suffer from cumulative propagation delay.

Synchronous counters, in contrast, employ a common clock signal for all flip-flops. State transitions are managed by additional combinational logic, leading to faster and more pre-

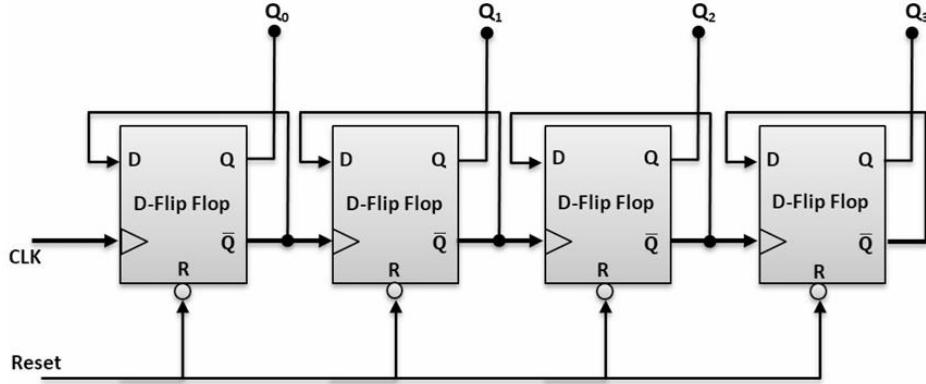


Figure 2.3: 4-bit asynchronous ripple counter using D Flip-Flops[5]

dictable performance, but at the cost of increased circuit complexity. The choice between asynchronous and synchronous counters is a key design decision, explored in this thesis for the 4-bit FDC.

The output register, typically implemented using N D-Flip-Flops, captures and holds the N-bit count from the counter at the precise moment marking the end of the sampling period T_s . This ensures a stable digital value D_{out} for subsequent digital systems, even as the counter itself might be resetting or starting a new counting cycle. This register is clocked by a common latch enable or clock signal, distinct from the F_{out} signal, synchronized with the completion of the T_s interval.

2.5.1.1 Considerations for FDC Design

Several factors are critical in the design and performance of an FDC:

Sampling Time (T_s): The duration and stability of T_s are paramount, as this period directly scales the input frequency to the output digital count. Any jitter or inaccuracy in T_s translates to conversion errors.

Counter Resolution (Number of Bits, N): This determines the maximum digital value the FDC can produce. For a given T_s , it sets the maximum input frequency that can be measured without overflow. Conversely, for a given maximum frequency, it influences the required T_s .

or the quantization step size.

Maximum Operating Frequency: The counter and associated logic must be capable of operating reliably at the highest frequency expected from the VCO. This is particularly a concern for asynchronous ripple counters.

Synchronization: Careful design is required to ensure proper synchronization between the VCO output signal, the generation of the T_s window, the counter operation, and the latching of the count into the output register to prevent timing hazards like metastability and ensure accurate conversions.

2.6 Application

Wearable and implantable biomedical systems are rapidly advancing, transforming healthcare towards a proactive, personalized paradigm through remarkable progress in miniaturization and integration into everyday items or less invasive implantable forms. These systems boast increasingly sophisticated multiparameter sensing capabilities, including novel non-invasive biomarker detection, all driven by enhanced accuracy and ultra-low-power electronics devices. Seamless wireless connectivity, coupled with cloud and edge computing, facilitates robust data management, while the integration of AI and machine learning unlocks personalized insights, enables early disease detection shown in Figure 2.4. Concurrently, advancements in biocompatible paving the way for continuous health monitoring, effective remote patient management, and increasingly integrated therapeutic interventions that are pushing the boundaries of personalized medicine.

2.6.1 Photoplethysmography (PPG) Application

Photoplethysmograph (PPG) signal is the representation of the volumetric changes in blood vessels. The principle of operation is based on registration of a useful signal by two possible methods. One is transmissive method, where light passes through the tissues another is reflective method, where light is reflected by the tissues. PPG signals originate by absorption of

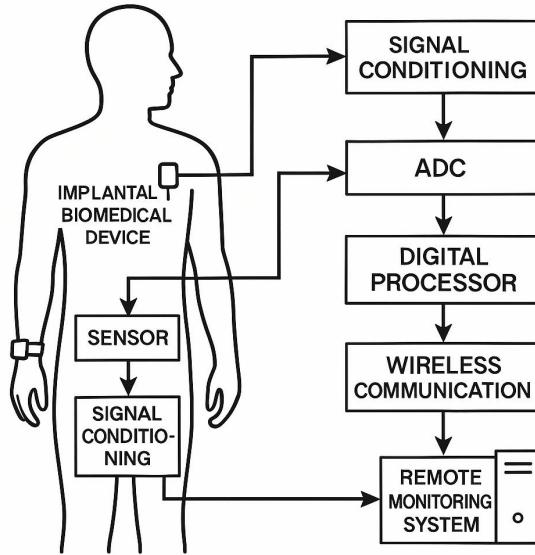


Figure 2.4: Wearable and Implantable Biomedical System.

optical radiation by the pulsating blood volume and contain valuable clinical information. The whole architecture is shown in Figure 2.5. The raw PPG signal can be varied from 200mV to 1000mV and for getting the accuracy in information 10-15Hz frequency is considered. After preprocessing by using Analogue Front End (AFE) module consisting of filters and amplifiers to detect the systolic peak and the reflected wave peak of the raw analogue signal ADC is considered here for extracting medical purpose information such as Pulse Transit Time(PPT) or Pulse Wave velocity(PWV), analysing waveform Morphology to assess vascular compliance or missing peaks flag atrial fibrillation etc that contains lots of physiological significances resulting in better clinical diagnosis[31]. In both wearable and implantable biomedical applications, photoplethysmography (PPG) enables continuous, noninvasive monitoring of cardiovascular dynamics by converting blood-volume pulsations into rich electrical waveforms.

2.6.2 Brain Machine Interface(BMI) Application

Brain–Machine Interfaces (BMIs) are bidirectional systems that translate neural activity into digital control signals and, conversely, deliver sensory feedback to the nervous system, enabling direct communication between the brain and external devices. In biomedical contexts,

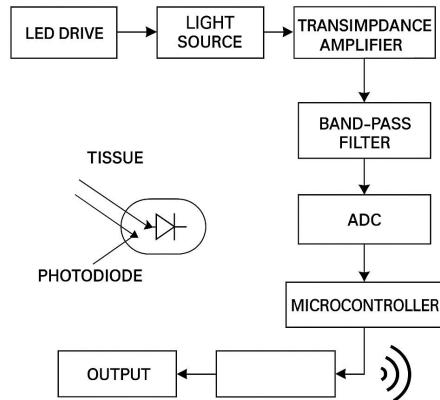


Figure 2.5: Photoplethysmography(PPG) Block Diagram.

BMIs have revolutionized neuroprosthetics by allowing paralyzed patients to control robotic limbs or computer cursors purely through thought, facilitated advanced rehabilitation therapies for stroke and spinal-cord injury via real-time neural feedback. In wireless neural recording 4 bit ADC can be considered as shown the in the Figure 2.6. Electrode array captures raw extracellular neural signals varies from $100\mu\text{V}$ to 1mV and this neural activity lies in the frequency range of 300Hz to 10KHz . Analogue front end with 60dB gain amplifies the signal into ADC's input range and drives a low capacitance load suitable for a VCO input. It captures the fast upstroke of action potentials while its 4-bit quantization is just enough to resolve spike peaks above the noise floor. The spike detection reveals some significant medical information for diagnosis purpose such as Parkinson's and Movement Disorder Biomarkers, Sleep and Anesthesia Depth, Cognitive Load and Attention[32]

In both the cases Analogue Front End (AFE) is considered for pre-processing the raw signal to compatible with the ADC. Figure 2.6 shows a simplified block diagram of a biopotential acquisition system which comprises an AFE and an ADC. The AFE is composed of an instrumentation amplifier (IA), a programmable gain amplifier (PGA), and an anti-aliasing low-pass filter. The bioelectric signals have dynamic range between tens of microvolt to hundreds of millivolt, and they cover a frequency band with the highest frequency less than 10 kHz . To

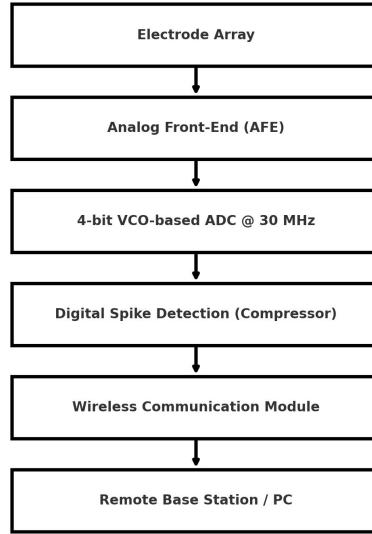


Figure 2.6: Brain Machine Interfaces (BMI) Block Diagram.

extract the low-level bioelectric signals, the IA filters the differential electrode offset, and defines a low noise performance and a high common-mode-ripple-rejection (CMRR) of the AFE. The PGA is used to adjust the gain and bandwidth of the readout for different bioelectric signals. In certain cases, to meet with stringent power budgets, the PGA can also perform the operation of an anti-aliasing filter. Finally, the bioelectric signals after sensing, filtering, and amplifying by the AFE are strong enough to be digitized in the succeeding ADC.

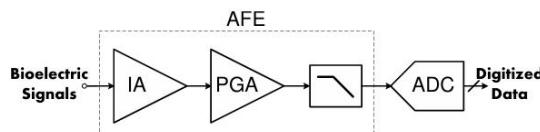


Figure 2.7: Biomedical Acquisition System.

ADC is a key component as the interface between the analog world and the digital domain. Conversion of the low-frequency bioelectric signals with ultra-low-power consumption. This, combined with the required conversion accuracy makes the design of such ADCs a major challenge. This thesis proposes an architecture of a 4-Bit Voltage Controlled Oscillator (VCO) based ADC with a very power consumption efficiency in a compact area and fast, which will

enhance the battery life and portability of wearable and implanted biomedical electronics devices with reasonable accuracy.

2.7 Design Considerations

VCO-based ADCs convert an analog input voltage into a digital output by modulating the frequency or phase of a voltage-controlled oscillator (VCO), which is then digitized by a counter or a time-to-digital converter. There are some critical design considerations which includes the VCO's linearity, as its voltage-to-frequency/phase characteristic directly impacts the ADC's overall linearity and accuracy, the VCO's phase noise and jitter are paramount, as they set fundamental limits on the ADC's resolution (ENOB) and signal-to-noise ratio (SNR). Managing trade-offs between conversion speed dictated by VCO slew rate, counter speed, and quantization time, power consumption especially for high-frequency, low-noise VCOs, and the VCO's tuning range, alongside the need for potential calibration to mitigate process, voltage, and temperature (PVT) variations, are also key aspects. All design considerations are classified into two different block one is VCO block and another is FDC block.

2.7.1 VCO Design Parameters

Voltage-Controlled Oscillator (VCO) serves as the crucial analog-to-time (or frequency/phase) domain converter. Its fundamental role is to take the continuous analog input voltage and transform it into an oscillating signal whose frequency or phase is directly modulated by this input voltage. This intermediate, time-varying signal carries the analog information in its frequency or phase. Thereafter it is processed by subsequent digital circuitry. Therefore, the VCO enabling the conversion by translating voltage amplitude into a more easily quantifiable time-based parameter. Significant parameter such as stage of parameters, VCO type, phase noise are always be considered.

2.7.1.1 VCO type Selection

Among the various types of Voltage-Controlled Oscillators (VCOs), the Ring VCO has been selected for this ADC design due to its compact size, low power consumption, and wide bandwidth, key attributes for modern integrated systems. Unlike LC-based oscillators, Ring VCOs are fully compatible with standard CMOS processes, making them highly suitable for on-chip integration in area- and power-constrained applications such as biomedical and sensor interfaces. Despite exhibiting higher phase noise compared to LC VCOs, the trade-offs are acceptable in this context, where minimizing die area and achieving broad tuning capability are prioritized over ultra-low noise performance.

2.7.1.2 Number of Stages

The number of stages in a ring VCO is a critical design parameter that directly influences its oscillation frequency, phase noise, power consumption, and output waveform quality. To sustain oscillation, the ring must have an odd number of stages to produce a 180° phase shift and meet the Barkhausen criteria for oscillation. The oscillation frequency f_{osc} of a ring VCO is inversely proportional to the number of delay stages. More stages introduce more delay, thus lowering the frequency. Fewer stages enable higher frequency operation.

$$f_{\text{osc}} = \frac{1}{2Nt_{\text{delay}}} \quad (2.9)$$

Increasing the number of stages can improve phase noise performance slightly, increased power dissipation. Since we aim wide bandwidth with low power, Five stage ring oscillator is considered to balance speed and design simplicity, especially in low-power ADC application.

2.7.1.3 Delay Cell Design

CMOS inverter is considered here for each delay cell. Inverter sizing is significant to balance gm for speed vs. parasitic C for swing and power. Larger devices lower phase noise but increase C_{par} and power. Significant Vds headroom so that current-starve devices operate in saturation across PVT corners called stack effect. series resistors or source degeneration to decouple control-voltage feedthrough into the oscillator nodes.

2.7.1.4 Frequency tuning range and linearity

The absolute tuning range is considered as

$$\Delta f = f_{\max} - f_{\min} \quad (2.10)$$

Frequency most importantly depends on delay(t) of each cells that depends on node capacitance(C), device trans conductance(B) and transistor sizing.

$$f(V_{\text{ctrl}}) \approx \frac{1}{2N t_{\text{delay}}(V_{\text{ctrl}})} \quad (2.11)$$

$$t_{\text{delay}} \approx \frac{C_L V_{DD}}{\beta (V_{\text{ctrl}} - V_{th})^2} \quad (2.12)$$

By tuning the device trans conductance and load capacitance, frequency range is tuned until it meets the condition.

$$\beta = \frac{1}{2} \mu C_{ox} \frac{W}{L} \quad (2.13)$$

Supply voltage also impact the tuning frequency range where the relation is inversely pro-

portional. But higher Vdd can increase the maximum headroom for control voltage enabling a smaller delay and larger frequency. Body biasing is also an alternative way to control the frequency range by affecting threshold voltage.

$$t_{\text{delay}} \propto \frac{V_{DD}}{(V_{\text{ctrl}} - V_{th})^2} \quad (2.14)$$

2.7.1.5 Phase Noise

Phase noise describes the random fluctuations of an oscillator's phase around its ideal periodic signal. In a VCO, these fluctuations manifest as skirts on the carrier in the frequency domain, degrading spectral purity and system performance. A widely used model for oscillator phase noise is Leeson's equation, which captures thermal noise amplification by the resonator's quality factor and flicker noise up-conversion. In radians, it can be written as

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left[\frac{F kT}{2 P_{\text{sig}}} \left(1 + \frac{\omega_0^2}{4Q^2 \Delta\omega^2} \right) \right] \quad (2.15)$$

Here, F is the noise factor of the active devices and Q is the loaded quality factor. Below the flicker-noise corner ω_c , flicker noise up-conversion adds an extra term,

$$\mathcal{L}_{\text{flicker}}(\Delta\omega) = \mathcal{L}(\Delta\omega) + 10 \log_{10} \left(1 + \frac{\omega_c}{\Delta\omega} \right) \quad (2.16)$$

Leeson's equation shows that increasing signal power, lowering device noise factor, or boosting Q at the resonance all reduce phase-noise skirts.

2.7.1.6 Jitter Effect

Jitter is the time-domain counterpart of phase noise, quantifying the uncertainty in the timing of zero-crossings or edges of an oscillator output. It directly impacts sampling accuracy in ADCs and timing in digital systems. The RMS phase deviation is found by integrating the single-sideband phase-noise spectrum

$$\sigma_{\phi,\text{rms}}^2 = 2 \int_{\Delta\omega_l}^{\Delta\omega_2} 10^{\frac{\mathcal{L}(\Delta\omega)}{10}} d(\Delta\omega) \quad (2.17)$$

Converting to timing jitter gives

$$\sigma_{\tau,\text{rms}} = \frac{\sigma_{\phi,\text{rms}}}{\omega_0} = \frac{1}{\omega_0} \sqrt{2 \int_{\Delta\omega_l}^{\Delta\omega_2} 10^{\frac{\mathcal{L}(\Delta\omega)}{10}} d(\Delta\omega)} \quad (2.18)$$

Integrating phase noise over the relevant offset range yields the oscillator's timing uncertainty, which dictates overall system timing accuracy.

2.7.1.7 Output Buffering and Loading

The buffer sits between the VCO core and the load ADC to prevent the downstream load capacitance or impedance from pulling on the oscillator nodes and perturbing delay of each cell. It provides sufficient current to charge/discharge the load without excessive droop or distortion. In some cases the buffer also translates the swing to CMOS logic levels or boosts amplitude. We have used Inverter cells as buffer cell. Any buffer input capacitance or bias-node capacitance appears in the ring's total load

$$C_{L,\text{total}} = C_{\text{par}} + C_{\text{ext}} + C_{\text{in,Buf}} \quad (2.19)$$

By increasing the buffer capacitance it exhibits a reduced frequency range.

2.7.1.8 Layout and parasitics

Due to the parasitic components such as capacitance and resistance, the frequency range that is achieved in schematic simulation will be reduced. Therefore, it is important to consider this to make the ADC workable perfectly.

2.7.1.9 Slew Rate

VCO Slew Rate describes the maximum rate at which the oscillator's output voltage can change, at the steepest edge of its waveform. In a current-starved ring VCO, this is set by the available tail current charging or discharging the output capacitance.

$$SR = \max \left| \frac{dV_{out}}{dt} \right| \quad (2.20)$$

In a single delay cell, the peak charging (or discharging) current is approximately the starvation bias current. With total node capacitance the maximum slope is

$$SR \approx \frac{I_{bias}}{C_L} \quad (2.21)$$

The more bias current increases and the node capacitance decreases, the more SR rises. Sharper edges (higher SR) reduce uncertainty in zero-crossing detection, lowering timing jitter and Phase noise. But the power also increases. Therefore there need a trade off between them.

2.7.2 FDC Design Parameters

A Frequency-to-Digital Converter (FDC) translates an input signal's frequency into a digital output, most commonly by counting input signal cycles over a precisely known reference time window, or by measuring the input signal's period using a stable, high-frequency reference clock. Key design considerations include defining the required resolution and accuracy,

which are directly influenced by the stability and precision of the reference time/clock, the counter's bit-width, and the chosen measurement interval (which also dictates conversion speed). Managing the input frequency range, minimizing quantization error, mitigating the impact of jitter on both the input and reference signals, and considering power consumption versus performance trade-offs are also crucial for robust FDC design.

2.7.2.1 Quantization Noise and SNR

Quantization noise arises because an analog signal of arbitrary amplitude must be mapped to one of a finite set of discrete levels by the ADC. The difference between the true signal $x(t)$ and its quantized version $x_q(t)$ is the quantization error $e(t)$, which can be modeled as an additive noise source under certain conditions (e.g. a sufficiently busy signal), no correlation between signal and quantization steps. Quantization Noise is modeled as

$$\sigma_q^2 = \frac{\Delta^2}{12} \quad (2.22)$$

Signal Power for sinusoid Case is considered as

$$P_{\text{sig}} = \frac{V_{\text{FS}}^2}{8} \quad (2.23)$$

The linear SNR is the ratio of signal power to quantization noise power

$$\text{SNR}_{\text{lin}} = \frac{P_{\text{sig}}}{\sigma_q^2} \quad (2.24)$$

Oversampling by a factor M spreads quantization noise over a wider bandwidth, reducing in-band noise by 3 dB per doubling of M.

$$\text{SNR}_{\text{OS}} \approx 6.02N + 1.76 + 10\log_{10}(M) \quad (2.25)$$

2.7.2.2 Measurement Intervals

The time window over which incoming VCO pulses are counted. Longer intervals improves frequency resolution but increases conversion latency.

$$T_{\text{meas}} = N_{\text{ref}} T_{\text{ref}} \quad (2.26)$$

2.7.2.3 Frequency Resolution

The smallest detectable frequency step. It sets the quantization size, directly tied to conversion time.

$$f_{\text{res}} = \frac{1}{T_{\text{meas}}} \quad (2.27)$$

2.7.2.4 Linearity (INL, DNL)

DNL quantifies how evenly spaced an ADC's individual steps are compared to the ideal 1 LSB step size. For each code k , you compare the actual voltage difference between successive code transitions ($V_{k+1} - V_k$) to the ideal LSB. Good converters keep $|DNL[k]| < 1 \text{ LSB}$ so that they remain monotonic and never miss codes.

INL measures how far the ADC's actual transfer curve strays from a perfectly straight ideal line. At code K , it's the cumulative sum of all previous DNL errors (or equivalently the deviation of the actual code edge V_k from its ideal position). Keeping INL small (e.g. within

± 0.5 LSB) is crucial for precision applications, since it limits the maximum deviation from the ideal analog-to-digital mapping.

2.7.2.5 Effective Number of Bit(ENOB)

Effective Number of Bits quantifies an ADC's real-world resolution by relating its measured signal-to-noise-and-distortion ratio (SINAD) to the ideal quantization noise floor. It tells you how many bits of “perfect” resolution your converter effectively achieves when noise and non-idealities are included.

$$\text{ENOB} = \frac{\text{SINAD}_{\text{dB}} - 1.76}{6.02} \quad (2.28)$$

ENOB directly shows how many bits of performance your ADC truly delivers. Knowing ENOB lets you budget noise and distortion against your system’s precision requirements.

2.7.2.6 Spurious-Free Dynamic Range (SFDR)

SFDR measures the ratio between the amplitude of the fundamental signal and the amplitude of the largest undesired spectral spur (harmonic or distortion product) within the converter’s bandwidth. It indicates how well the ADC (or any frequency-converting system) can distinguish a desired tone from spurious tones, and thus its ability to handle low-level signals in the presence of distortion.

$$\text{SFDR}_{\text{dB}} = 20 \log_{10} \left(\frac{A_{\text{signal}}}{A_{\text{spur,max}}} \right) \quad (2.29)$$

SFDR often limits the usable dynamic range more than noise floor or ENOB in systems sensitive to distortion. SFDR tells how far below the carrier you can detect another signal without spur interference.

2.8 Chapter Summary

This chapter has provided a comprehensive review of the background and related works related to the design of a VCO-based ADC. The fundamental principles, architectures, limitations, and key design parameters for both Current-Starved Ring Oscillators (CSROs) and Frequency-to-Digital Converters (FDCs) have been detailed. Furthermore, the critical role and demanding requirements of ADCs in emerging biomedical applications, such as PPG and BMI systems, have been highlighted. This context underscores the motivation for developing power-efficient, compact, and reasonably accurate ADCs. The limitations of conventional approaches and the specific design considerations discussed here set the stage for the novel 4-bit VCO-based ADC architecture proposed and analyzed in the subsequent chapters of this thesis, which aims to address these challenges.

CHAPTER 3

DESIGN CONCEPT

3.1 Introduction

Building upon the foundational concepts of VCO-based Analog-to-Digital Converters (ADCs) and the review of existing techniques discussed in previous chapters, this chapter details the proposed 4-bit ADC architecture. The limitations of conventional Current-Starved VCOs (CSVCOs) and standard Frequency-to-Digital Converter (FDC) approaches, highlighted in Chapter 2, motivate the novel design elements presented here.

This chapter focuses on two primary contributions. First, it describes the design of the custom Voltage-Controlled Oscillator (VCO) that serves as the analog front-end. The proposed VCO, incorporates specific enhancements such as source degeneration and an integrated charge pump to improve linearity and phase noise. Second, the chapter details the design of the 4-bit FDC, with a comparative investigation of asynchronous (ripple) and synchronous binary counter implementations. The design of the associated 4-bit output register is also covered.

3.1.1 Proposed VCO

The frequency of a Ring Voltage-Controlled Oscillator (Ring VCO) is primarily dependent on node capacitance and transistor sizing because both factors directly impact the delay per stage, which determines the oscillation frequency as discussed before.

Each inverter output sees a load capacitance (node capacitance), which includes Parasitic capacitance of the transistors (gate, drain, diffusion) and explicitly added capacitors. Hence higher the node capacitance, the longer time it will take to charge and discharge and it will lead to a longer delay time and lower frequency. Therefore in this proposed VCO, each delay cell output node is introduced with 10fF (C) explicitly capacitance to achieve a suitable and wide frequency bandwidth.

In the proposed current starved ring VCO architecture, M11 and M22 are the global current starving component that regulates the total current flows through the entire VCO not in an individual stage. M11 is biased in such a way it acts as a voltage controlled current source and always operates in saturation region. If V_{ctrl} increases M11 limits the current flow into pMOS pull up transistors (M1, M3, M5) and directly impacts the rising edge slope and delay per stage. Similarly, M22 acts as voltage controlled current sink that allows more discharge current to flow when V_{ctrl} increases. It controls the pull down operation of nMOS transistors of each stage (M17, M19, M21). The current in each inverter stage defines the charging discharging rate of inverter output node, delay and oscillation frequency.

For the ADC purpose, to maintain this wide tuning range, delay of each stage need to be increased. Therefore capacitor load is used in each delay cell, then frequency bandwidth can be tuned as

$$t \propto \frac{C_{tot}}{I_d} \quad (3.1)$$

In our proposed VCO the total capacitance of three inverter stage is

$$C_{tot} = \frac{5}{2} C_{ox} (w_{pLp} + w_{nLn}) + C \quad (3.2)$$

$$C = C_1 = C_3 = C_5 \quad (3.3)$$

Transistor sizing affects how strong a transistor is and measure its ability to source or sink current. For MOSFET in saturation

Larger W/L will produce larger current. Thus it takes smaller time to charge and discharge of

node that implies to a higher frequencies.

Transconductance is a measure of how effectively a transistor converts a change in gate voltage into a change in drain current.

The delay of an inverter stage in a VCO is inversely related to the transconductance of the transistors because stronger drive capability allows the output node to charge/discharge faster.

To achieve the frequency range, we used a supply volt of 1.8V that will serve the purpose of VCO and compatibility with ADC.

$$t_{\text{delay}} \propto \frac{V_{DD}}{(V_{\text{ctrl}} - V_{th})^2} \quad (3.4)$$

Therefore the bandwidth is tuned in a well mannered and achieved the range from 39MHz to 697MHz which is sufficient for the condition. But variations in temperature can alter capacitance values and other characteristics, potentially compromising circuit stability. Parasitic inductance and resistance, can adversely affect performance, especially at high frequencies[33]. Achieving high capacitance values necessitates larger component sizes, which can be impractical in compact IC layouts[34]. For solving the issue, traditional capacitor is replaced with Pmos capacitor

Taking account all the parameters we tuned all the transistor size according to the table that is given below.

The issue of non-linearity of the current starved ring vco arises because of the non-linear behavior of drain current of current starved transistor with the controlling voltage. The nonlinear dependence of the drain current upon the overdrive voltage introduces excessive nonlinearity. The linear behavior of a CS stage can be accomplished by placing a “degeneration” resistor in series with the source terminal so as to make the input device more linear [35].

Device Number	Width	Length
M11	$1\mu\text{m}$	180nm
M1, M3, M5	900nm	180nm
M2, M4	$4\mu\text{m}$	180nm
M6-M10	$1\mu\text{m}$	100nm
M12-M16	500nm	100nm
M17, M19, M21	450nm	180nm
M18, M20	$2\mu\text{m}$	180nm
M22	500nm	180nm
M24-M28	$8.41\mu\text{m}$	180nm
M23	120nm	180nm

Table 3.1: Physical Dimension of Devices

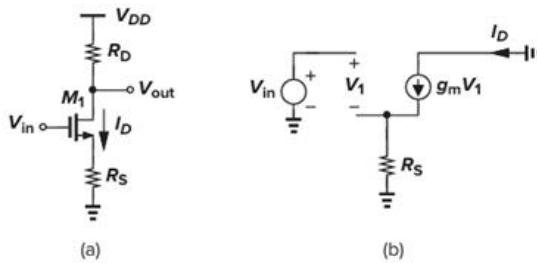
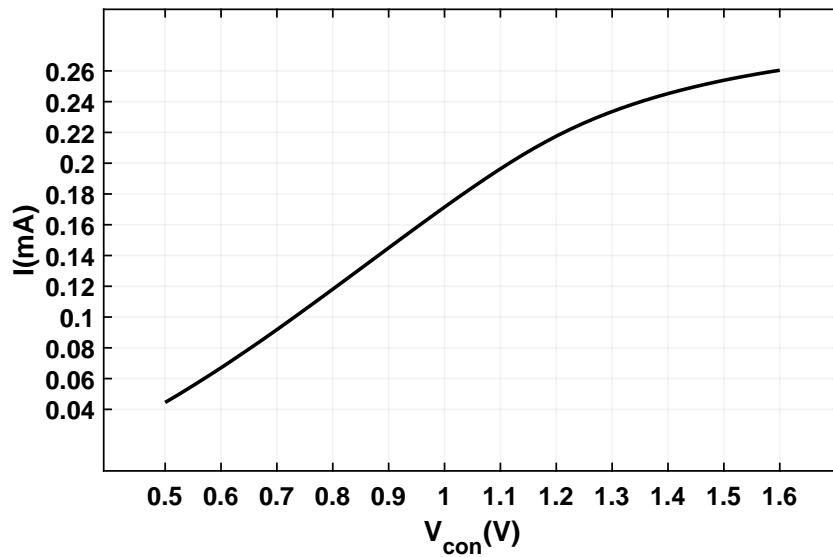
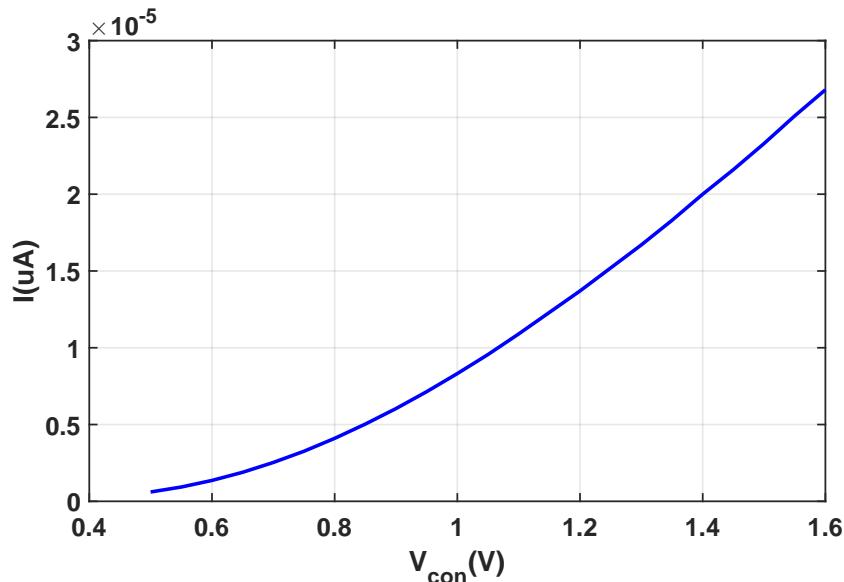


Figure 3.1: CS Stage a. Source degeneration b. Small signal analysis[35]

From the depicted figure it is clear that if control voltage increases it leads to increase the drain current and also the voltage across the resistor. The change in control voltage appears across the resistor more than the overdrive voltage. That implies a linear behavior of voltage and current. For increasing the resistance more, equivalent trans-conductance becomes a less dependent on g_m and hence the drain current becomes linear function.

The drain current saturates with the increasing voltage since the initial current is much higher. In Figure 3.2 current saturates after 1.1 voltage. But the source degeneration resistors (M23 - M28) limit the initial current to a much lower value and makes the current increasing linearly with increasing voltage shown in Figure 3.3 where the current is raising till 1.6 voltage.

Regarding fabrication process, maintaining a fix value with reasonable physical size is much

**Figure 3.2:** Voltage Current relation**Figure 3.3:** Voltage Current relation

more challenging. Also resistance is not a robust option against heat dissipation and power consumption. For solving the issue, diode connected load is applied shown in Figure 3.4. Interesting fact here, transistor will always be operated in saturation region

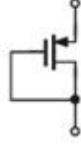


Figure 3.4: Diode Connected NMOS

3.2 Charge Pump and Phase Noise Reduction

Phase noise represents random fluctuations in the phase of the VCO's output signal, degrading its spectral purity and adversely affecting system performance. According to the linear time-varying (LTV) phase noise model of Lee and Hajimiri [36], the single-sideband phase noise density at an offset frequency Δf can be expressed as:

$$\mathcal{L}(\Delta f) = \frac{F k T}{2 P_s} \frac{1}{\Delta f^2} \left(\frac{\omega_0}{Q} \right)^2 |\Gamma(\theta)|^2, \quad (3.5)$$

where F is the noise factor of the active devices, k is Boltzmann's constant, T is absolute temperature, P_s is the oscillator's signal power, ω_0 the oscillation angular frequency, Q the resonator quality factor, and $\Gamma(\theta)$ denotes the impulse sensitivity function (ISF) over the oscillation phase θ . Equation (3.5) highlights that phase noise is minimized when noise is injected at points where $|\Gamma(\theta)|$ is small.

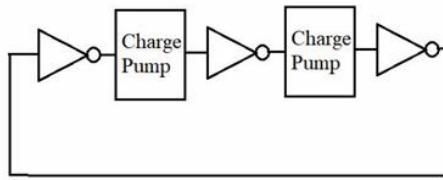


Figure 3.5: Charge Pump application in CSRVCO [17]

To exploit this theory, the proposed VCO incorporates charge pump stages in its 2nd and 4th delay cells (Fig. 3.5). Each such stage uses an inverter (M7/M13 or M9/M15) gated by current-starved pMOS (M2, M4) and nMOS (M18, M20) devices tied to GND and VDD. By delivering energy as short, controlled pulses rather than a continuous analog control volt-

age, the charge pump concentrates energy injection around the ISF minima, thereby sharply reducing the time during which the oscillator is vulnerable to noise upconversion.

Device-level operation can be described by the charge-injection relationship

$$I_p = C \frac{dV}{dt}, \quad C = C_2 = C_4, \quad (3.6)$$

where C_2 and C_4 are the node capacitances in the pump stages. An increased bias current I_p and reduced C yield a higher slew rate, thus sharpening the voltage edges, reducing zero-crossing uncertainty, and lowering timing jitter and phase noise.

Source degeneration resistors (M24, M26) further smooth these transitions by modulating the nMOS gate-source voltage according to the resistor's voltage drop. This controlled discharge yields transitions less sensitive to supply and thermal variations, narrowing the spectral width and decreasing phase noise.

Within the phase-locked loop context, the charge pump also drives the loop filter. Injected current I_{CP} over a time Δt produces a control voltage increment:

$$\Delta V_{ctrl} = \frac{I_{CP} \Delta t}{C_{LF}}, \quad (3.7)$$

where C_{LF} is the loop-filter capacitance. The resulting control voltage V_{ctrl} is smoothed by the $R-C$ network, with its noise spectral density $S_{V_{ctrl}}(f)$ directly shaping the VCO's phase noise via

$$S_\phi(f) = \left(\frac{K_{VCO}}{f}\right)^2 S_{V_{ctrl}}(f), \quad (3.8)$$

where K_{VCO} (Hz/V) is the VCO's sensitivity and f the Fourier frequency. By minimizing

$S_{V_{ctrl}}(f)$ through accurate current steering and matched up/down currents, the charge pump greatly suppresses control-voltage noise, which, when combined with the impulsive energy delivery at ISF minima, yields substantially improved phase noise performance.

Simulation results confirm that an optimally sized charge pump—providing large I_{CP} and minimal output capacitance—shifts the phase noise floor downward, particularly at close-in offsets critical for ADC accuracy. These findings align with the theoretical LTV model of Lee and Hajimiri [36], validating the effectiveness of the charge pump in our 4-bit VCO-based ADC architecture.

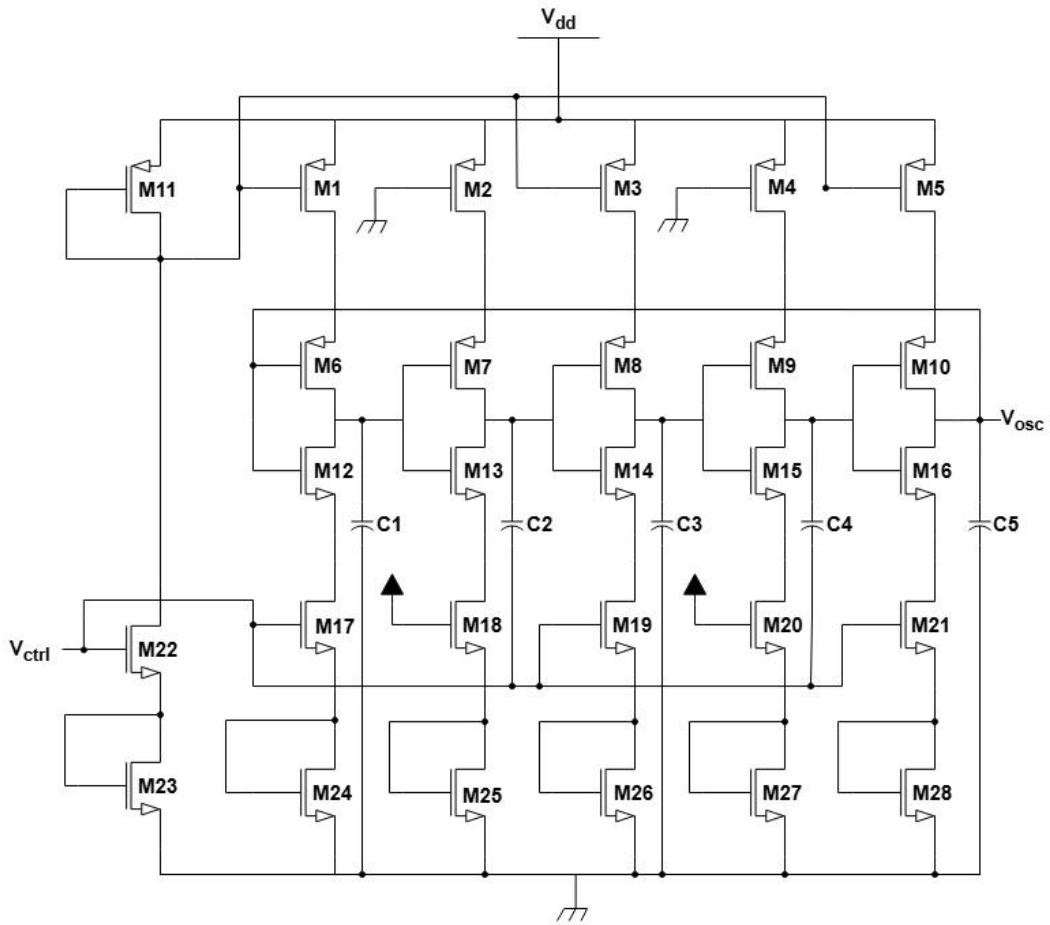


Figure 3.6: Proposed Current Starved VCO.

3.3 Design of the 4-bit Frequency-to-Digital Converter (FDC)

The Frequency-to-Digital Converter (FDC) serves as the crucial interface between the analog-domain frequency output of the Voltage-Controlled Oscillator (VCO) and the digital domain. Within the proposed 4-bit VCO-based ADC, the FDC is responsible for quantizing the VCO's output frequency (F_{out}) into a 4-bit digital word. This section details the design considerations and architecture of the FDC, with a particular focus on its core component: the 4-bit counter.

3.3.1 Role of the FDC in the 4-bit ADC

The primary function of the FDC, as depicted in the block diagram in Figure 2.2, is to convert the continuous frequency signal generated by the VCO into a discrete numerical representation. In a 4-bit ADC system, this means transforming the VCO's frequency into one of $2^4 = 16$ distinct digital levels. This conversion is typically achieved by counting the number of VCO output cycles (F_{out}) within a precisely defined sampling window, T_s . The F_{out} signal from the VCO acts as the input clock to the FDC's counter. The duration of T_s , often controlled by an external reference clock or timing signal, directly influences the resolution and range of the FDC.

The fundamental relationship governing the FDC's operation can be expressed as:

$$\text{Digital Output (Count)} \approx F_{out} \times T_s \quad (3.9)$$

Thus, the FDC effectively measures the average frequency of the VCO over the interval T_s . The stability and accuracy of this sampling window are paramount, as any jitter or variation in T_s will directly translate into conversion errors in the ADC output. The counter accumulates the pulses, and upon completion of the sampling window, its value is transferred to an output register, providing a stable 4-bit digital output. A reset signal is also essential to initialize the counter before each new conversion cycle.

3.3.2 4-bit Counter Design

The counter is the heart of the FDC, tasked with accumulating the incoming pulses from the VCO. For the 4-bit resolution targeted by this ADC, the counter must be capable of representing 16 unique states, typically corresponding to counts from 0 (0000_b) to 15 (1111_b). The choice of counter architecture involves trade-offs between speed, power consumption, and circuit complexity.

3.3.2.1 Fundamental Requirements for the 4-bit Counter

Beyond the basic requirement of cycling through 16 states, the 4-bit counter must satisfy several performance criteria. Primarily, its maximum operating frequency must be sufficiently high to correctly process the highest frequency output by the VCO (F_{VCO_max}). If the counter cannot keep pace with the incoming pulses, counting errors will occur, leading to ADC non-linearity or malfunction. Other considerations include the power dissipated by the counter, especially in low-power applications, and the silicon area occupied by its implementation. These factors guide the selection among different counter topologies, such as asynchronous, synchronous, or Gray code counters.

D-Flip-Flop Implementation Details The D-type flip-flop (D-FF) is a fundamental sequential logic element extensively used in digital systems for storing one bit of information and forming the basis of counters and registers. The symbol and truth table for the D-FF utilized in this work are presented in Figure 3.7. The D-FF has a data input (D), a clock input (CLK), an asynchronous reset input (R), and complementary outputs Q and Q'.

The gate-level schematic also provided in Figure 3.7 illustrates one possible implementation of such a D-flip-flop using NAND gates. This type of construction generally operates on the master-slave principle, which enables edge-triggered behavior. The structure consists of two cascaded latch stages: a "master" latch followed by a "slave" latch. The operational sequence ensures that the D-FF's output (Q) only changes state in response to the data at the D input

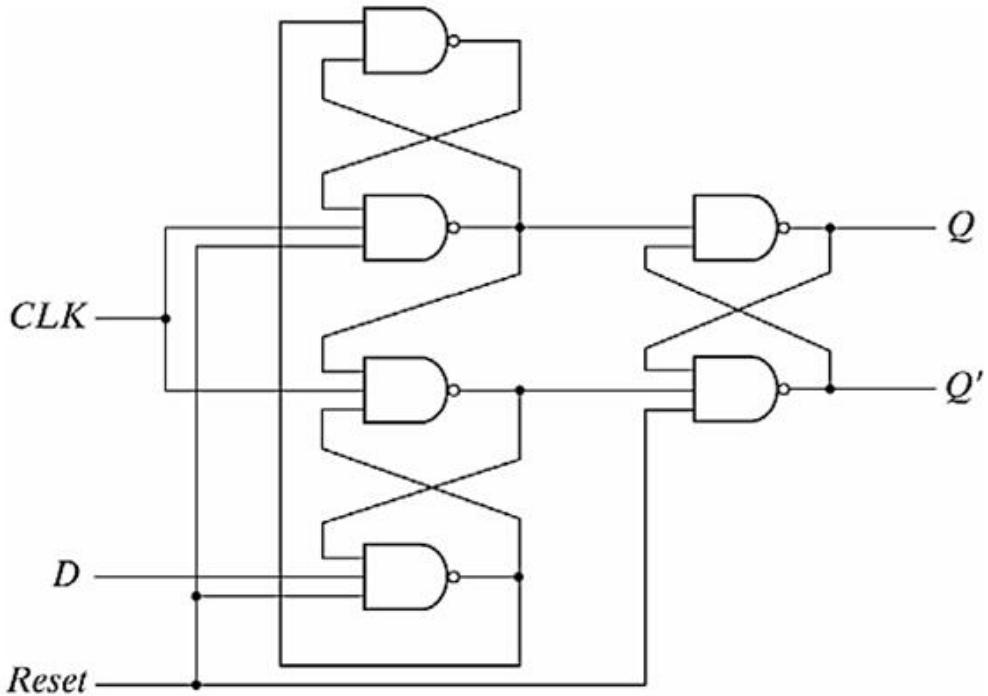


Figure 3.7: 6 NAND Gate D-Flip-Flop[5]

at a specific edge of the clock signal (e.g., the rising edge, as indicated by the ‘↑’ symbol in the truth table). For instance, if D is ‘1’ just before and during the active clock edge, Q will become ‘1’ after the edge. If D is ‘0’, Q will become ‘0’. Once the edge has passed, changes at the D input do not affect the output Q until the next active clock edge. The asynchronous Reset (R) input provides a mechanism to override the clocked operation and force the flip-flop into a known state. As shown in the truth table, when the Reset input is asserted (e.g., R=‘0’ for an active-low reset), the output Q is forced to ‘0’ and Q’ to ‘1’, irrespective of the D input or the clock signal. This feature is crucial for initializing counters and registers to a starting state. This D-flip-flop serves as the fundamental building block for the various counter architectures discussed subsequently.

3.3.2.2 Asynchronous (Ripple) Counter

An asynchronous counter, often referred to as a ripple counter, offers a straightforward approach to implementing the counting function. Its design simplicity is a key advantage. As illustrated in Figure 2.3, a 4-bit asynchronous ripple counter can be constructed by cascading

four D-type flip-flops (D-FFs), such as the one detailed in Figure 3.7.

In this configuration, each D-FF is set up to operate in toggle mode. This is commonly achieved by connecting the D input of the flip-flop to its complemented output (Q'). The output of the VCO (F_{out}) serves as the clock input (CLK) for the first flip-flop (FF0), which represents the Least Significant Bit (LSB, Q_0) of the counter. The complemented output (Q') of each flip-flop then drives the clock input of the subsequent flip-flop. For instance, Q'_0 clocks FF1 (generating Q_1), Q'_1 clocks FF2 (generating Q_2), and Q'_2 clocks FF3 (generating Q_3 , the Most Significant Bit, MSB). A common asynchronous Reset signal is applied to all flip-flops to initialize their outputs to ‘0’.

The operation relies on the toggling action propagating, or “rippling,” through the chain of flip-flops. Assuming positive edge-triggered D-FFs, FF0 toggles its state (Q_0) on every active edge of the input F_{out} . Subsequently, FF1 toggles its state (Q_1) when its clock input, driven by Q'_0 , experiences an active edge. This behavior continues for subsequent stages, with each flip-flop toggling at half the rate of the preceding one, effectively creating a binary up-counting sequence from $Q_3Q_2Q_1Q_0$.

The primary advantages of the asynchronous ripple counter are its simplicity in design, which translates to a smaller silicon footprint and easier implementation, and potentially lower static power in some states as not all flip-flops are actively switching with every input clock pulse.

However, asynchronous counters also possess inherent disadvantages. The most significant drawback is the cumulative propagation delay, often termed ripple delay. Since the clock signal for each stage (except the first) is derived from the output of the previous stage, the propagation delay of each flip-flop accumulates. This total delay limits the maximum input frequency the counter can reliably handle. Consequently, asynchronous counters are generally slower than their synchronous counterparts. Furthermore, during state transitions, the outputs of the flip-flops do not change simultaneously, which can lead to transient, incorrect output

values (glitches) if the counter outputs are directly fed into subsequent combinational logic for immediate decoding. For direct registration of the count, as in this FDC, this might be less critical if the register is latched after all outputs have settled, but it remains a characteristic of the architecture.

Despite these limitations, for applications where the maximum VCO frequency is moderate and design simplicity or low component count is prioritized, an asynchronous counter can be a viable option for the FDC. The schematic representation of such a 4-bit asynchronous counter, as might be implemented at the transistor or gate level using the D-FFs from Figure 3.7, is visualized in Figure 2.3.

3.3.2.3 Synchronous Counter

In contrast to the ripple counter, a synchronous counter employs a design methodology where all constituent flip-flops are triggered simultaneously by a common clock signal. This parallel clocking eliminates the cumulative propagation delay inherent in asynchronous designs, thereby allowing for significantly higher operating frequencies and more predictable timing behavior. The change of state for each flip-flop is determined by its current state and the states of other relevant flip-flops, orchestrated by dedicated combinational logic connected to the data inputs (D inputs in the case of D-Flip-Flops) of each flip-flop.

The proposed 4-bit synchronous counter, depicted in its entirety in Figure 3.8, is constructed using four D-type flip-flops (FF_A, FF_B, FF_C, FF_D), identical in structure to those described in Figure 3.7. These flip-flops produce the counter outputs Q_A, Q_B, Q_C , and Q_D . For the purpose of this description, Q_D will be considered the Least Significant Bit (LSB) and Q_A the Most Significant Bit (MSB) of the 4-bit count. All flip-flops share a common clock (CLK) input derived from the VCO's output (F_{out}), and a common asynchronous Reset input, ensuring synchronized state transitions and initialization.

The core of the synchronous counter's functionality lies in the specific combinational logic

circuits that generate the D input for each flip-flop. This logic dictates the next state of the counter based on its current state. The D input for each flip-flop (D_A , D_B , D_C , D_D) is determined by a set of Boolean equations, implemented using NAND gates as shown in the subsequent figures.

For the LSB flip-flop, FF_D , which drives the Q_D output, the data input D_D is simply the complemented output of the flip-flop itself:

$$D_D = \overline{Q_D} \quad (3.10)$$

This configuration ensures that FF_D toggles its state Q_D on every active edge of the common clock signal, a characteristic behavior of the LSB in a standard binary up-counter.

The data input D_C for the next flip-flop, FF_C , is generated by the combinational logic circuit illustrated in Figure 3.9. This circuit, composed of two 2-input NAND gates whose outputs feed into a final 2-input NAND gate, implements the following Boolean expression:

$$D_C = \overline{(Q_C \cdot \overline{Q_D})} \cdot \overline{(\overline{Q_C} \cdot Q_D)} \quad (3.11)$$

This logic simplifies to $D_C = (Q_C \cdot \overline{Q_D}) + (\overline{Q_C} \cdot Q_D)$, which is equivalent to $Q_C \oplus Q_D$ (Q_C XOR Q_D). This means Q_C will toggle its state if Q_D was '1' in the previous state and maintain its state if Q_D was '0', which is the typical behavior for the second bit in a binary counter.

Moving to the next stage, the data input D_B for FF_B is derived from the logic circuit shown in Figure 3.10. This circuit uses three 2-input NAND gates, with their outputs forming the inputs to a final 3-input NAND gate. The implemented equation is:

$$D_B = \overline{(\overline{Q_B} \cdot \overline{Q_D})} \cdot \overline{(Q_B \cdot \overline{Q_C})} \cdot \overline{(\overline{Q_B} \cdot Q_C \cdot Q_D)} \quad (3.12)$$

3.3 Design of the 4-bit Frequency-to-Digital Converter (FDC)

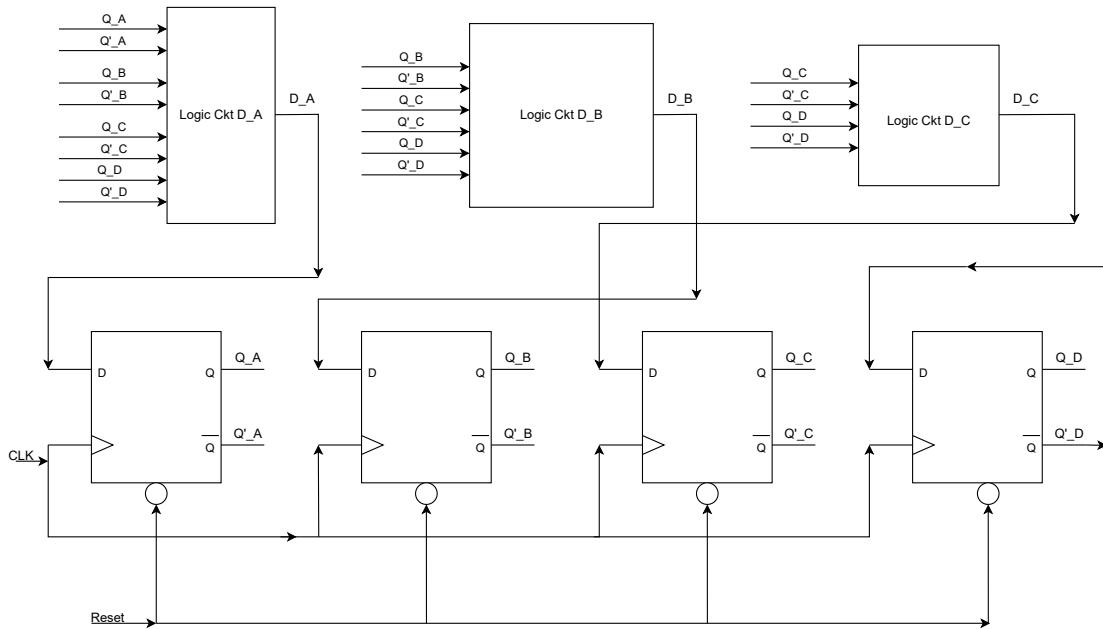


Figure 3.8: 4-bit synchronous counter.

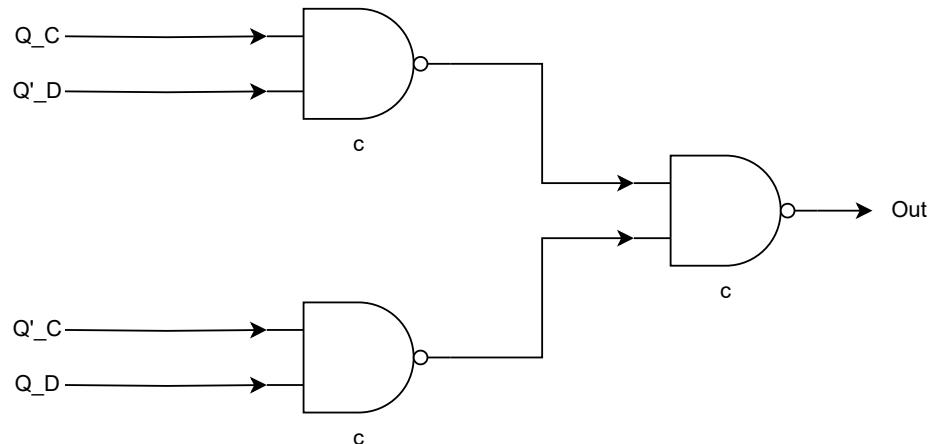


Figure 3.9: Combinational logic for D_C input of FF_C.

This configuration, upon simplification, realizes an expression equivalent to $D_B = (Q_B \cdot \overline{Q_D}) + (Q_B \cdot \overline{Q_C}) + (\overline{Q_B} \cdot Q_C \cdot Q_D)$. This logic determines when Q_B should toggle based on the current states of Q_B, Q_C, and Q_D. For a standard binary up-counter, D_B would typically be $Q_B \oplus (Q_C \cdot Q_D)$. The provided logic implements a more specific state transition.

Finally, the data input D_A for the MSB flip-flop FF_A is generated by the combinational circuit

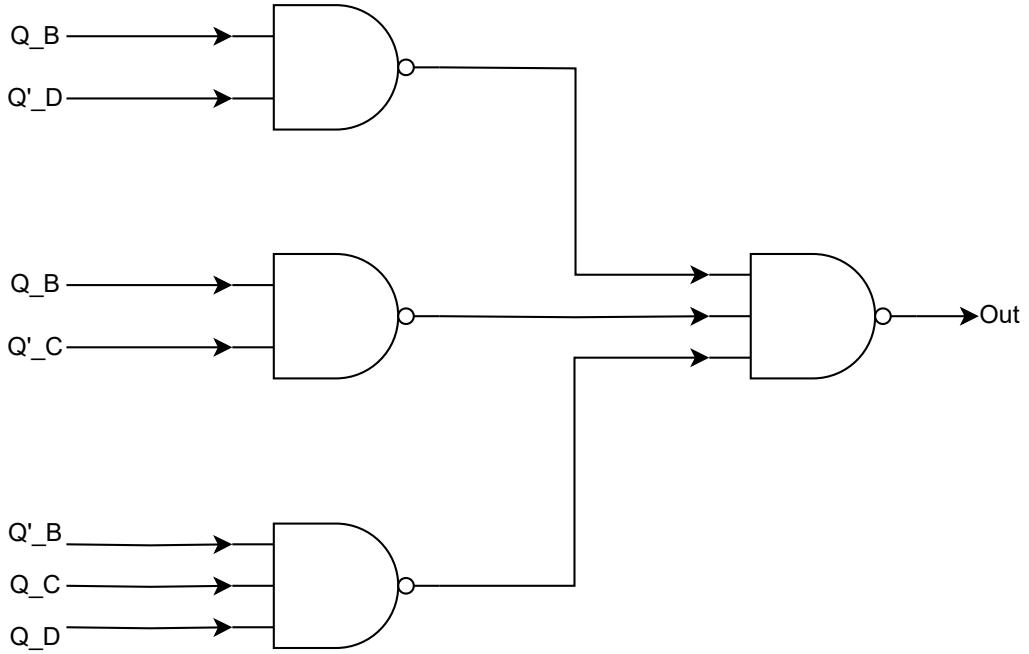


Figure 3.10: Combinational logic for D_B input of FF_B .

shown in Figure 3.11. This circuit comprises four 2-input NAND gates whose outputs feed into a 4-input NAND gate. The Boolean equation for this logic is:

$$D_A = \overline{(Q_A \cdot \overline{Q_C})} \cdot \overline{(Q_A \cdot \overline{Q_D})} \cdot \overline{(\overline{Q_A} \cdot Q_B \cdot Q_C \cdot Q_D)} \cdot \overline{(Q_A \cdot \overline{Q_B})} \quad (3.13)$$

This logic structure, once simplified, will yield an expression such as $D_A = (Q_A \cdot \overline{Q_C}) + (Q_A \cdot \overline{Q_D}) + (\overline{Q_A} \cdot Q_B \cdot Q_C \cdot Q_D) + (Q_A \cdot \overline{Q_B})$. This comprehensive logic dictates the next state of the MSB Q_A based on the complete current state of the counter (Q_A, Q_B, Q_C, Q_D). For a standard binary up-counter, D_A would typically be $Q_A \oplus (Q_B \cdot Q_C \cdot Q_D)$. The provided logic implements a more specific set of state transitions.

In operation, on each active edge of the common CLK signal, the current state of the counter (Q_A, Q_B, Q_C, Q_D) is fed into these combinational logic blocks. The logic blocks compute the next state values (D_A, D_B, D_C, D_D) almost simultaneously. These D values are then latched

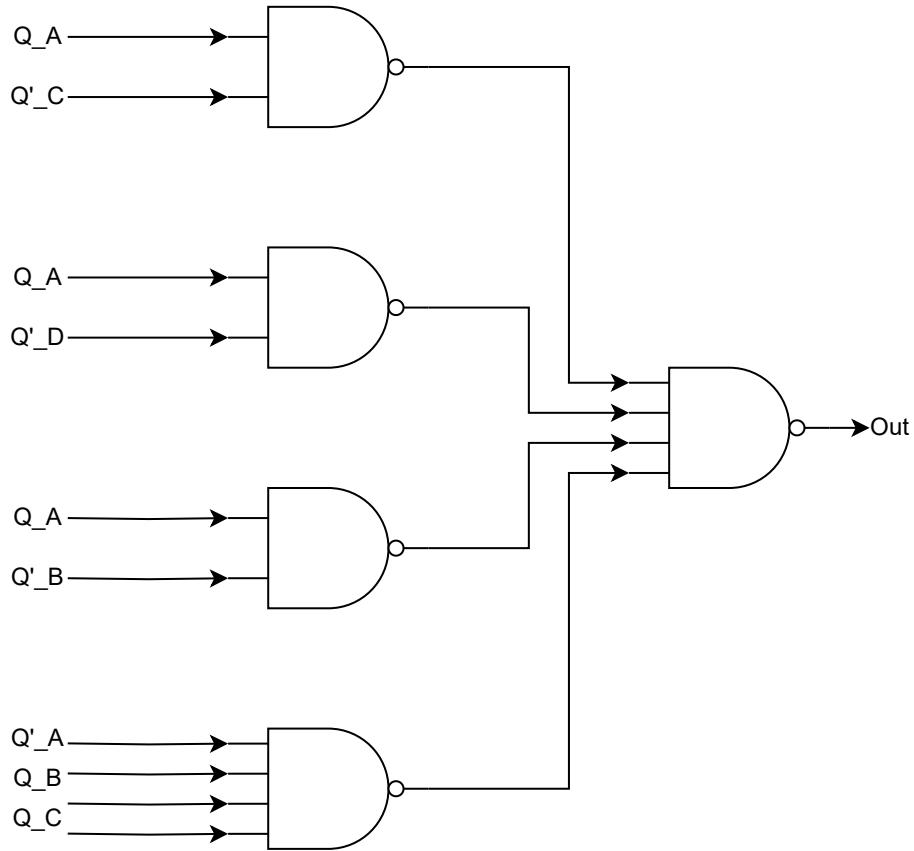


Figure 3.11: Combinational logic for D_A input of FF_A .

into their respective flip-flops, causing the counter to transition to its next state according to the designed sequence.

The principal advantages of this synchronous design are its higher operational speed and the absence of ripple delay. Since all flip-flops are clocked together, the maximum operating frequency is determined by the propagation delay through a single flip-flop plus the delay through the most complex combinational logic path feeding any D input, rather than the sum of all flip-flop delays. Furthermore, synchronous counters are inherently free from the decoding glitches associated with the staggered output changes of ripple counters, as all outputs change (or remain stable) in synchrony with the clock edge.

However, these benefits come at the cost of increased circuit complexity due to the additional combinational logic required to generate the D inputs for each flip-flop. This can lead to a larger silicon area and potentially higher dynamic power consumption compared to a simple ripple counter, as more gates may be switching during each clock cycle. The specific design of the combinational logic, as detailed by the equations and figures above, ensures the counter progresses through its intended sequence.

3.3.3 4-bit Output Register

Following the counting operation performed by the 4-bit counter (whether asynchronous, synchronous, or Gray code), an output register is essential to capture and hold the resulting digital count. This register provides a stable 4-bit digital output (D_{out}) for the ADC, isolating it from the potentially rapidly changing internal state of the counter as it proceeds through subsequent counting cycles or resets. The stability of this output is crucial for interfacing with downstream digital processing stages or for direct digital readout.

The 4-bit output register, as depicted in the circuit schematic in Figure 3.12, is implemented using four D-type flip-flops, structurally similar to those employed in the counter designs (see Figure 3.7). Each D-flip-flop in the register is dedicated to storing one bit of the 4-bit count. The Q outputs of the counter stages (e.g., Q_A, Q_B, Q_C, Q_D from the synchronous counter, or Q_3, Q_2, Q_1, Q_0 from an asynchronous counter) are connected to the respective D inputs of the flip-flops forming the register (labeled as D0, D1, D2, D3 in Figure 3.12, corresponding to the data inputs of the register's flip-flops).

All flip-flops within the output register share a common clock input, distinct from the VCO's output frequency that clocks the counter. This register clock, often referred to as a latch enable (LE) or sampling clock, is synchronized with the completion of the FDC's sampling window (T_s). Upon an active edge of this register clock, the 4-bit data present at the D inputs (i.e., the final count from the counter) is transferred to the Q outputs of the register's flip-flops (labeled Q0, Q1, Q2, Q3 in Figure 3.12, representing the final 4-bit digital output of the ADC). These

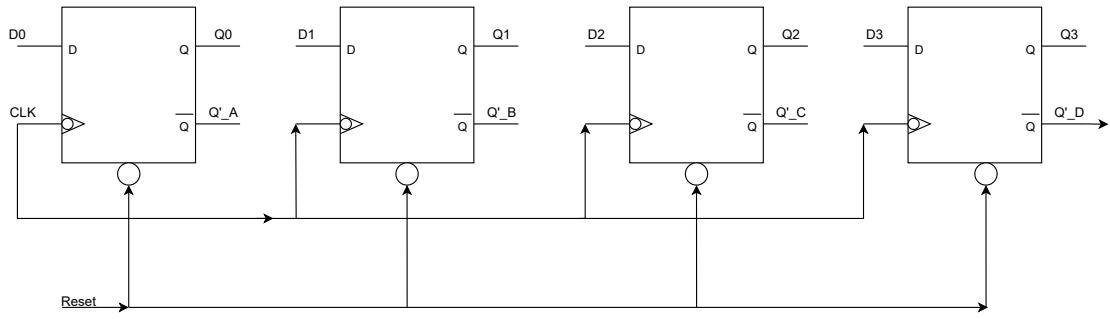


Figure 3.12: 4-bit output register

Q outputs then maintain their state until the next active edge of the register clock, regardless of any subsequent changes at the counter's outputs.

The register also incorporates a common asynchronous Reset input, typically tied to the same system reset signal used for the counter. This ensures that the output register can be initialized to a known state (usually all zeros) at the beginning of operation or upon a system reset. The use of D-flip-flops ensures a straightforward and reliable mechanism for parallel data storage, providing a clean and stable 4-bit digital representation of the analog input voltage after the VCO and FDC conversion process.

3.3.3.1 Comparative Analysis and Rationale for Investigating Implemented Counter Types

The selection of an appropriate counter architecture for the FDC is a critical design decision, influenced by factors such as the maximum operating frequency of the VCO, power consumption constraints, allowable circuit complexity, and susceptibility to timing hazards. The two counter types detailed in this chapter—asynchronous (ripple) and synchronous (binary)—present distinct advantages and disadvantages. These differences are expected to translate into varying performance characteristics when each is integrated into the overall 4-bit VCO-based ADC.

Asynchronous ripple counters, as discussed, offer the simplest implementation and potentially the lowest static power consumption due to their minimal gating logic. However, their primary

drawback is the speed limitation imposed by the cumulative propagation delay of the clock signal rippling through the flip-flop stages. This characteristic may pose a challenge to the ADC's ability to accurately process the highest frequencies generated by the wideband VCO.

In contrast, synchronous counters, while entailing greater complexity due to the additional combinational logic required for state generation, provide significantly higher operating speeds and inherently glitch-free outputs because all flip-flops are clocked simultaneously by the VCO's output. This architecture is generally anticipated to offer more robust performance for high-speed applications and precise timing requirements.

A qualitative comparison of these two counter types for the 4-bit FDC application is summarized in Table 3.2

Parameter	Asynchronous (Ripple)	Synchronous (Binary)
Max. Speed	Low - Moderate	High
Complexity	Low	Moderate - High
Power (Dynamic)	Moderate	Potentially Higher
Glitches	Prone if decoded directly	Glitch-free outputs
Switching Noise	Staggered	Simultaneous
Area	Smallest	Larger

Table 3.2: Comparative Analysis of 4-bit Counter Architectures.

Given the distinct trade-offs associated with these two counter architectures and the objective of comprehensively evaluating the performance of the proposed 4-bit VCO-based ADC, it is deemed insightful to design and investigate FDC implementations utilizing both asynchronous (ripple) and synchronous (binary) counter types. The wideband nature of the VCO (up to 619 MHz post-layout) poses a particular challenge for the asynchronous counter's speed capabilities. By implementing and simulating the ADC with each of these counter types, their respective impacts on key ADC performance metrics such as maximum operating frequency,

power consumption, linearity (ENOB, SFDR), and overall noise performance can be empirically determined and compared. This comparative study, which will be presented in Chapter 4, will provide valuable insights into the optimal FDC design choice based on specific application priorities (prioritizing maximum operational speed versus minimizing power consumption or silicon area). The specific asynchronous and synchronous binary counter designs detailed in sections 3.4.2.2 and 3.4.2.3, respectively, will form the basis for these distinct FDC implementations.

3.4 Experimental methodology

3.5 Chapter Summary

This chapter has detailed the architecture and design elements of the proposed 4-bit VCO-based Analog-to-Digital Converter. The ADC leverages a novel five-stage current-starved ring VCO featuring diode-connected NMOS source degeneration for enhanced V-F linearity and an integrated charge pump technique for reduced phase noise. This VCO serves as the analog front-end, converting the input voltage to a proportional frequency.

The subsequent Frequency-to-Digital Converter (FDC) stage has been explored with two distinct counter architectures: asynchronous (ripple) and synchronous (binary). Each counter type, designed to quantize the VCO's output frequency, presents different trade-offs in terms of speed, complexity, and potential noise characteristics. These counters are followed by a 4-bit output register to provide a stable digital output. The design considerations for interfacing these blocks, managing the timing and control logic, and mapping the VCO's wide tuning range to the 4-bit ADC resolution have been discussed.

The chapter also highlighted key design trade-offs concerning performance metrics such as linearity, phase noise, speed, power consumption, and area. The proposed approach involves implementing and comparing the overall ADC performance with each of these two FDC counter configurations to provide a comprehensive understanding of their impact. The subse-

quent chapter will present simulation results and a detailed comparative performance analysis of the 4-bit VCO-based ADC utilizing these different FDC designs.

CHAPTER 4

SIMULATION RESULTS AND DISCUSSIONS

4.1 Introduction

The simulation results of the ADC demonstrate how it performs and functions in various operating scenarios. The document provides a summary of the simulation and post layout outcomes showcasing the efficiency and robustness of the ADC design. The simulation was carried out using Cadence Virtuoso in the gpdk 90nm process. Various aspects of the ADC were thoroughly investigated, including transient analysis, frequency synthesis, DC power consumption, phase noise, process corner analysis, temperature sweeping, and Monte Carlo analysis. According to the simulation results, the ADC design can meet rigorous performance criteria and be integrated into Biomedical application. The importance of using simulation-based assessment in ADC design development and optimization for real-world deployment is highlighted by these findings. The performance of VCO and VCO based ADC is analyzed separately.

4.2 VCO Performance

The proposed architecture of VCO is designed and simulated in 90 nm CMOS process technology in the cadence virtuoso environment. Transient analysis, pss, phase-noise and DC analysis have been performed on the schematic design and also post layout design to measure the performance attributes of the proposed topology.

4.2.1 Transient Analysis

Figure 4.1 displays the transient output voltage of your current-starved ring VCO over a 100 ns time window. The oscillation starts with a higher initial peak reaching approximately 1.1V, then settles into a more stable pattern. The waveform consists of repeating pulses with sharp rising edges and somewhat slower, more rounded falling edges. The non-50% duty cycle in a

current-starved ring VCO typically arises from an asymmetry in the charging and discharging currents through the inverter stages. In a current-starved design, separate PMOS and NMOS transistors (controlled by a bias voltage) limit the current available to charge (pull-up via PMOS) and discharge (pull-down via NMOS) the load capacitance of each stage. Sharp rise and slower fall suggest the pull-up current is likely stronger or less restricted than the pull-down current.

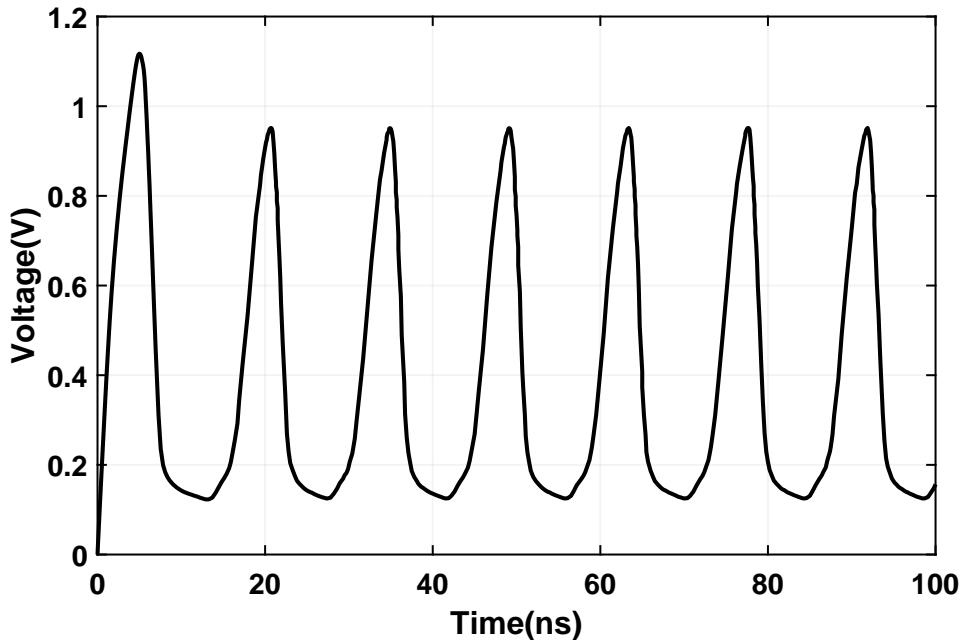


Figure 4.1: Transient response at $V_{con}= 0.6V$ (Post layout)

4.2.2 Periodic Steady State (PSS) Analysis

Figure 4.2, illustrates a reasonably linear relationship between oscillation frequency and gradually increasing control voltages from 0.52 V to 1.6 V, maintaining a wide tuning range from 39 to 697 MHz in schematic and from 38 to 619 MHz in post layout. The lowest frequency defines the oscillation frequency of the VCO, while the highest frequency satisfies the condition of being 16 times of the oscillation frequency.

The tuning characteristic of the current-starved ring Voltage-Controlled Oscillator (VCO) is presented in Figure 4.2. This graph plots the oscillation frequency in Gigahertz (GHz) against the applied control voltage (V_{con}) in Volts, which ranges from approximately 0.5 V to

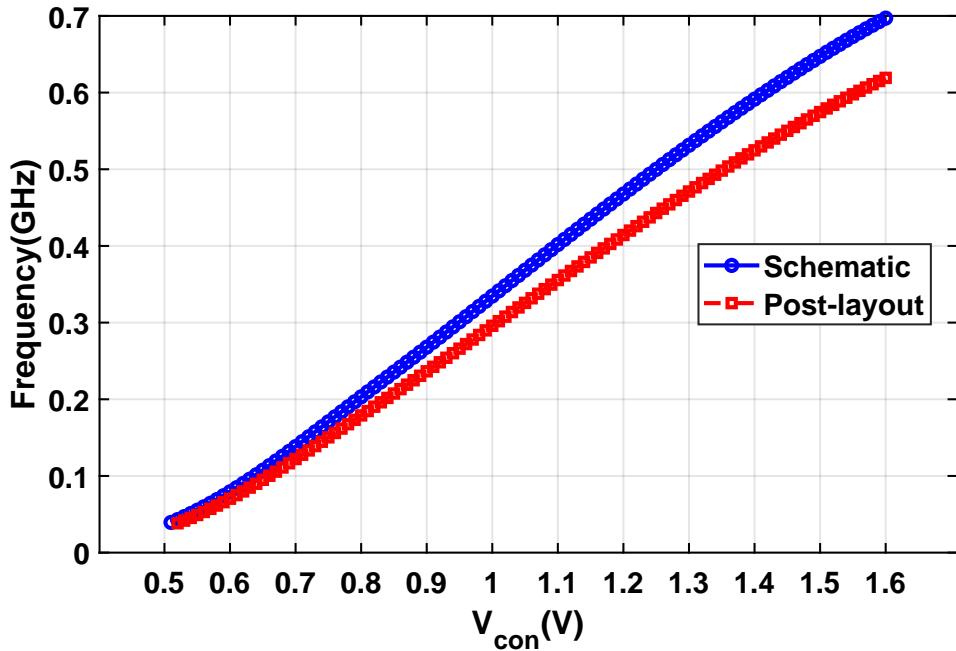


Figure 4.2: Oscillation frequency for different control voltages.

1.6 V. Two distinct curves are shown: the blue curve (marked with circles) represents the ideal schematic-level simulation results, indicating a frequency range from approximately 39 MHz to 697 MHz. The red curve (marked with squares) depicts the post-layout simulation results, showing a frequency range from approximately 38 MHz to 619 MHz. For both simulations, the frequency increases with higher V_{con} as expected, due to increased current delivery to the inverter stages which reduces their propagation delay. The notable reduction in the maximum achievable frequency, and a general downward shift across the entire operating range for the post-layout simulation, is primarily attributed to the inclusion of parasitic capacitances and resistances. These parasitics, introduced by the physical layout of interconnects, vias, and device proximities, effectively increase the load capacitance at the output of each inverter stage. This increased load leads to a longer propagation delay per stage, thereby lowering the overall oscillation frequency.

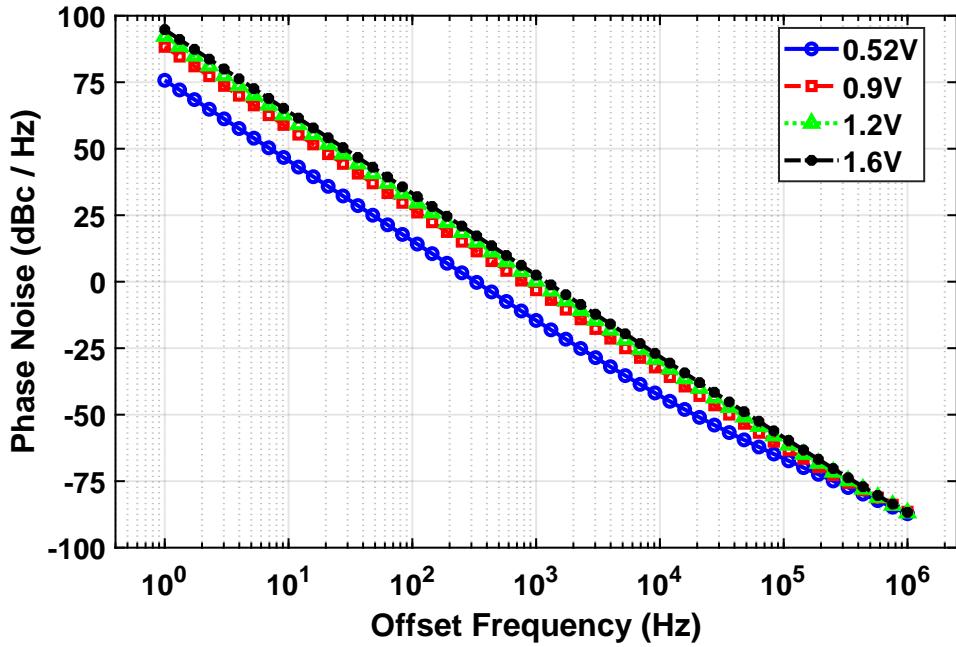


Figure 4.3: Phase noise for different ctrl Voltage (Post Layout).

4.2.3 Phase Noise Analysis

Figure 4.3 illustrates the post-layout simulated phase noise (in dBc/Hz) at offset frequency (Hz) for different control voltages. All exhibiting the characteristic downward slope with increasing offset. The data indicates that phase noise performance is generally best (lowest) at the lowest control voltage of 0.52V, and slightly degrades (increases) as the control voltage rises through 0.9V, 1.2V, and 1.6V. Specifically, the stated phase noise variation from -88.63 dBc/Hz (for 0.52V) to -87.66 dBc/Hz (for 1.6V) corresponds to the values observed at a 1 MHz offset frequency, confirming this trend. This behavior suggests that for this VCO design, the detrimental effects of increased thermal noise associated with higher currents at larger control voltages outweigh potential phase noise benefits from faster switching or increased signal swing, leading to slightly better phase noise at lower operating frequencies and currents within this tested range.

The figure of merit, FOM (in dBc/Hz), incorporating three basic performance parameters is

calculated by the following equation [37],

$$FOM = L(\Delta\omega) + 10 \log \left(\frac{P_{\text{diss}}}{1 \text{ mW}} \right) - 20 \log \left(\frac{\omega_o}{\Delta\omega} \right)$$

Where,

$L(\Delta\omega)$ = Phase noise at offset frequency

P_{diss} = Power dissipation

ω_o = Oscillation frequency

Oscillation center frequency is 329MHz. Phase noise and DC power consumption at corresponding frequency is -87.92 dBc/Hz and 524.4uW. That exhibits the FOM of VCO is -141.15 dBc/Hz.

4.2.4 Analysis For Different Process Corner

The robustness of the current-starved ring VCO to manufacturing process variations is evaluated through simulations across different process corners, as depicted in Figure 4.4 and Figure 4.5. Figure 4.4 illustrates the oscillation frequency in Gigahertz (GHz) as a function of the control voltage (V_{con}) for four distinct corners: FF (Fast PMOS, Fast NMOS), FS (Fast PMOS, Slow NMOS), SS (Slow PMOS, Slow NMOS), and SF (Slow PMOS, Fast NMOS). As anticipated, the FF corner consistently yields the highest operating frequencies for a given V_{con} due to the faster transistor characteristics, while the SS and SF corners result in the lowest frequencies. Despite these absolute frequency shifts inherent to process variations, the VCO maintains a broad tuning range across all corners, where the maximum achieved frequency is approximately sixteen times larger than the minimum frequency. This wide operational spectrum is critical for meeting the requirements of the intended Analog-to-Digital Converter (ADC) application, ensuring sufficient coverage despite process-induced deviations.

Complementing this, Figure 4.5 presents the phase noise in dBc/Hz versus offset frequency in Hertz (Hz) for the same four process corner conditions. A key observation is the remarkable

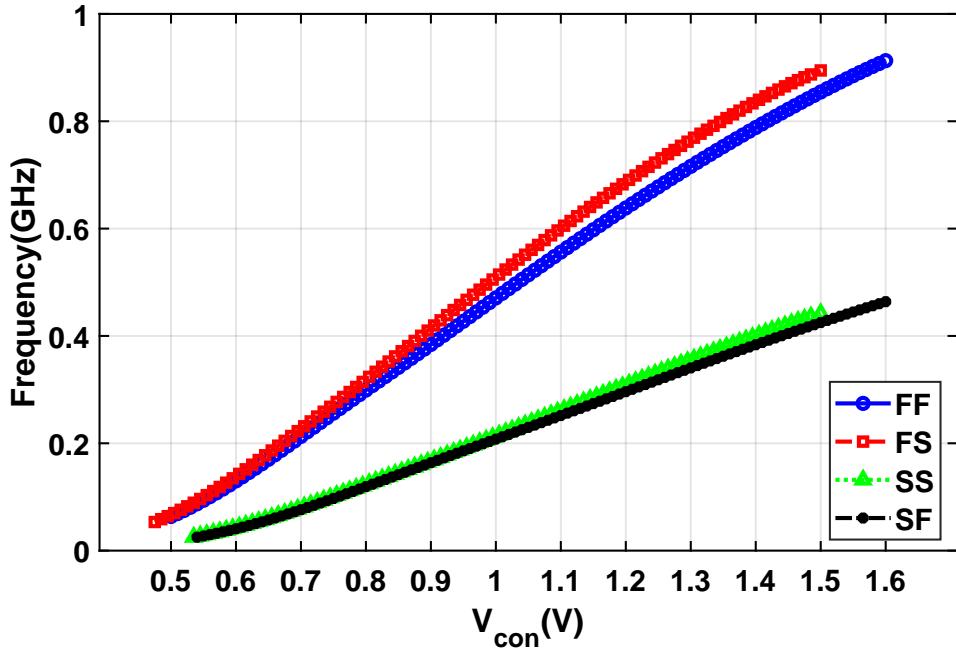


Figure 4.4: Oscillation frequency vs. Vctrl for different corner conditions.

consistency of the phase noise profiles; the curves for all four corners (FF, FS, SS, SF) are virtually indistinguishable, overlapping almost perfectly. This demonstrates excellent phase noise stability and robustness against process variations, ensuring that the VCO's noise contribution to the ADC system (impacting metrics like SNR and ENOB) remains predictable and stable regardless of manufacturing variability. The characteristic phase noise slopes are maintained across all corners, indicating a well-designed VCO resilient to process-induced changes in its fundamental noise behavior.

4.2.5 Analysis For Different Temperature

Figure 4.6 plots the oscillation frequency of the current-starved ring VCO as a function of the control voltage (V_{con}) under four different operating temperatures: 65°C, 45°C, -45°C, and -65°C. A key observation is the impact of temperature on the absolute frequency: at any given V_{con} , lower temperatures (-65°C and -45°C) result in significantly higher oscillation frequencies compared to higher temperatures (45°C and 65°C). This is primarily due to the temperature dependence of transistor characteristics, where carrier mobility often decreases with increasing temperature, leading to slower switching speeds and thus lower frequencies.

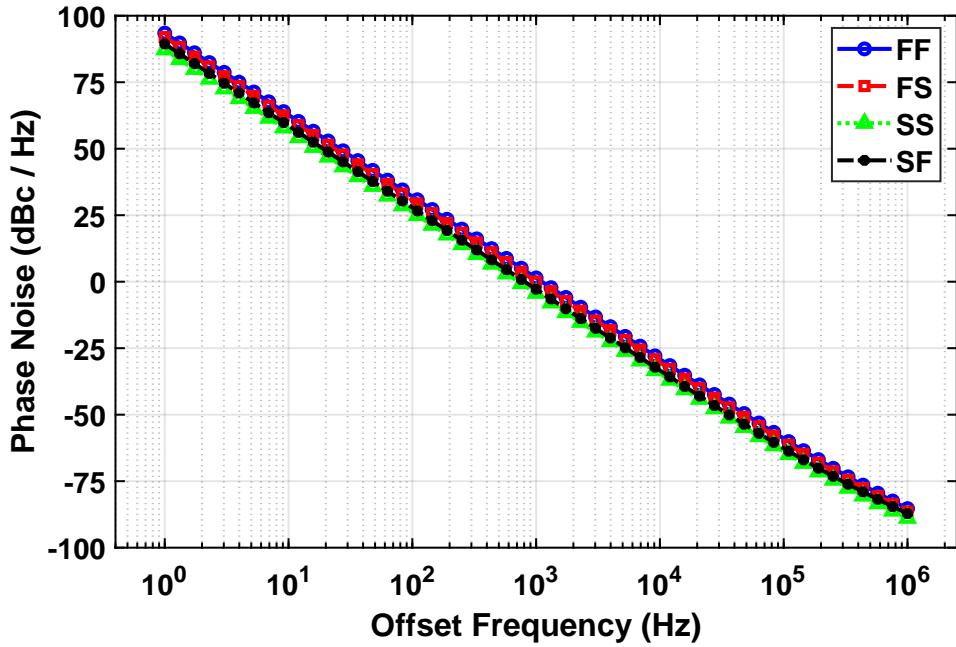


Figure 4.5: Phase noise vs offset frequency for different corner condition.

Conversely, at lower temperatures, mobility increases, leading to faster operation. Despite these absolute shifts in the frequency tuning curves due to temperature variations, the graph demonstrates that the VCO maintains a suitable and wide frequency tuning range at all tested temperatures. This ensures that the VCO can still cover the necessary operational spectrum required by the ADC, even under varying thermal conditions, which is crucial for robust system performance.

Figure 4.7 displays the phase noise performance (in dBc/Hz) of the VCO versus the offset frequency for the same four operating temperatures. The most striking feature of this graph is that all four phase noise curves, representing the different temperatures, are virtually indistinguishable and overlap almost perfectly across the entire plotted offset frequency range from 1Hz to 1MHz. This indicates that the phase noise of the VCO is very stable and exhibits excellent robustness against temperature variations. Despite the significant changes in absolute oscillation frequency with temperature, the fundamental noise characteristics of the oscillator remain remarkably consistent. This is a highly desirable outcome, as it implies that the VCO's contribution to the overall noise of the ADC system will be predictable and sta-

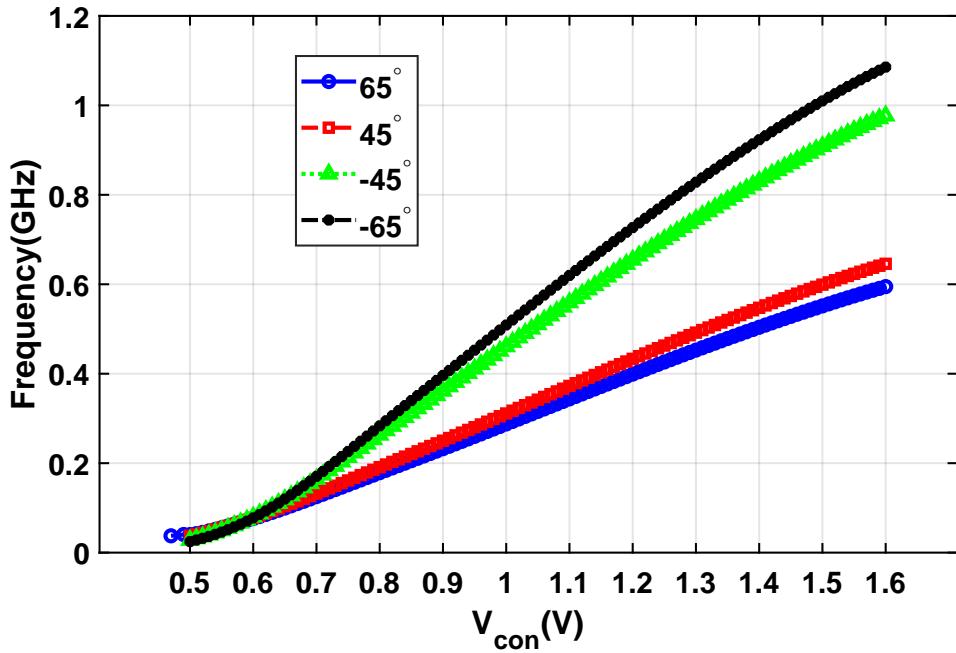


Figure 4.6: Oscillation frequency vs control voltage for different temperatures.

ble, regardless of the operating temperature, thereby ensuring consistent ADC performance metrics like Signal-to-Noise Ratio (SNR) and Effective Number of Bits (ENOB).

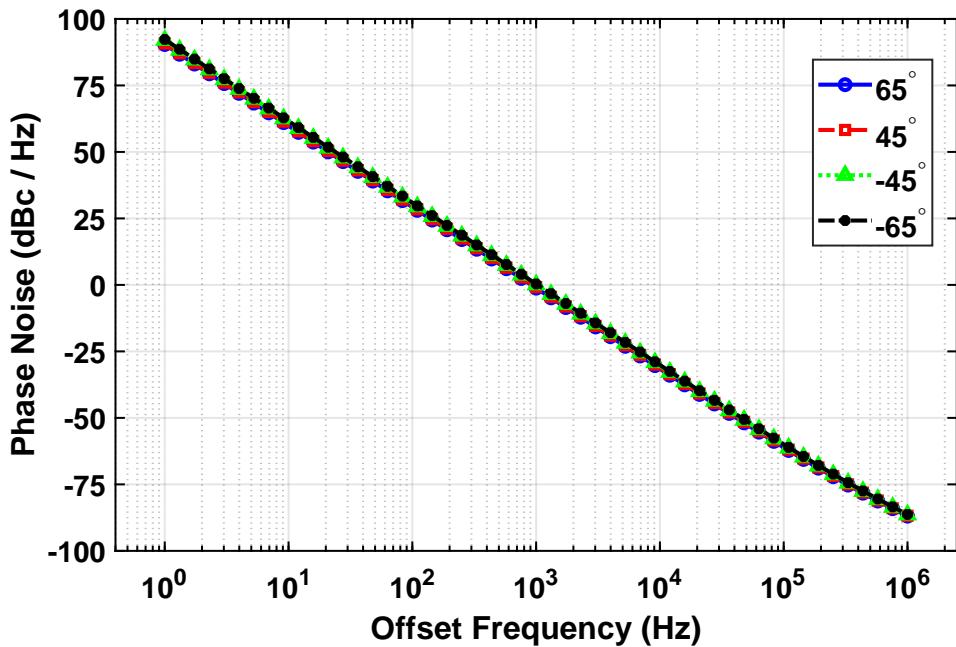


Figure 4.7: Phase noise vs offset frequency for different temperature.

4.2.6 Charge Pump Performance Analysis

The figure 4.8 presents a comparative analysis of the phase noise performance between a proposed VCO incorporating a charge pump and a conventional VCO design without one, specifically under what is stated to be a worst-case scenario. The graph plots phase noise in dBc/Hz against offset frequency, ranging from 100 kHz to 1 MHz. The blue solid line, representing the proposed VCO with the charge pump, consistently demonstrates superior phase noise across the entire plotted offset frequency range compared to the red dashed line, which represents the conventional VCO. This highlights the beneficial impact of the integrated charge pump on mitigating phase noise. At the 1 MHz offset frequency, which often serves as a key metric, the proposed VCO with the charge pump achieves a phase noise of -86.73 dBc/Hz. In contrast, the conventional VCO without the charge pump exhibits a poorer phase noise of -84.59 dBc/Hz under the same worst-case conditions. This specific comparison at 1 MHz offset clearly quantifies an improvement of approximately 2.14 dB, underscoring that the inclusion of the charge pump in the proposed VCO design leads to a more stable and improved phase noise profile, even in challenging operational scenarios.

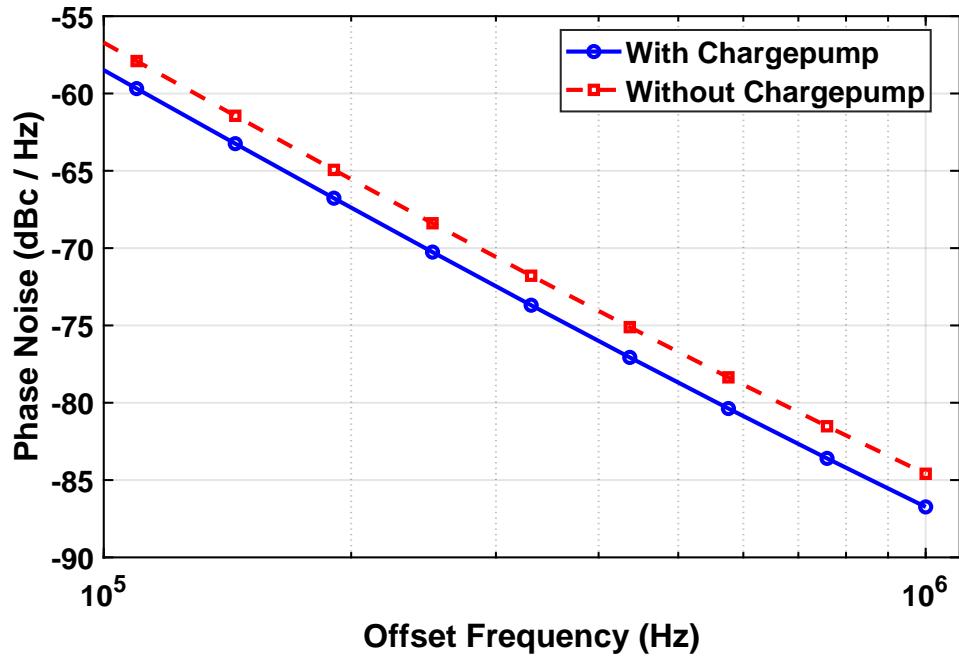


Figure 4.8: Phase Noise difference with conventional and proposed VCO

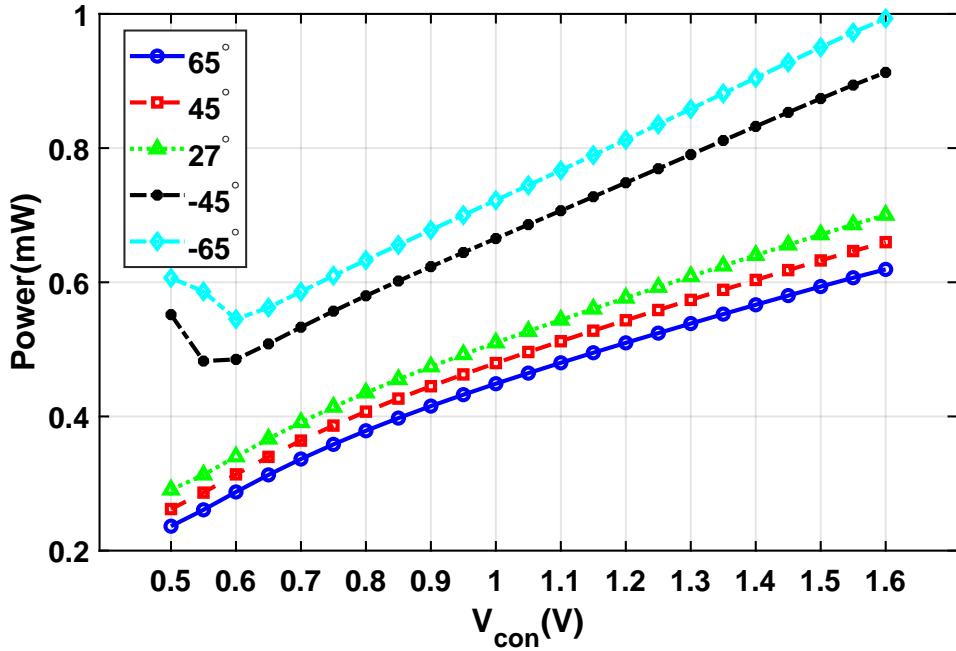


Figure 4.9: DC Power consumption vs tuning voltage for different temp.

4.2.7 DC Power Consumption

The figure 4.9 illustrates the DC power consumption (P) of the VCO as a function of the control voltage (V_{con}) across a range of operating temperatures. Generally, for the warmer temperatures (65, 45, and 27), the power consumption exhibits a monotonic increase as V_{con} rises from 0.5V to 1.6V. This trend is expected, as a higher V_{con} typically increases the current supplied to the oscillator's core stages, leading to greater power dissipation ($P = V_{\text{supply}} \times I_{\text{avg}}$). For the colder temperatures (-45 and -65), the behavior is more nuanced; power consumption initially shows a slight dip as V_{con} increases from 0.5V to approximately 0.6V, after which it follows the general trend of increasing power with increasing V_{con} . This behavior can primarily be explained by the temperature dependence of transistor threshold voltages (V_t). As temperature decreases, the V_t of MOS transistors typically decreases. Consequently, for the same gate control voltage (V_{con} applied to the current-starving transistors), the overdrive voltage ($V_{gs} - V_t$) effectively increases, leading to higher drain current through these devices and thus increased overall power consumption. Therefore, the VCO consumes more DC power at colder temperatures for a fixed control voltage due to these fundamental device physics.

4.2.8 Statistical Analysis

Monte Carlo simulations are crucial in integrated circuit (IC) design because manufacturing processes are not perfect. There are inherent, unavoidable variations in parameters like transistor threshold voltages, oxide thickness, doping concentrations, and interconnect dimensions. These variations, known as process variations, mean that no two manufactured chips, even from the same wafer, will be exactly identical. It randomly varies the relevant device and process parameters according to their known statistical distributions and shows what percentage of fabricated chips will meet the desired specifications. It shows how sensitive the design is to these variations. A narrow distribution for a parameter indicates a robust design, while a wide distribution suggests high sensitivity and potentially low yield.

Figure 4.10 displays the statistical distribution of the DC power consumption of your VCO when the control voltage is fixed at 1.05V, across 200 Monte Carlo simulation runs. The distribution is roughly bell-shaped, centered around a mean value. The histogram shows that while the nominal design might target a specific power, the actual power will vary, with most instances falling between approximately 480 μW and 570 μW .

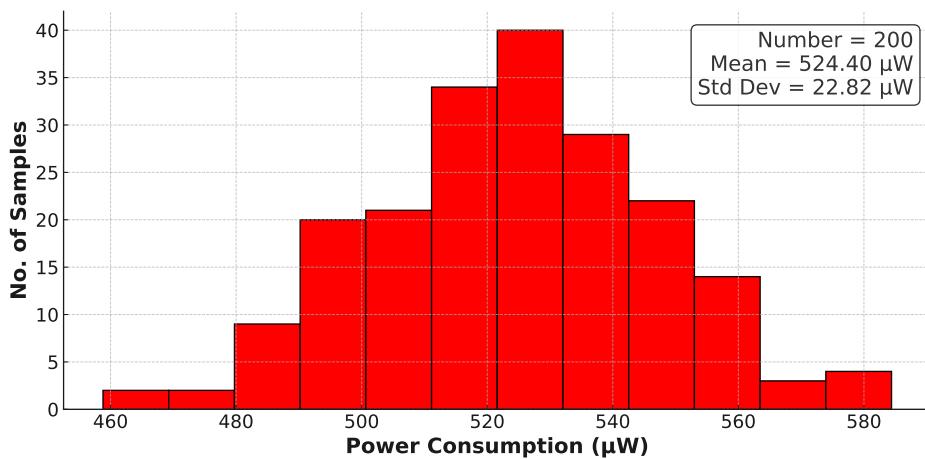


Figure 4.10: Statistical analysis of DC power consumption for $V = 1.05\text{V}$

Figure 4.11 histogram displays the statistical distribution of the VCO's phase noise at a fixed control voltage of 1.05V, across 50 Monte Carlo simulation runs. The distribution shows how

phase noise varies due to process variations. Mean is -87.81 dBc/Hz which is the average phase noise value expected. Std Dev is 0.40 dBc/Hz, indicating that the phase noise performance is quite robust against the simulated process variations. Most instances will have phase noise very close to the mean. The histogram shows that most instances have phase noise between approximately -88.50 dBc/Hz and -87.25 dBc/Hz.

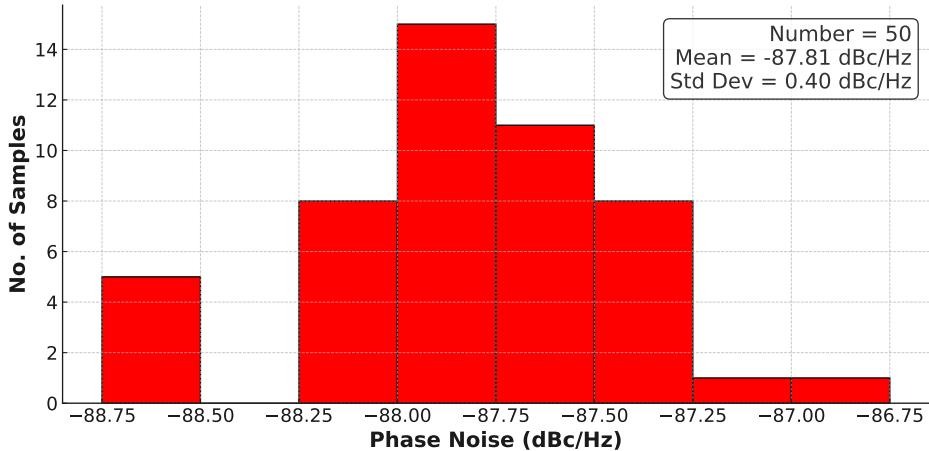


Figure 4.11: Statistical analysis of Phase Noise for $V = 1.05V$

Figure 4.12 exhibits the chip fabrication sensitivity for frequency for 100 Monte Carlo simulation runs. The distribution is somewhat bell-shaped. Std Dev is 23.36 MHz, this is a significant standard deviation relative to the mean. It indicates that the center frequency of the VCO is quite sensitive to process variations. A variation of ± 23.36 MHz around the mean of 322.76 MHz is substantial. while the average frequency is around 323 MHz, individual manufactured VCOs could operate anywhere from below 280 MHz to above 360 MHz for the same 1.05V control input.

4.2.9 Post Layout Analysis

Figure 4.13 illustrates the layout of the proposed design. For interconnecting purposes, Metal1, Metal2, Metal3, Metal5, and Polysilicon were used. The total area used is $16.64 \times 17.605 \mu m$ or $292.9472 \mu m^2$. From the post layout, the total number of extracted parasitic capacitance is 198 and total number of parasitic resistance is 333.

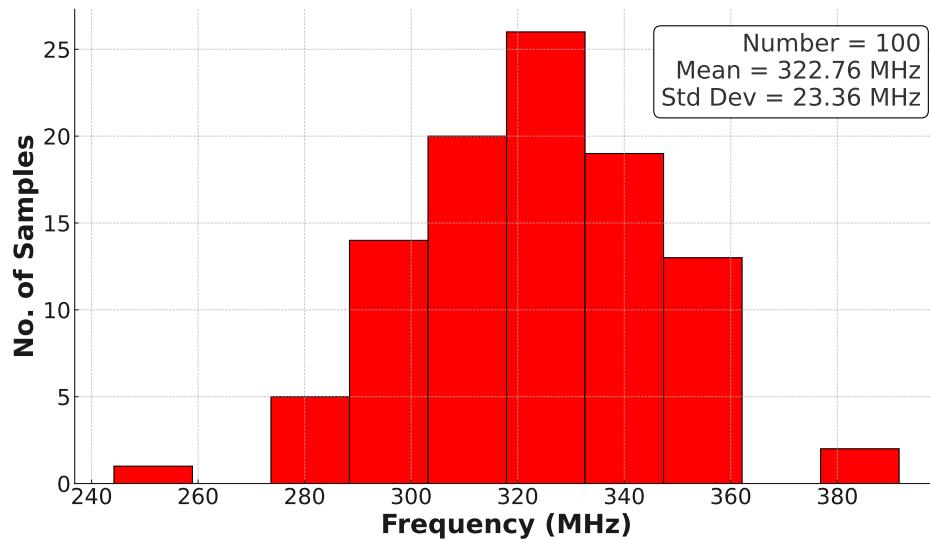


Figure 4.12: Statistical analysis of centre Frequency for $V = 1.05v$

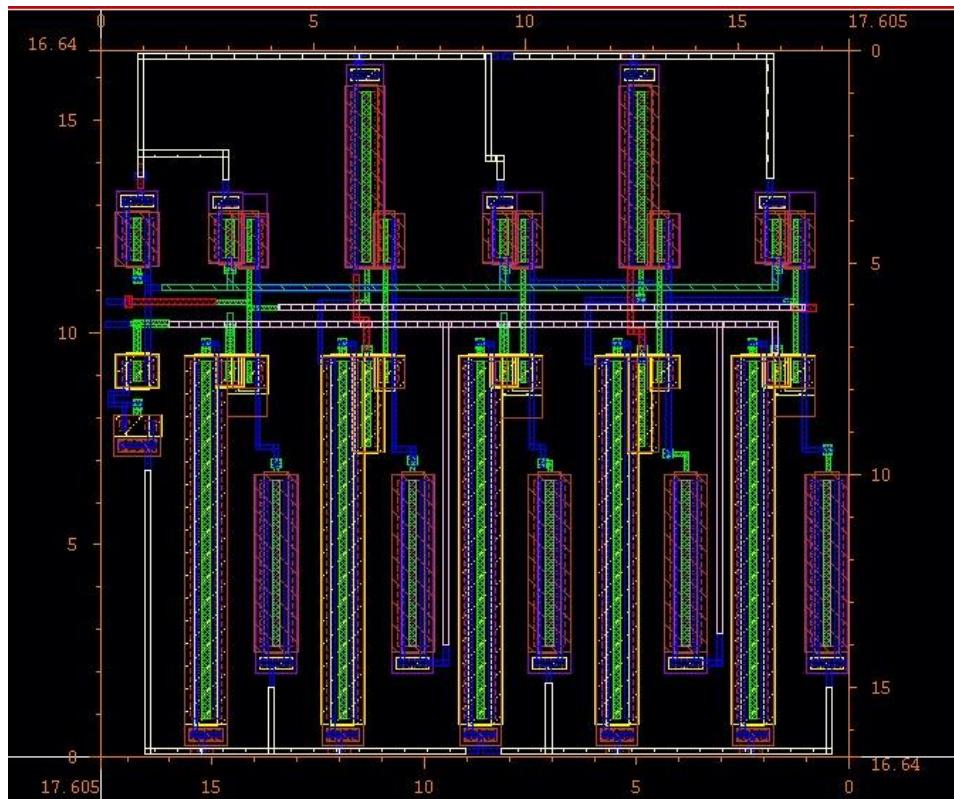


Figure 4.13: Layout of the proposed CS-VCO.

4.2.10 Comparison Table Analysis

The comparison table shows that the proposed circuit achieves a linear high tuning Bandwidth and low phase noise occupying small area.

Parameters	[38]	[39]	[40]	[17]	This Work
Technology	180nm	90nm	90nm	-	90nm
Supply Voltage (V)	1.8	0.6	0.2-0.6	-	1.8
Power Consumption (μ W)	260	771	87.6	-	354.6
Center Frequency (MHz)	404.5	-	-	-	323
Tuning Range (%)	92.45	94	94.81	-	93.86
Phase Noise (dB/Hz)	-82.28	-89	-89	-86.29	-88.63
FOM (dBc/Hz)	-140.27	-	-	-	-141.15

Table 4.1: Performance Comparison Table

4.3 ADC Performance Analysis

Having established the performance benchmarks for the core Voltage-Controlled Oscillator in the preceding analysis, this part broadens the scope to evaluate the complete 4-bit VCO-based Analog-to-Digital Converter system. The focus shifts to how the VCO's characteristics, in conjunction with the chosen Frequency-to-Digital Converter (FDC) architecture, translate into overall ADC performance. Key static parameters such as Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), along with dynamic metrics including Signal-to-Noise and Distortion Ratio (SNDR) and Effective Number of Bits (ENOB), are meticulously assessed.

Furthermore, the total power consumption of the ADC is quantified, providing a holistic view of the converter's efficiency and its potential for integration into power-sensitive applications.

4.3.1 Transient Response

This involves simulating the ADC with a defined time-varying input, typically a DC voltage, ramp or sinusoidal waveform, and observing the corresponding digital output codes over time. The primary utility of this investigation lies in the direct verification of the ADC's ability to correctly track the input signal and produce the expected sequence of output codes. This time-domain perspective offers a fundamental check on the converter's operational integrity and its capacity to translate continuous analog signals into a discrete digital stream. The transient response provides a crucial visual link between the analog input, the VCO's frequency modulation, and the final digital output generated by the Frequency-to-Digital Converter (FDC).

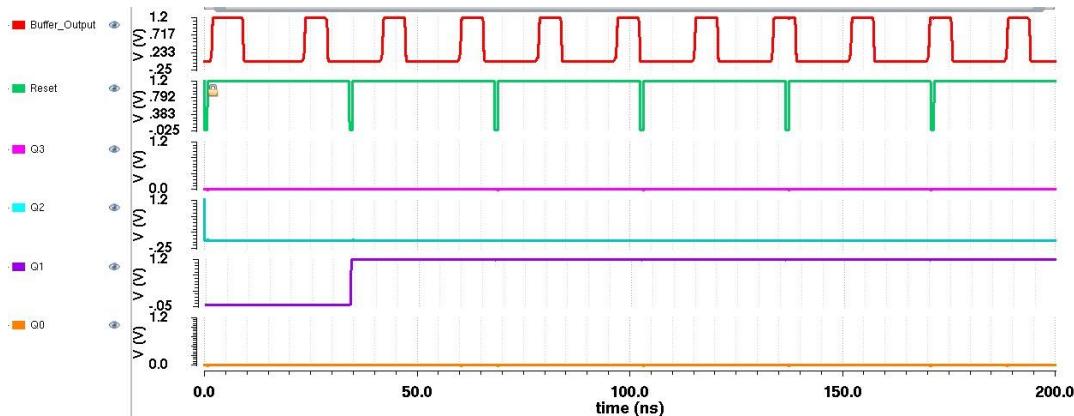


Figure 4.14: Transient Analysis for 0.55V (0010)

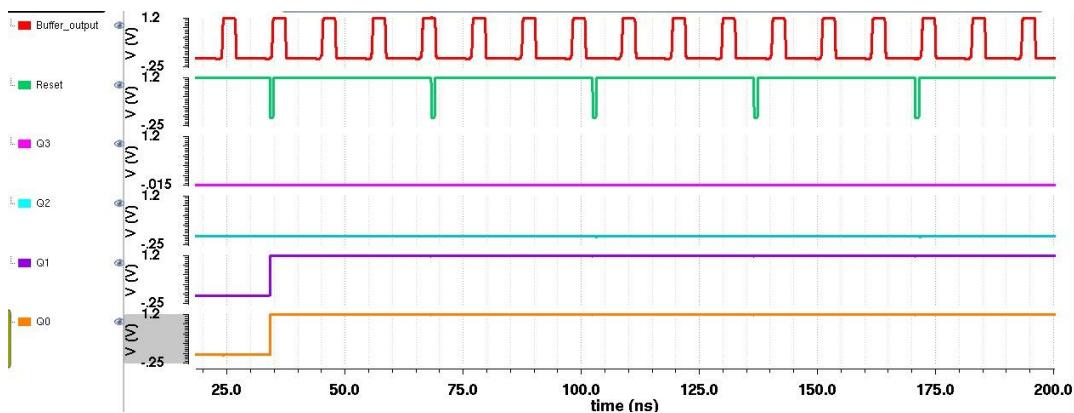


Figure 4.15: Transient Analysis for 0.62V(0011)

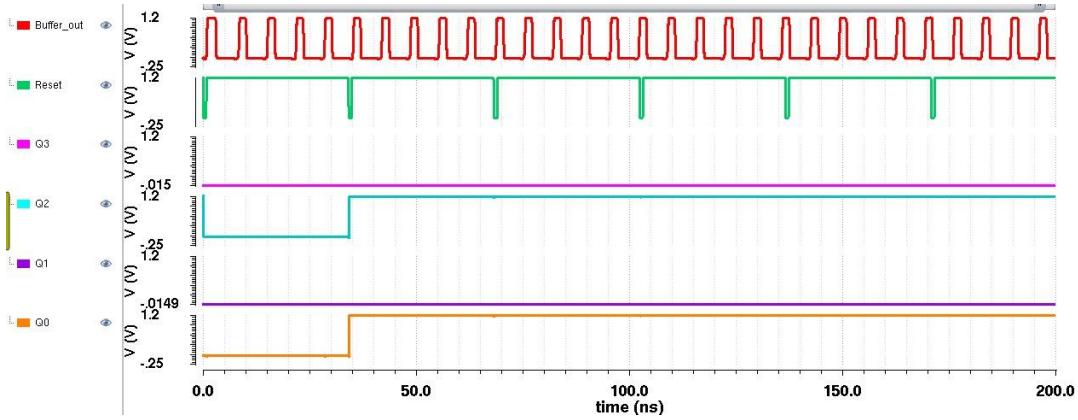


Figure 4.16: Transient Analysis for 0.72V(0101)

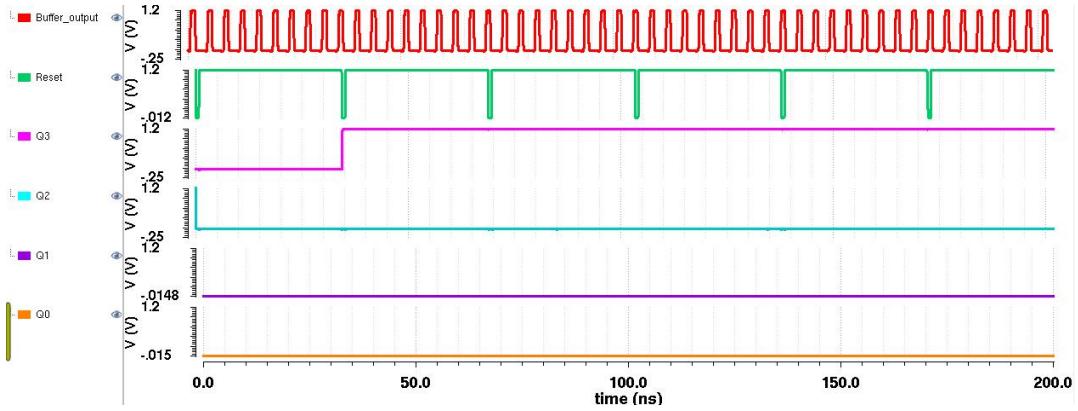


Figure 4.17: Transient Analysis for 0.9V(1000)

4.3.2 Static Performance

The static performance of an Analog-to-Digital Converter delineates its behavior under steady-state or quasi-DC input conditions. This analysis focuses on quantifying the deviations of the actual ADC transfer curve from its idealized counterpart. The principal metrics under investigation are Differential Non-Linearity (DNL), which assesses the uniformity of individual code bin widths, and Integral Non-Linearity (INL), which measures the cumulative deviation from a perfect straight-line transfer function. These parameters are typically ascertained by applying a precisely controlled ramp input. The results of this static characterization are vital for applications demanding high precision and monotonicity in the analog-to-digital conversion process.

This usually involves applying a very slowly varying, high-resolution analog ramp signal across the ADC's entire input voltage range. As the input sweeps, the digital output codes produced by the ADC are recorded along with the exact analog input voltage at which each code transition occurs. From this set of code transition voltages, the width of each individual digital code bin is determined.

4.3.2.1 Synchronous Counter Performance

The DNL plot shows significant variations across the 16 output codes (0 to 15) of the 4-bit ADC. The DNL values fluctuate both positively and negatively, indicating that the widths of the individual code bins are not uniform. A critical aspect revealed by DNL is monotonicity. An ADC is guaranteed to be monotonic if its DNL is always greater than -1 LSB (DNL \geq -1 LSB). In Figure 4.18, the most negative DNL is approximately -0.6 LSB. Since this value is greater than -1 LSB, the ADC is monotonic. It means the digital output will always increase or stay the same for an increasing analog input, it will not decrease, preventing missing codes. These considerable variations in code bin widths directly contribute to the overall linearity of the ADC and to ADC's effective resolution.

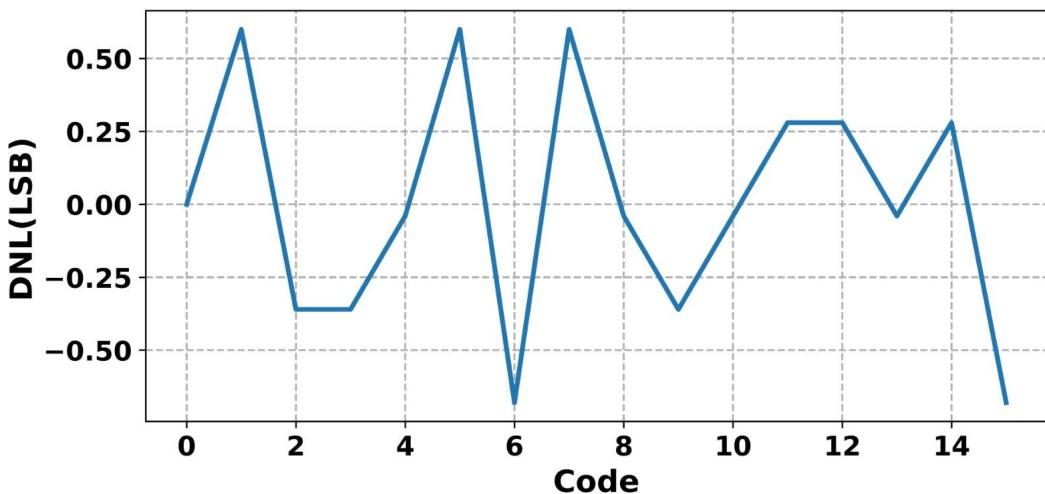


Figure 4.18: Differential Non Linearity (DNL) Plot.

The INL plot shown in Figure 4.19, which represents the cumulative sum of DNL errors, shows how much the actual ADC transfer function deviates from an ideal straight line. The

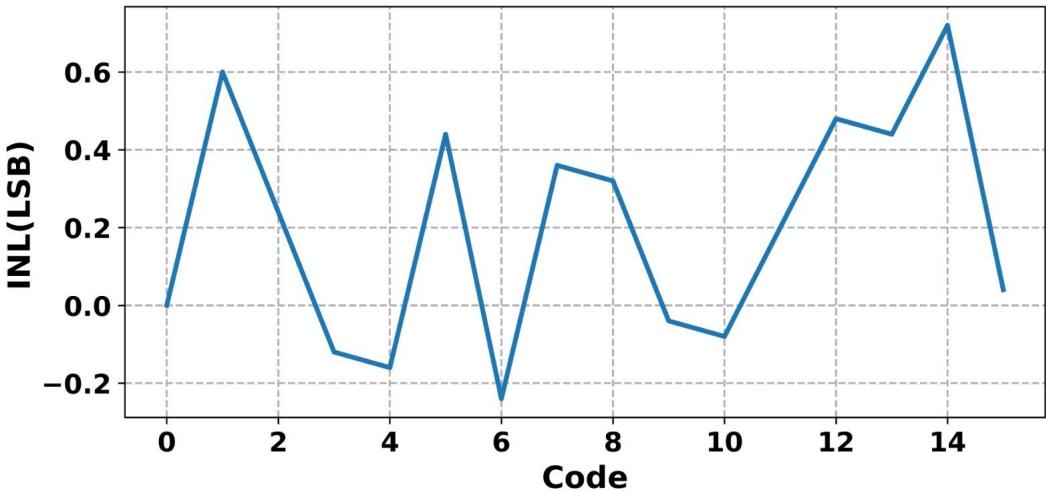


Figure 4.19: Integral Non Linearity (INL) Plot.

INL also exhibits significant variations across the codes. The INL values indicate the absolute error in the digital output representation relative to an ideal ADC. An INL of +0.7 LSB means that at code 14, the analog voltage corresponding to this code transition is 0.7 LSB higher than it would be for a perfectly linear ADC. For a 4-bit ADC, an ideal device would have INL and DNL values very close to 0 LSB (Practically within ± 1 LSB). The observed peak INL of +0.7 LSB and DNL of ± 0.6 LSB suggest that the ADC's linearity is achieved and suitable enough for the application mentioned.

4.3.2.2 Asynchronous Counter Performance

The performance analysis of this 4-bit VCO-based ADC, utilizing an asynchronous counter, reveals little linearity imperfections. The Differential Non-Linearity (DNL) plot exhibits excursions between approximately -0.75 LSB and +0.6 LSB, signifying considerable variation in quantization step widths likely stemming from propagation delay accumulation and ripple effects inherent in asynchronous counter designs. While monotonicity is maintained as DNL remains above -1 LSB, these variations, particularly prominent around codes 2, 11, and 13, contribute directly to the Integral Non-Linearity (INL). The INL plot, reflecting the cumulative sum of these differential errors, reaches a peak of around +0.75 LSB, indicating a discernible deviation from an ideal linear transfer function across the ADC's operational

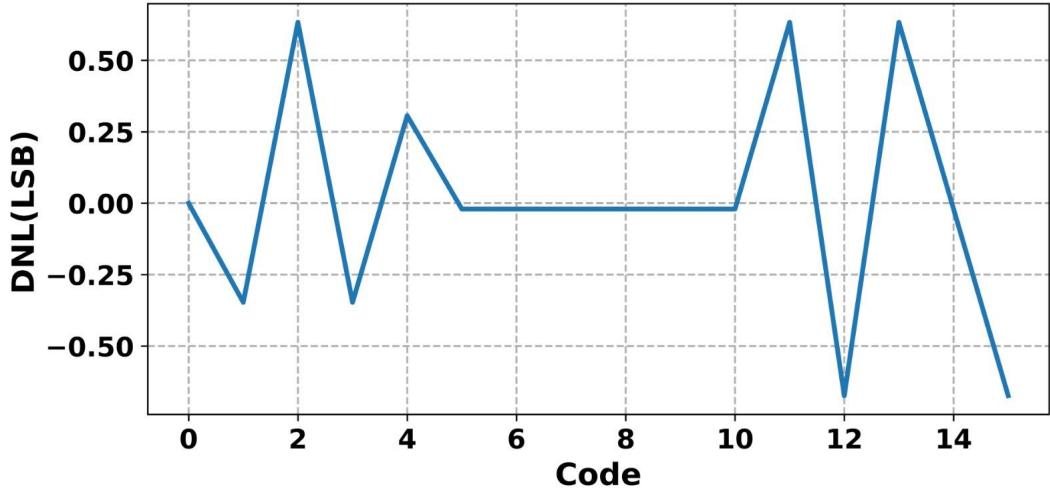


Figure 4.20: Differential Non Linearity (DNL) Plot.

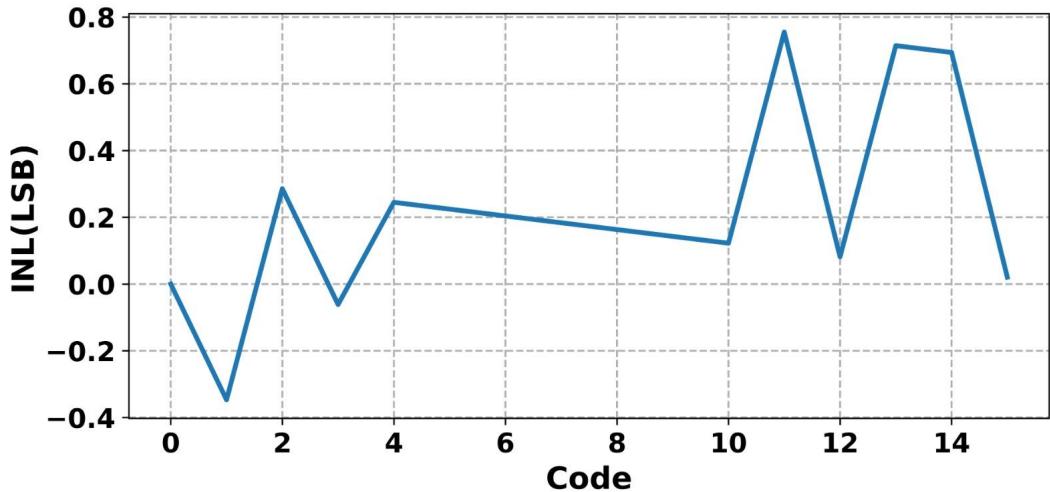


Figure 4.21: Integralal Non Linearity (INL) Plot.

range, particularly pronounced at higher code values where timing skews tend to compound more significantly.

4.3.3 Dynamic Response

While static characteristics define an Analog-to-Digital Converter's (ADC) precision with DC inputs, its dynamic performance is paramount when processing real-world, time-varying signals. This section delves into the comprehensive evaluation of the ADC's behavior under such dynamic conditions. By applying a spectrally pure sinusoidal input and analyzing the resultant

digital output stream in the frequency domain, typically via a Fast Fourier Transform (FFT), critical figures of merit are extracted. These include the Signal-to-Noise and Distortion Ratio (SNDR), Spurious-Free Dynamic Range (SFDR), Total Harmonic Distortion (THD), and the derived Effective Number of Bits (ENOB). These dynamic metrics collectively quantify the ADC's ability to accurately convert AC signals while accounting for noise, harmonic distortion, and other spurious components, thereby providing a holistic measure of its fidelity in practical applications.

The dynamic capabilities were assessed by stimulating the ADC with a sinusoidal input of known frequency and amplitude. The core of this dynamic characterization hinged on spectral analysis, achieved by performing a Fast Fourier Transform (FFT) on the coherently sampled, digitized output sequence. This transformation converts the time-domain representation of the ADC's output into its frequency-domain equivalent, allowing for the distinct identification and quantification of the desired signal component versus unwanted noise and distortion products. Prior to the FFT, a windowing function was typically applied to the dataset to mitigate end-effect errors. The resulting power spectrum then served as the basis for extracting crucial dynamic metrics including SNDR, SFDR, THD, and consequently, the ENOB.

4.3.3.1 Synchronous Counter Performance

Figure 4.22 reveals Signal-to-Noise and Distortion Ratio (SNDR) from approximately 23.25 dB (3.57 ENOB) at 600 kHz input frequency to 22.05 dB (3.37 ENOB) at 800 kHz. For target input signals in the 1-10 kHz range, this ADC would operate with a very high Oversampling Ratio (OSR) of approximately. Such a high OSR will leverage the VCO's inherent first-order noise shaping characteristics and spread quantization and thermal noise power over a much wider band, allowing significant in-band SNDR improvement after digital filtering. Concurrently, the reduced dynamic demands on the VCO at these lower input frequencies will minimize distortion. Therefore, by observing the consideration and substantial benefits of oversampling, SNDR and overall performance when this ADC is utilized for such signal

application mentioned earlier.

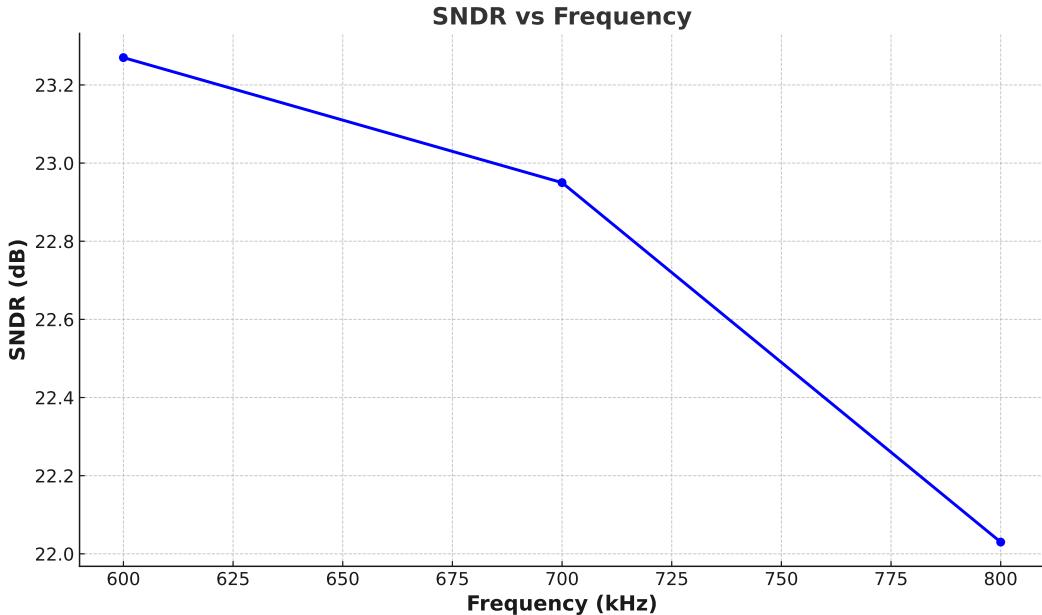


Figure 4.22: Signal to Noise Distortion Ratio (SNDR) at Different Frequency.

The SFDR plot shown in Figure 4.23 demonstrates the SFDR from 27.7 dBc at 600 kHz to 25.8 dBc at 700 kHz, and further drops to 24.3 dBc at 800 kHz. This trend suggests that higher input frequencies exacerbate stronger spurious harmonic components. Any generated harmonics will be well-separated in frequency from the low-frequency signal of interest and the dominant quantization noise, making them easier to attenuate with subsequent digital filtering.

From Figure 4.24 to Figure 4.26 discusses about the strength of input signal power and the worst spur level that measured the highest power level of unwanted spikes (called spurs) in the spectrum. The comparison is shown for different frequencies such as 600KHz, 700Khz and 800KHz. The purple arrow points to "SFDR" which measures the difference between the power of the fundamental frequency (0 dB) and the worst spur. This SFDR dB tells you how much stronger the main signal is compared to the strongest unwanted signal, a key indicator of the ADC's ability to handle distortion. For 600KHz the signal strength also close to worst spur level after getting drop and for 800KHz this signal strength is at more below

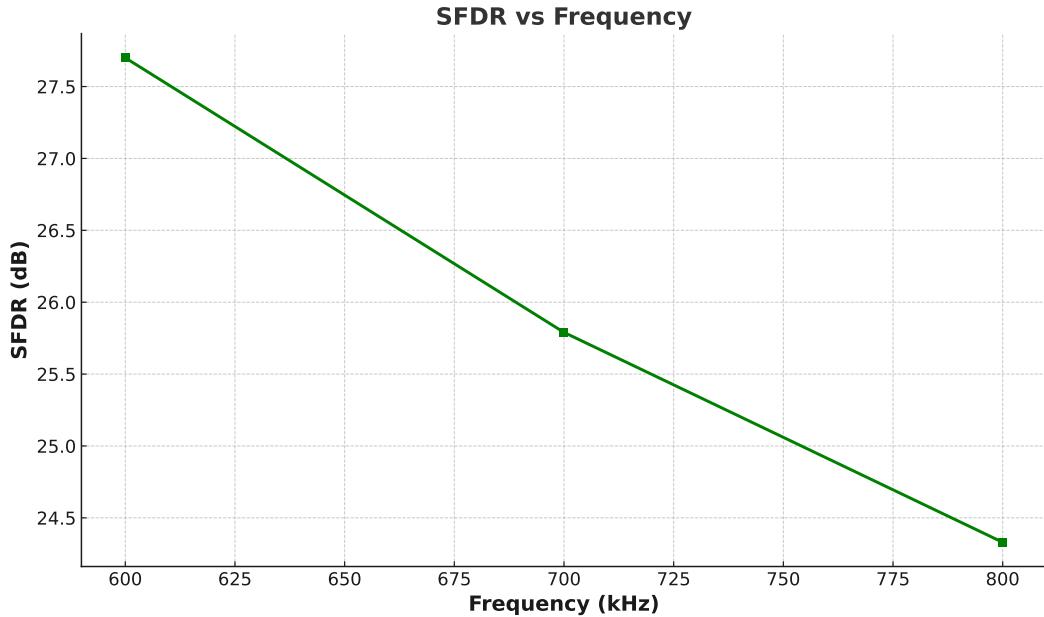


Figure 4.23: Spurious Free Dynamic Range (SFDR) at Different Frequency.

than the worst spur level which happens because of the higher harmonic noise. It Shows a well observation on the performance on ADC against the noise signal to enhance regarding the choice of application.

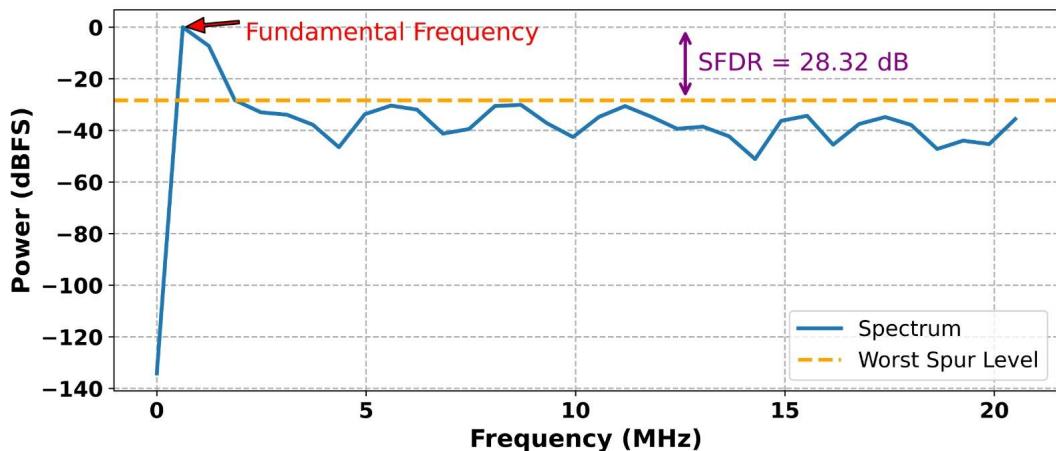


Figure 4.24: Dynamic Test Simulation Result (600KHz).

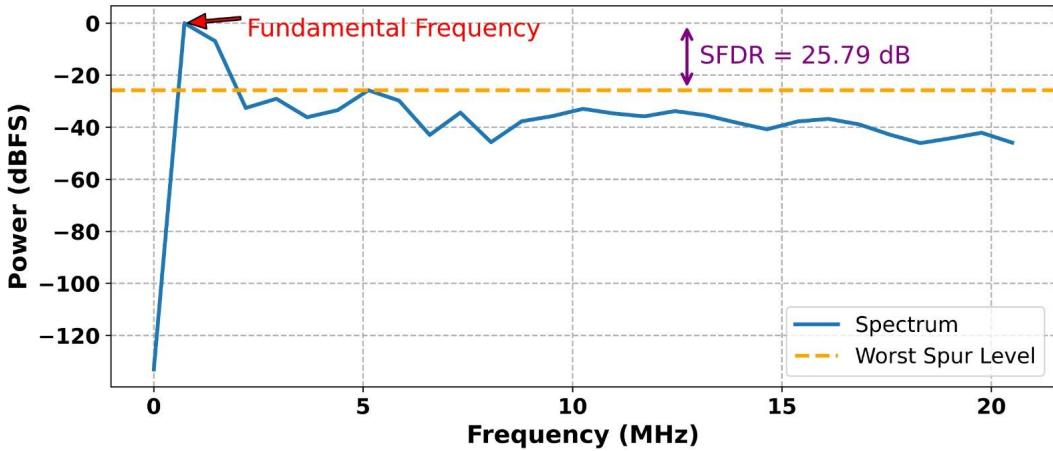


Figure 4.25: Dynamic Test Simulation Result (700KHz).

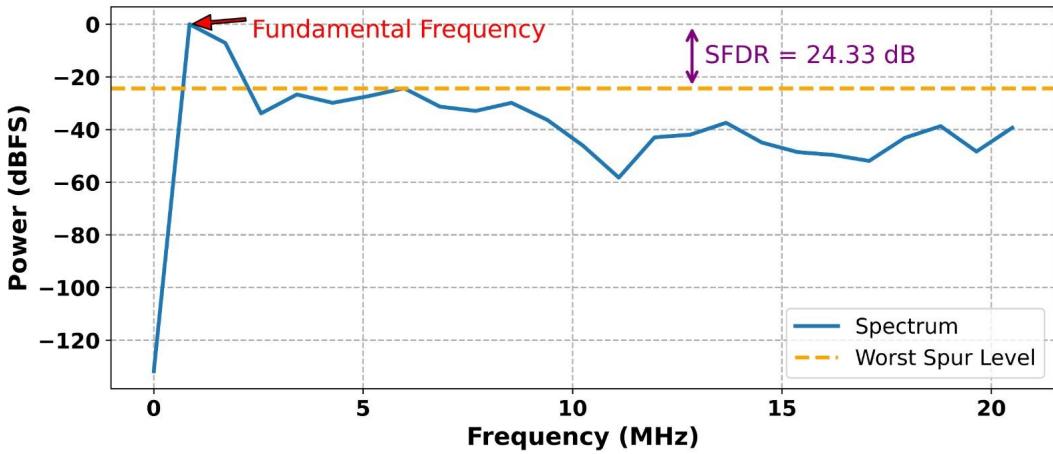


Figure 4.26: Dynamic Test Simulation Result (800KHz)

4.3.3.2 Asynchronous Counter Performance

The Figure 4.27 and Figure 4.28 illustrate the Signal-to-Noise-and-Distortion Ratio (SNDR) and Spurious-Free Dynamic Range (SFDR) performance of a 4-bit Voltage-Controlled Oscillator (VCO)-based ADC with an asynchronous counter across different frequencies, ranging from 600 kHz to 800 kHz. The SNDR graph shows a decline from 22.5 dB at 600 kHz to approximately 20 dB at 800 kHz, indicating a degradation in signal quality and linearity as frequency increases, which is typical due to increased noise and distortion at higher operating frequencies. The SFDR graph similarly decreases from 23.9 dB at 600 kHz to around 23.6 dB at 800 kHz, reflecting a reduction in the strength of the fundamental signal relative to the

largest spurious tone, suggesting potential limitations in harmonic distortion management at higher frequencies. For our target application frequency below 10 kHz, these results suggest that the ADC's performance would likely be significantly better, as the observed degradation occurs at much higher frequencies.

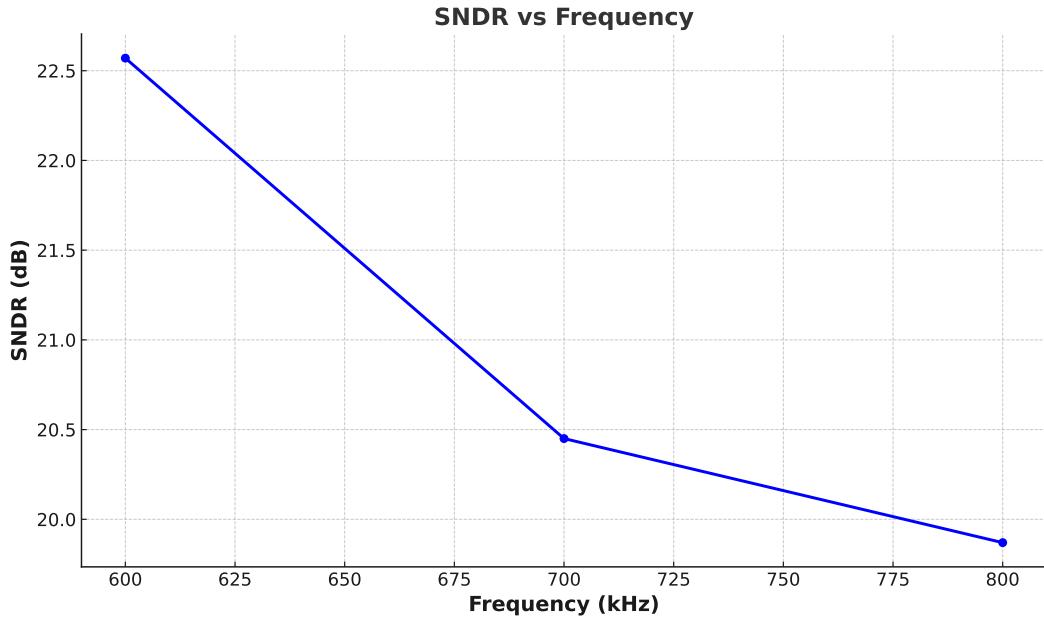


Figure 4.27: Signal to Noise Distortion Ratio (SNDR) at Different Frequency.

The 4-bit VCO-based ADC with an asynchronous counter, as depicted in the vibrant power spectrum graphs (Figure 4.29, Figure 4.30, Figure 4.31) for input frequencies of 600 kHz, 700 kHz, and 800 kHz, showcases an Spurious-Free Dynamic Range (SFDR) of 23.90 dB, 23.74 dB, and 23.60 dB respectively. the fundamental frequency, elegantly rising near 0 MHz, peaks at a crisp 0 dBFS, while the worst spur level lingers around a steady -20 dBFS. It is pointing to promising avenues for enhancement such as refining the VCO's linearity or bolstering the counter's accuracy. Is showing a stable strength against the higher harmonic frequency noise.

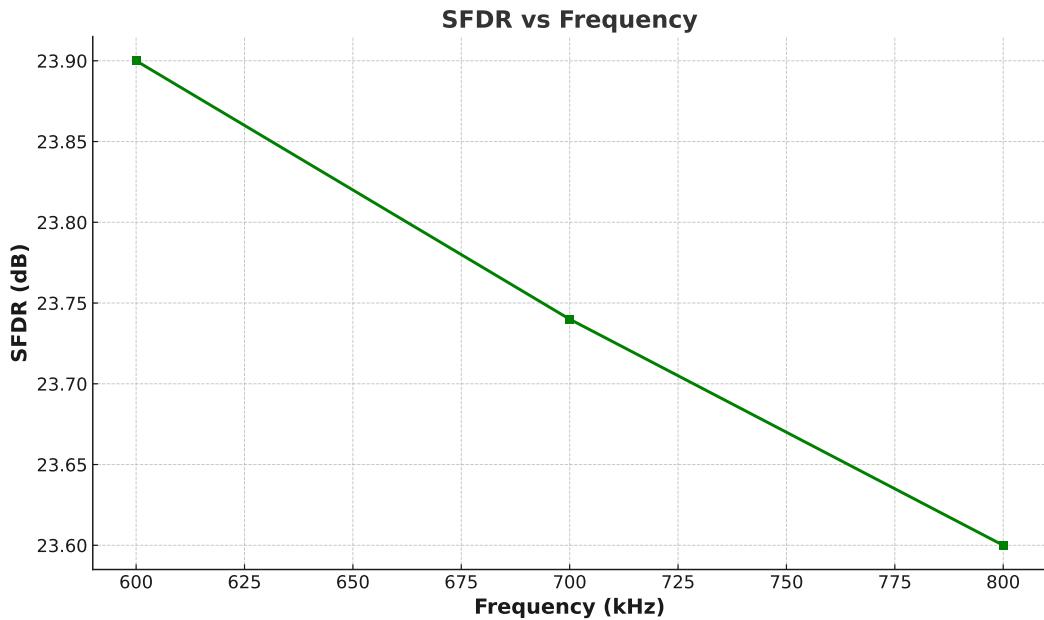


Figure 4.28: Spurious Free Dynamic Range (SFDR) at Different Frequency.

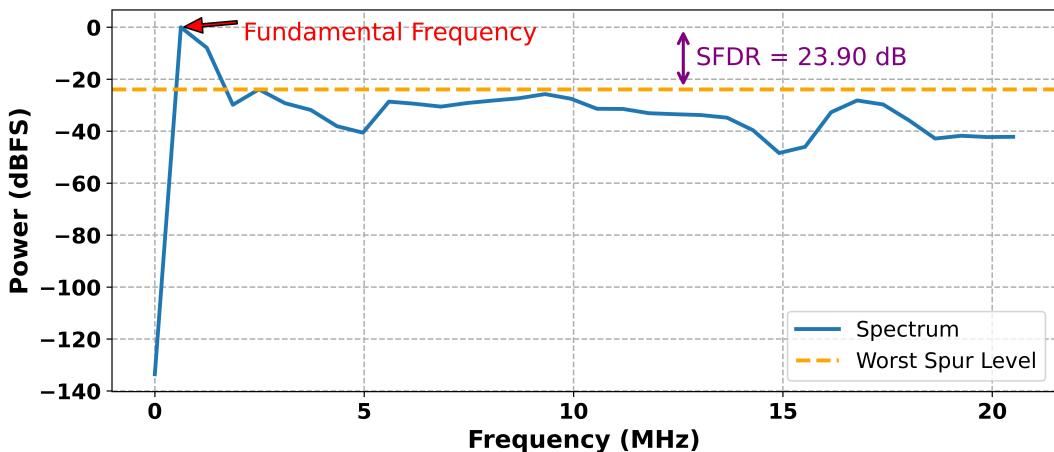


Figure 4.29: Dynamic Test Simulation Result (600KHz).

4.3.4 Reconstructed ADC Output

Figure 4.32 and Figure 4.33 consistently portrays the output of a 4-bit Analog-to-Digital Converter for sine input for three different frequencies stair-step quantization of an input sinusoidal voltage. This 4-bit resolution inherently limits the signal representation to 16 discrete amplitude levels, causing the smooth analog wave to be approximated as a series of stepped transitions, oscillating roughly between 0.5V and 1.6V. Variations across the plots, specific-

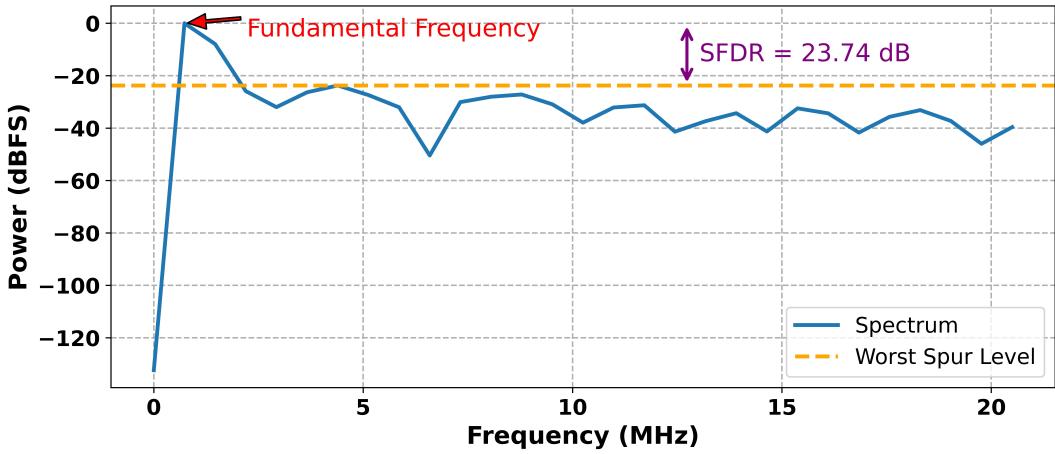


Figure 4.30: Dynamic Test Simulation Result (700KHz).

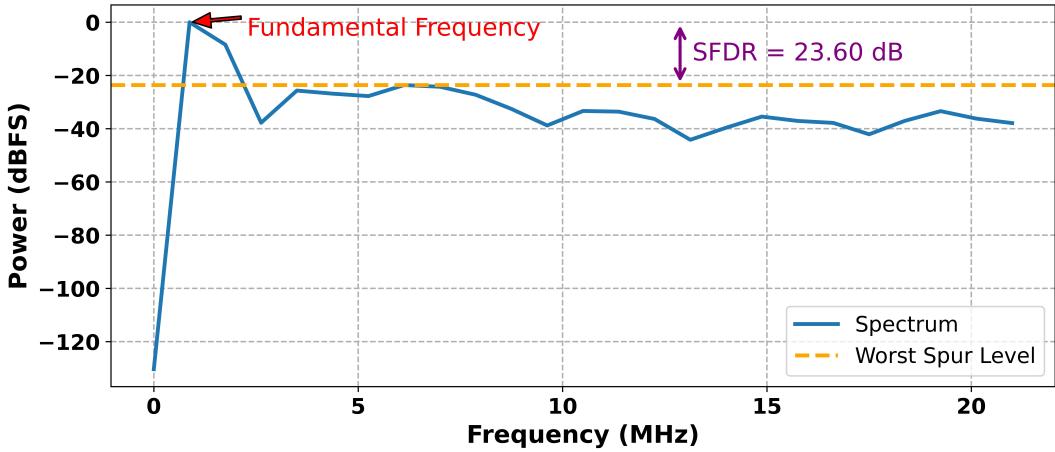


Figure 4.31: Dynamic Test Simulation Result (800KHz)

cally in the horizontal compression or expansion of the sine wave, effectively demonstrate the ADC's response to differing input signal frequencies relative to its sampling rate. Lower frequencies yield more temporally detailed waveforms with more samples per cycle, while higher frequencies result in more compressed representations. Notably, despite this coarse quantization, the fundamental sinusoidal character of the signal is well-preserved in all instances, with the steps appearing generally clean and free from obvious, large-scale erratic deviations.

When comparing the potential performance of ADCs based on synchronous versus asynchronous counters in generating such outputs, the primary differentiator lies in their internal

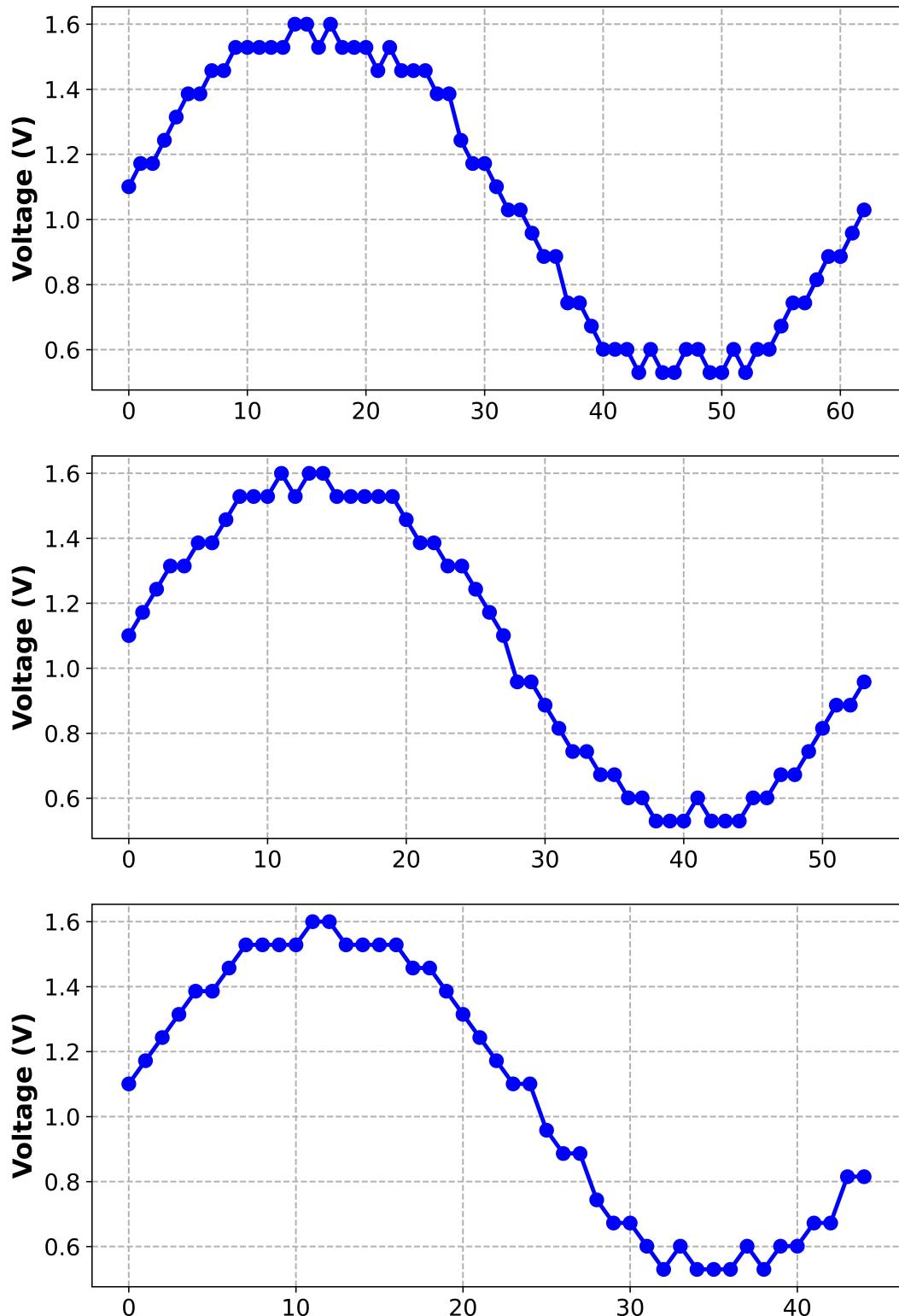


Figure 4.32: Reconstructed Graph For input Frequency 600KHz, 700KHz, 800KHz (Asynchronous)

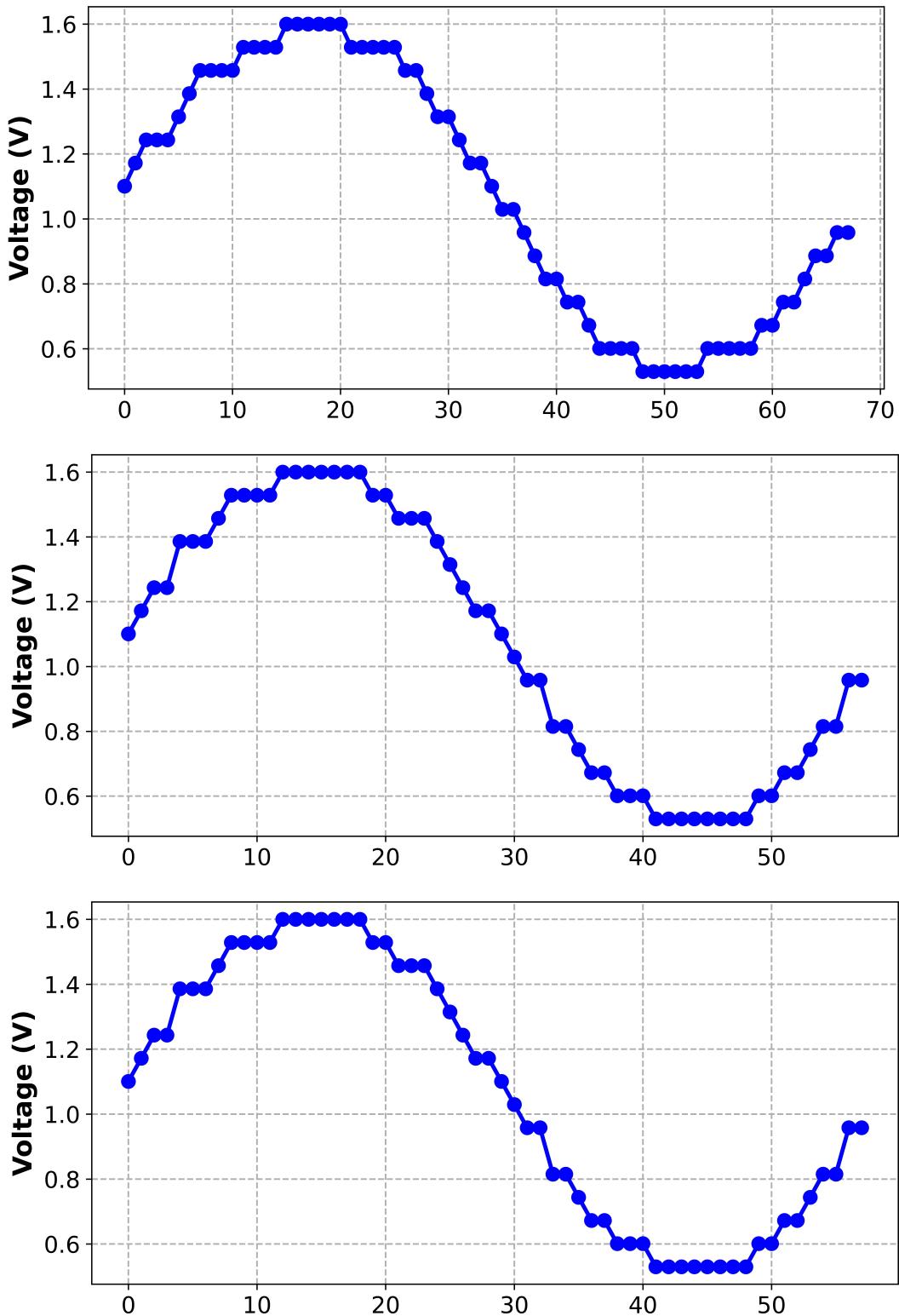


Figure 4.33: Reconstructed Graph For input Frequency 600KHz, 700KHz, 800KHz (Synchronous)

signal integrity. Synchronous counter ADCs, where all counter bits transition in unison with the clock, produce an inherently cleaner, glitch-free internal reference ramp for the conversion process, which would translate to very regular and predictable quantization steps in the final output, aligning well with the consistent appearance of the provided graphs. Conversely, asynchronous counter ADCs, with their sequential bit changes, are susceptible to generating transient glitches on their internal DAC output during counter transitions. If significant, these glitches could corrupt the conversion, manifesting in the final plots as occasional rogue data points, less perfectly flat quantization steps, or "noisier" transitions. The absence of such prominent artifacts in these visuals suggests that the depicted performance leans towards the cleaner operation characteristic of a synchronous counter design, or implies a very well-implemented asynchronous system where glitch effects are either minimal or effectively mitigated, thus not visibly degrading the 4-bit quantized output.

4.3.5 Layout Implementation and Area Considerations

The physical realization of the 4-bit VCO-based ADC, including its core components, was undertaken using the 90nm CMOS process in Cadence Virtuoso. This phase involved translating the schematic designs of the VCO, the Frequency-to-Digital Converter (FDC) – with both asynchronous and synchronous counter options – and the output register into physical layouts. The layouts for the asynchronous counter, the complete ADC with this counter, the synchronous counter, and its corresponding complete ADC are depicted in Figures 4.34, 4.35, 4.36, and 4.37 respectively. Standard design practices were followed to ensure a functional and robust physical implementation.

A key aspect of the physical design is the silicon area occupied by the different configurations, as summarized in Table 4.2.

The data clearly shows that the synchronous counter, due to its inherent circuit complexity involving additional logic for parallel clocking (as discussed in Chapter 3), occupies a larger area ($995.41 \mu\text{m}^2$) compared to the simpler asynchronous counter ($696.55 \mu\text{m}^2$). This dif-

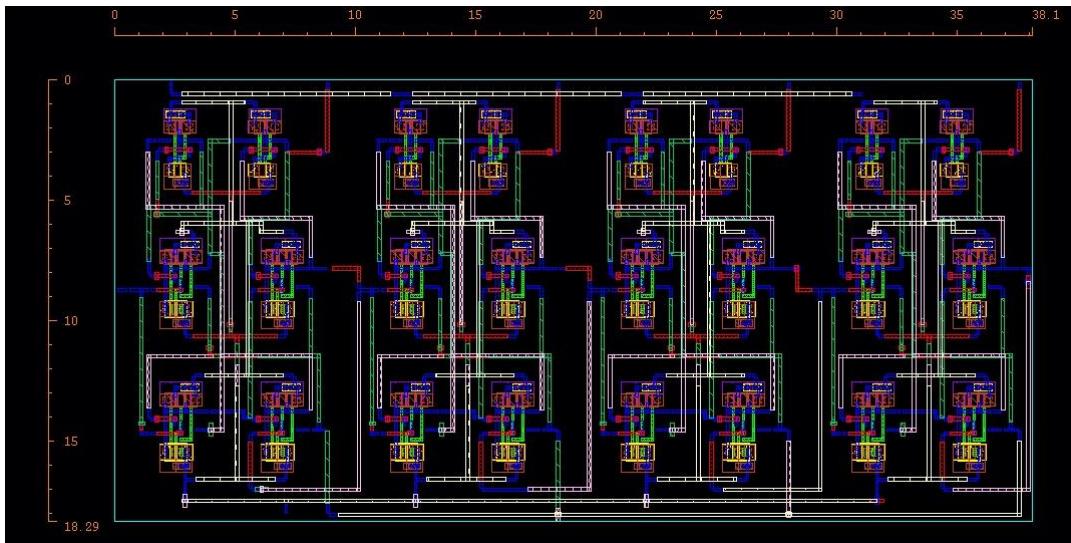


Figure 4.34: Layout of the 4-bit Asynchronous (Ripple) Counter.

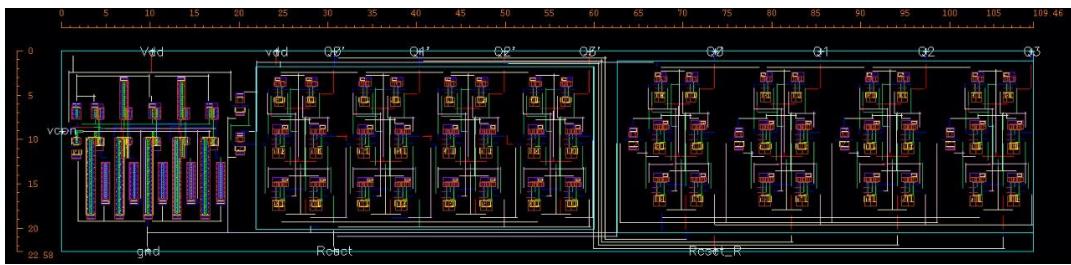


Figure 4.35: Layout of the complete 4-bit VCO-based ADC with Asynchronous Counter.

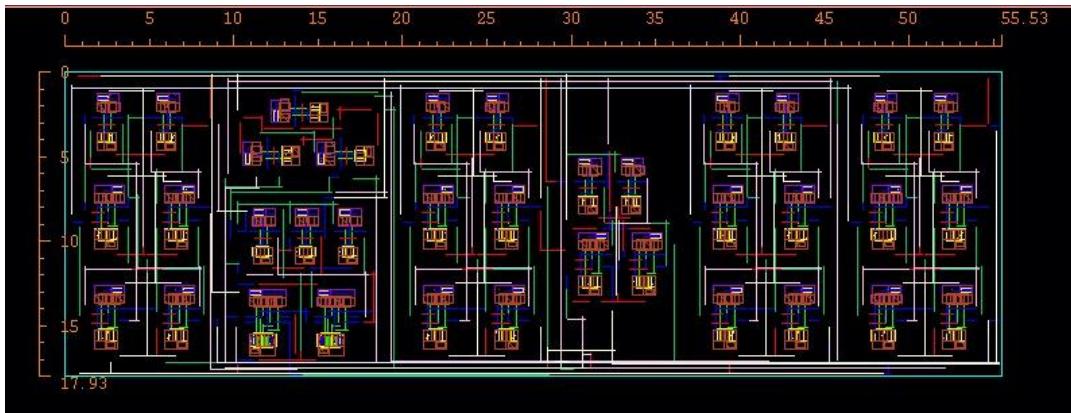


Figure 4.36: Layout of the 4-bit Synchronous Counter.

ference in area for the FDC core contributes to the overall size of the complete ADC. The ADC incorporating the synchronous FDC is consequently larger ($2874.93 \mu\text{m}^2$) than its asynchronous counterpart ($2473.74 \mu\text{m}^2$). This area trade-off is a significant consideration, particularly for compact biomedical device integration, where minimizing silicon footprint is often

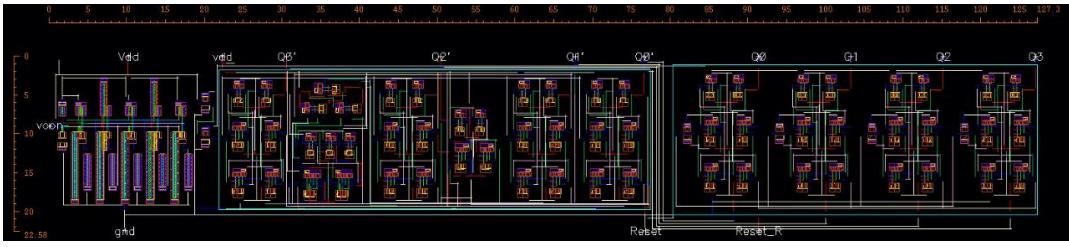


Figure 4.37: Layout of the complete 4-bit VCO-based ADC with Synchronous Counter.

Table 4.2: Layout Area of FDC and ADC Implementations.

Layout Component	Width (μm)	Height (μm)	Area (μm^2)
VCO	16.64	17.605	292.95
Asynchronous Counter	38.1	18.29	696.55
Synchronous Counter	55.53	17.93	995.41
Complete ADC (Async)	109.46	22.58	2473.74
Complete ADC (Sync)	127.3	22.58	2874.93

a priority. The physical design focused on efficient placement and routing to manage signal integrity and component density.

4.3.6 Performance Comparison Table

	[41]	[42]	[43]	[44]	[45]	[46]	[47]	[48]	This Work
Technology (nm)	130	90	180	28	32	180	350	90	90
Resolution (Bits)	6	6	4	6	4	Adaptive	Adaptive	6	4
VSupply (V)	1.5	1.2	1.8	0.95	1.2	0.5	2.4	1.2	1.8
Sampling (Hz)	10M	1G	1.8G	2.4G	-	1K	1K	3G	41M
ENOB (Bits)	6.01	5.4	3.7	5.48	-	5.6	4-8	5.3	3.64
INL (LSB)	-	0.74	0.3		0.34	-	-	0.2	-0.04 ~ 0.72
DNL (LSB)	-	0.49	0.29		-	0.5	-	0.2	-0.04 ~ -0.68
Power (W)	1.12m	18.7m	15.5m	23m	24m	0.22u	2u	90m	$328.3 \mu\text{W}$
FoM (pJ/Conv.step)	2.15	0.44	0.695	0.215	-	1.24	0.15	7.8	0.642
Area (mm^2)	0.007	0.38	0.3	0.03	-	0.03	0.037	0.28	0.00287

Table 4.3: Comparison of ADC designs.

4.4 Chapter Summary

This chapter presented a comprehensive evaluation of the simulation results and performance characteristics of the proposed Voltage-Controlled Oscillator (VCO) and the complete 4-bit VCO-based Analog-to-Digital Converter (ADC) system. All simulations were conducted using Cadence Virtuoso in the gpdk 90nm CMOS process technology.

The performance of the novel five-stage current-starved VCO was thoroughly investigated. Transient analysis confirmed stable oscillation, while Periodic Steady State (PSS) analysis demonstrated a wide post-layout tuning range from 38 MHz to 619 MHz, closely aligning with the schematic-level results (39 MHz to 697 MHz), with the slight reduction attributed to parasitic effects. Phase noise analysis revealed a post-layout performance of approximately -87.66 dBc/Hz at a 1 MHz offset (for a 1.6V control voltage), and the integration of the charge pump yielded an improvement of about 2.14 dB compared to a conventional design under worst-case conditions. The VCO achieved a Figure of Merit (FOM) of -141.15 dBc/Hz. Robustness was confirmed through process corner and temperature sweep simulations, which showed consistent tuning range maintenance and remarkable stability in phase noise profiles despite variations in absolute frequency. DC power consumption analysis indicated predictable behavior across different temperatures and control voltages. Statistical Monte Carlo simulations provided insights into the design's sensitivity to process variations, quantifying the expected distribution for power consumption, phase noise, and center frequency, and highlighting a compact layout area of 292.9472 μm^2 .

Subsequently, the chapter detailed the performance of the complete 4-bit VCO-based ADC, systematically evaluating implementations with both synchronous and asynchronous Frequency-to-Digital Converter (FDC) architectures. Transient response simulations verified the correct tracking of input signals and generation of corresponding digital output codes. Static performance, characterized by Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), was assessed for both counter types. The synchronous counter based ADC exhibited DNL within approximately ± 0.6 LSB and a peak INL of +0.7 LSB, ensuring monotonicity. The asynchronous counter version showed DNL between approximately -0.75 LSB and +0.6 LSB, and a peak INL around +0.75 LSB, also maintaining monotonicity but with more pronounced variations attributed to ripple effects. Dynamic performance metrics, including Signal-to-Noise and Distortion Ratio (SNDR) and Spurious-Free Dynamic Range (SFDR), were evaluated at various input frequencies (600 kHz, 700 kHz, 800 kHz). The syn-

chronous counter based ADC demonstrated an SNDR ranging from 23.25 dB (3.57 ENOB) to 22.05 dB (3.37 ENOB), and SFDR from 27.7 dBc to 24.3 dBc. The asynchronous counter based ADC yielded an SNDR from 22.5 dB to approximately 20 dB, and SFDR from 23.9 dBc to 23.6 dBc over the same input frequency range. These results provided a clear comparison of the trade-offs between the two FDC approaches in the context of the proposed wideband VCO.

The extensive simulation results, encompassing both schematic and post-layout analyses along with variability assessments, collectively validate the functionality and robustness of the proposed 4-bit VCO-based ADC design, establishing its potential for integration into power-sensitive biomedical applications. The chapter concluded with a comparative table summarizing the ADC's performance against existing works, highlighting its competitive characteristics.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

This thesis has focused on the design, implementation, and comprehensive evaluation of a 4-bit Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converter (ADC) tailored for low-power biomedical applications. The research addressed inherent challenges in conventional VCO-based ADC architectures, particularly concerning VCO linearity, phase noise, and the impact of Frequency-to-Digital Converter (FDC) design choices on overall system performance.

5.1 Conclusions

The primary objective of this research was to develop a compact, power-efficient ADC architecture that improves upon existing designs by incorporating novel circuit-level techniques. The findings and contributions are summarized below.

5.1.1 Research outcomes

The research presented in this thesis yielded several significant outcomes in the domain of VCO-based ADC design for low-power biomedical applications.

A primary outcome was the successful design, simulation, and post-layout verification of a novel five-stage current-starved ring Voltage-Controlled Oscillator (VCO). This VCO architecture distinctively incorporated diode-connected NMOS source degeneration to enhance the voltage-to-frequency (V-F) linearity and an embedded charge pump mechanism within alternating delay stages, which demonstrably reduced phase noise. Implemented and characterized in a 90nm CMOS technology, the VCO exhibited a wide post-layout tuning range, operating from 38 MHz to 619 MHz. Post-layout simulations indicated a commendable phase noise performance of approximately -87.66 dBc/Hz at a 1 MHz offset (for a 1.6V control voltage). The inclusion of the charge pump contributed to a phase noise improvement of approximately

2.14 dB when compared to a conventional counterpart under worst-case operational scenarios. Furthermore, the VCO achieved a notable Figure of Merit (FOM) of -141.15 dBc/Hz, while occupying a compact total layout area of 292.9472 μm^2 , underscoring its suitability for area-constrained applications.

Another key outcome involved the detailed design and comparative investigation of two distinct 4-bit Frequency-to-Digital Converter (FDC) architectures: an asynchronous (ripple) counter and a synchronous binary counter. Both counter types, along with a 4-bit D-Flip-Flop based output register, were implemented to effectively quantize the VCO's frequency output. This comparative approach facilitated an empirical assessment of the trade-offs associated with each counter topology, particularly in terms of operational speed, potential for glitching, and circuit complexity when integrated with the wideband VCO.

The integration of the proposed VCO with these FDC architectures resulted in a comprehensive 4-bit ADC system. Rigorous simulations, encompassing transient analysis, DC power consumption, process corner variations, temperature sweeping, and Monte Carlo analysis, confirmed the robustness of the proposed VCO design and provided a foundational understanding of the complete ADC architecture's performance characteristics under diverse operating conditions. The static performance, evaluated through DNL and INL metrics, indicated monotonicity for both counter types, with the synchronous counter generally exhibiting slightly more uniform code bin widths. Dynamic performance assessments (SNDR, SFDR, ENOB) across various input frequencies highlighted the capabilities and limitations of each FDC implementation, providing critical data for application-specific design choices. For instance, the synchronous counter based ADC demonstrated an SNDR from approximately 23.25 dB (3.57 ENOB) at 600 kHz down to 22.05 dB (3.37 ENOB) at 800 kHz, while the asynchronous counter version showed an SNDR from 22.5 dB down to approximately 20 dB over the same frequency range.

Collectively, these outcomes provide a well-characterized, power-efficient 4-bit VCO-based

ADC design with tangible improvements at the circuit level, and a practical evaluation of FDC design choices critical for optimizing performance in targeted biomedical applications.

5.1.2 Research significance

The significance of this work lies in its contribution towards advancing compact and power-efficient ADC solutions, which are critical for the rapidly expanding field of biomedical devices. By systematically addressing V-F non-linearity and phase noise at the circuit level within the VCO, this research offers practical techniques to enhance the performance of VCO-based ADCs. The demonstrated improvements in linearity and phase noise, achieved through source degeneration and integrated charge pumps respectively, are particularly relevant for applications requiring accurate signal conversion with minimal power and area overhead.

Furthermore, the detailed investigation into asynchronous versus synchronous FDC implementations provides valuable insights for designers. This study highlights the performance implications of counter architecture choices, especially when interfacing with a wideband VCO, enabling more informed design decisions based on specific application priorities such as maximum operating speed, power constraints, or silicon footprint. The comprehensive simulation results, including post-layout and variability analyses, underscore the potential of the proposed 4-bit VCO-based ADC architecture as a viable candidate for integration into modern, power-constrained biomedical systems like Photoplethysmography (PPG) sensors and Brain-Machine Interfaces (BMIs), where efficiency and compactness are paramount.

5.2 Future Works

While this thesis has achieved its primary objectives, the research opens several avenues for future investigation and enhancement. The following points outline potential directions for extending this work:

- **Higher Resolution and Dynamic Range:** Future efforts could focus on extending the ADC resolution beyond 4 bits. This might involve exploring more sophisticated VCO linearization techniques to maintain performance over a wider input range, or investigating advanced FDC architectures. For instance, incorporating noise-shaping techniques, such as a delta-sigma modulator with a VCO-based quantizer, could significantly improve the dynamic range and effective number of bits (ENOB).
- **Advanced FDC Architectures and Jitter Reduction:** The comparative study of FDC counters could be expanded. Investigating architectures like Gray-code counters for reduced switching noise or pipelined/interleaved FDCs for higher throughput could be beneficial. Furthermore, research into techniques for mitigating the impact of clock jitter on the sampling window (T_s) and its effect on the FDC's accuracy could improve overall ADC performance.
- **System Integration and Experimental Validation:** A crucial next step would be the physical fabrication of the proposed 4-bit VCO-based ADC as an integrated circuit. Experimental characterization of the fabricated chip would allow for a direct comparison with simulation results and a thorough assessment of its real-world performance. Integration with a complete biomedical sensor front-end (for PPG signal acquisition as outlined in Chapter 2) would provide a practical demonstration of its efficacy in a target application.
- **Exploration of Alternative VCO Topologies for Linearity:** While the current-starved ring oscillator with enhancements was effective, future work could explore other VCO topologies, or more advanced modifications to ring oscillators, that inherently offer better linearity or phase noise performance, potentially simplifying the overall ADC design or pushing its performance boundaries further.

Addressing these areas could lead to further advancements in VCO-based ADC technology, paving the way for even more efficient and higher-performing data converters suitable for a diverse range of applications.

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APPENDIX A

PYTHON CODE

A.1 Dynamic Response Simulation Script

```
1 import pandas as pd
2 import numpy as np
3 from scipy.signal import resample
4 from scipy.fft import fft
5 from numpy import blackman
6 import matplotlib.pyplot as plt
7
8 def calc_sndr(x, fs):
9     # Remove DC
10    x = x - np.mean(x)
11    N = x.size
12
13    # Apply Blackman window
14    w = blackman(N)
15    xw = x * w
16
17    # FFT
18    X = fft(xw)
19    P2 = np.abs(X)**2
20    P1 = P2[: N//2]
21
22    # Zero out DC
23    P1[0] = 0
24
25    # Find the fundamental
26    fund_bin = np.argmax(P1)
27
28    # Signal power
29    P_sig = P1[fund_bin]
30
31    # Zero that bin + neighbors to kill leakage
32    P1_sndr = P1.copy()
33    P1_sndr[fund_bin] = 0
34    if fund_bin > 0:
35        P1_sndr[fund_bin - 1] = 0
36    if fund_bin < len(P1) - 1:
37        P1_sndr[fund_bin + 1] = 0
38
39    # Sum the rest as noise+distortion
40    P_nd = np.sum(P1_sndr)
41
42    # Compute SNDR in dB
43    sndr_db = 10 * np.log10(P_sig / P_nd)
44    return sndr_db, fund_bin, x, N, P1, P2, fs
```

```

45
46 # --- MAIN SCRIPT ---
47
48 # Load non-uniformly sampled ADC comparator outputs
49 df = pd.read_csv("asy_data_800khz.csv")
50 df = df.rename(columns={
51     df.columns[0]: "time",
52     df.columns[1]: "bit3",
53     df.columns[2]: "bit2",
54     df.columns[3]: "bit1",
55     df.columns[4]: "bit0"
56 })
57
58 # Threshold each comparator output to get digital bits
59 Vth = 0.6
60 bit3 = (df["bit3"].values > Vth).astype(np.uint8)
61 bit2 = (df["bit2"].values > Vth).astype(np.uint8)
62 bit1 = (df["bit1"].values > Vth).astype(np.uint8)
63 bit0 = (df["bit0"].values > Vth).astype(np.uint8)
64
65 # Form 4 bit ADC code (0 15 )
66 adc_code = (bit3 << 3) | (bit2 << 2) | (bit1 << 1) | bit0
67 adc_code = (adc_code - 1) % 16
68 # Convert codes back to analog volts
69 Nbits = 4
70 Vmin, Vmax = 0.53, 1.6
71 analog = (adc_code.astype(float) / (2**Nbits - 1)) * (Vmax - Vmin) + Vmin
72
73 # Resample to a uniform time grid at Fs_target
74 Fs_target = 41e6
75 time = df["time"].values
76 capture_time = time[-1] - time[0]
77 Npts = int(round(capture_time * Fs_target))
78 analog_uniform = resample(analog, Npts)
79
80 # Calculate SNDR
81 sndr, fund_bin, x, N, P1, P2, fs = calc_sndr(analog_uniform, Fs_target)
82 print(f"Detected fundamental bin: {fund_bin}")
83 print(f"SNDR = {sndr:.2f} dB")
84 print(analog_uniform)
85 # Plot the reconstructed analog waveform
86 Ts = 1 / Fs_target
87 t_plot = np.arange(analog.size) * Ts * 1e6 # in microseconds
88
89 plt.figure(figsize=(8, 4))
90 plt.plot(np.arange(len(analog_uniform)), analog_uniform, marker='o', linestyle='--')
91 plt.title("Reconstructed Analog Signal from ADC Output")
92 plt.xlabel("Time (\mu s)")
93 plt.ylabel("Voltage (V)")
94 plt.grid(True)
95 plt.tight_layout()
96 plt.show()

```

```
97
98 # Power Spectrum and SFDR
99
100 # Avoid divide-by-zero by adding a small epsilon
101 epsilon = 1e-12
102 P1_dB = 10 * np.log10((P1 + epsilon) / (np.max(P2) + epsilon))
103 freqs = np.linspace(0, Fs_target / 2, len(P1_dB)) / 1e6
104
105 # Identify worst spur (excluding fundamental and its neighbors)
106 P1_temp = P1.copy()
107 P1_temp[fund_bin] = 0
108 if fund_bin > 0:
109     P1_temp[fund_bin - 1] = 0
110 if fund_bin < len(P1_temp) - 1:
111     P1_temp[fund_bin + 1] = 0
112 worst_spur_bin = np.argmax(P1_temp)
113
114 # Calculate SFDR (power ratio in dB)
115 spur_power = P1[worst_spur_bin] + epsilon
116 sfdr = 10 * np.log10((P1[fund_bin] + epsilon) / spur_power)
117 spur_dB = 10 * np.log10(spur_power / (np.max(P2) + epsilon))
118 print(f"SFDR= {sfdr:.2f}")
```

