

Wideband and Linear Current Starved VCO with Source Degeneration and Integrated Charge Pump for ADC Front Ends

Md. Mobin Khan¹, Md. Maruf Islam², Md. Galib Hasan³,

Tasmia Hassan Saika⁴ and Md Tawfiq Amin⁵

^{1,2,3,4,5}Department of EECE, Military Institution of Science and Technology

Dhaka, 1206, Bangladesh

Email: ¹mobin.ovi987@gmail.com, ²mdmarufislam740@gmail.com, ³hasangalib93@gmail.com,

⁴tasmia@eece.mist.ac.bd, ⁵tawfiqamin@gmail.com

Abstract—For Voltage Controlled Oscillator (VCO) based Analog-to-Digital Converter (ADC) front ends, achieving high linearity over a wide tuning range without compromising phase noise is a critical design challenge to get better performance of ADC. This paper proposes a novel five-stage current-starved ring oscillator (CSRO) with charge pump integration and diode-connected NMOS source degeneration technique on 90nm CMOS technology for Voltage Controlled Oscillator based ADC applications. The Bandwidth is maintained where the higher frequency is sixteen times of the lower oscillation frequency for four bit ADC application. The PSS simulation confirms the frequency range, linearity for both schematic and post layout simulation. As the source degeneration resistance are replaced by cmos transistor, silicon area consumption is significantly reduced while achieving a highly reasonable linearity. The charge pump is introduced with tuned charge pump current to produce sharp transition than conventional inverter which leads to reduction of phase noise. With the tuning voltage from 0.52V to 1.6V the frequency ranges from 38Mhz to 619Mhz. The average power consumption for two terminal voltage varies from $220.9\mu\text{W}$ to $354.6\mu\text{W}$. The phase noise is achieved from -88.63 to -87.66 dBc/Hz, at 1MHz offset frequency. The value of dc power consumption at center frequency 329MHz is $524.4\mu\text{W}$ which leads to figure of merit of this VCO is -141.15dBc/Hz. The proposed design occupies a remarkably compact area of $292.94\mu\text{m}^2$. All simulations were performed considering parasitic elements extracted from the layout and the values mentioned here is from post layout simulation.

Index Terms—CSRO, Source degeneration, Charge pump, Phase noise, PSS simulation.

I. INTRODUCTION

Nowadays, a wide range of Internet of Things (IoT) applications, including healthcare, smart home, smart city, and many other domains, are being widely adopted globally due to considerable advancements in technology in this industry [1]. VCO-based Analog-to-Digital Converters(ADCs) are gaining favorable position in scaled CMOS technologies for digital-friendly implementations due to their time-domain operation and intrinsic first order noise-shaping feature [2] [3] [4] [5].

VCO-based ADCs operate by first converting the analog input into frequency using a VCO shown in Figure 1, which

is then converted to digital values by a Frequency to Digital Converter (FDC) [6]. Often implemented with ring oscillators like Current-Starved Ring Oscillators (CSROs), the VCO's frequency is set by controlling the delay of its inverting cells via a current-starved bias circuit. In this way, VCOs can be used as transducers that convert voltage to frequency, allowing the designers to process signals within the time domain.

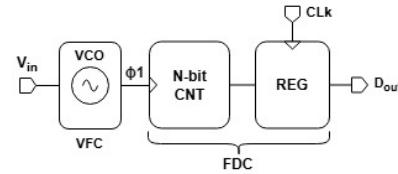


Fig. 1: ADC Block Diagram.

CSROs are particularly preferred in this role due to their straightforward integration, wide tuning capability, and low power consumption [7]–[9]. However, achieving highly linear relation between VCO's input control voltage and output frequency presents a significant challenge. Any nonlinearity introduces distortion and harmonics, ultimately degrading the ADC's effective resolution (ENOB) [2]. While system-level compensation strategies like calibration or feedback loops are available [2], [10], [11], they often add considerable complexity. This motivates the focus on circuit-level techniques [7], [12], to mitigate non-linearity directly within the VCO, aiming for a simpler overall system structure [2].

Conventional CSROs offer a wide tuning range, they may suffer from linearity issues and increased phase noise [2]. In order to improve the performance of CSROs, researchers have introduced novel techniques. Some approaches include: Employing differential delay cells to suppress even-order distortions and common-mode noise [2], using only NMOS sinks or PMOS sources to reduce complexity and power consumption [7], introducing symmetric loads in parallel with the current source/sink transistors to improve linearity and stability [7], using an output-switch scheme to achieve improved

power-delay product and phase-noise bandwidth product [7].

Further, phase noise is an important consideration in VCO design for ADC applications [8]. It is generally worse in ring oscillators compared to LC oscillators [8]. This phase noise translates to jitter in the time domain, further limiting the ADC's resolution and overall performance. To address these conflicting requirements of wide tuning range, linearity, and low phase noise simultaneously, this paper presents a novel CSRO architecture. Our primary contribution is the co-design of a diode-connected NMOS source degeneration scheme to linearize the V-F curve and an integrated charge pump to sharpen switching transitions, thereby reducing phase noise. The resulting design achieves the performance metrics necessary for low-power, wide-range VCO-based ADC applications.

II. CONVENTIONAL VCO

Turning to the standard Current Starved Voltage Controlled Oscillator (CSVCO) implementation, illustrated in Figure 2, the design typically uses an odd number of inverting delay stages (N) connected sequentially to form a ring structure [13], [14].

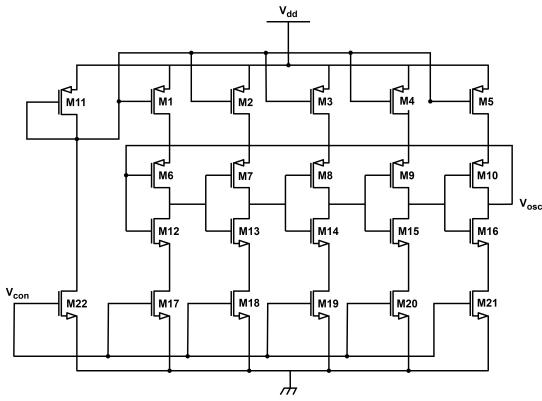


Fig. 2: Conventional Current Starved VCO.

CSROs control the delay of their inverter stages by limiting the current available to charge or discharge load capacitances of the stages, which facilitates the voltage control of their oscillation frequency [7], [9], [11]. The oscillation frequency of a CSRO can be tuned by varying a control voltage [7], [9], [11].

The operating frequency relies fundamentally on the propagation delay (T_d) for each stage. The core idea behind the CSRO is to render this delay voltage-controllable by "starving" the bias current (I_d) which is required to charge and discharge the total load capacitance (C_{tot}) at each stage's output. This modulation is commonly accomplished through the current mirrors powered by the control voltage (V_{con}) [11].

As a rule, the oscillation period varies inversely with the number of stages on the device and directly with the stage delay, which is approximated by [15]

$$t = \frac{T_d}{2N}$$

. Thus, it can be crudely stated that the oscillation frequency is [13] [16]

$$f_{osc} = \frac{I_D}{NC_{tot} \cdot V_{DD}}$$

and shows dependence on the starved current and load capacitance. Total capacitance C_{tot} is the summation of stage's output capacitance C_{out} and input capacitance C_{in} which can be expressed as [7]

$$C_{tot} = C_{out} + C_{in}$$

Based on standard MOS capacitance models, this can further be expressed in inverter transistor dimensions and process parameters as [7]:

$$C_{tot} = C'_{ox}(W_pL_p + W_nL_n) + \frac{3}{2}C'_{ox}(W_pL_p + W_nL_n)$$

The equation leads to

$$C_{tot} = \frac{5}{2}C'_{ox}(W_pL_p + W_nL_n)$$

So, while providing wide tuning range, conventional CSROs often exhibit non-linear frequency control, particularly when the starving transistors transition into the triode region at higher control voltages [7], and suffer from relatively high phase noise [8].

III. PROPOSED VCO

In the proposed current starved ring VCO architecture shown in Figure 5, M₁₁ and M₂₂ are the global current starving component that regulates the total current flows through the entire VCO not in an individual stage. M₁₁ is biased in such a way it acts as an voltage controlled current source and always operates in saturation region. If V_{con} increases M₁₁ limits the current flow into pMOS pull up transistors (M₁, M₃, M₅) and directly impacts the rising edge slope and delay per stage. Similarly, M₂₂ acts as voltage controlled current sink that allows more discharge current to flow when V_{ctrl} increases. It controls the pull down operation of nMOS transistors of each stage (M₁₇, M₁₉, M₂₁). The current in each inverter stage defines the charging discharging rate of inverter output node, delay and oscillation frequency.

$$f_{osc} \approx \frac{1}{2N \cdot t_{delay}} \propto I_{stage}$$

For the ADC purpose, to maintain this wide tuning range, delay of each stage need to be increased. Therefore capacitor load is used in each delay cell, then frequency bandwidth can be tuned as

$$t \propto \frac{C_{tot}}{I_d}$$

In our proposed VCO the total capacitance of three inverter stage is

$$C_{tot} = \frac{5}{2}C_{ox}(w_pL_p + w_nL_n) + C$$

$$C = C_1 = C_3 = C_5$$

Therefore the bandwidth is tuned in a well mannered and achieved the range from 39 MHz to 697 MHz which is

sufficient for the condition. But variations in temperature can alter capacitance values and other characteristics, potentially compromising circuit stability. Parasitic inductance and resistance, can adversely affect performance, especially at high frequencies [17]. Achieving high capacitance values necessitates larger component sizes, which can be impractical in compact IC layouts [18]. For solving the issue, traditional capacitor is replaced with Pmos capacitor

The issue of non-linearity of the current starved ring vco arises because of the non-linear behavior of drain current of current starved transistor with the controlling voltage. The drain current saturates with the increasing voltage since the initial current is much higher. In Figure 3 current saturates after 1.1 voltage. But the source degeneration resistors (M_{23} - M_{28}) limit the initial current to a much lower value and makes the current increasing linearly with increasing voltage shown in Figure3 where the current is raising till 1.6 voltage.

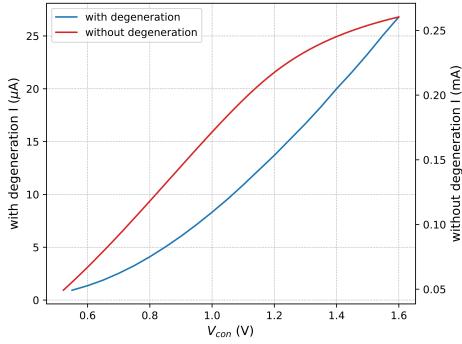


Fig. 3: Impact of source degeneration on Voltage-Current relationship

Regarding fabrication process and robustness, diode connected load is replaces source degeneration resistors where transistor will always be operated in saturation region.

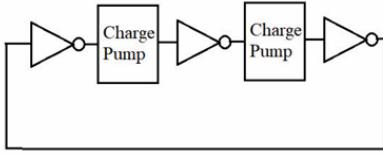


Fig. 4: Charge Pump application in CSRVCO [8]

In proposed architecture 2nd and 4th stages are two charge pump stages as shown in Figure 4, where the switching device is inverter consisting with M_7 , M_{13} and M_9 , M_{15} transistors. Current starved pMOS (M_2 , M_4) and nMOS (M_{18} , M_{20}) is connected to GND and VDD that strengthen the sourcing current to the inverter pull up operation and sinking current also. In addition to that the small capacitance making fast switching of the inverter output voltage.

$$I_p = C \frac{dV}{dt}$$

$$C = C_2 = C_4$$

Moreover, the source degeneration resistors (M_{24} , M_{26}) are one of the key factor for smooth transition. The gate source voltage of nMOS current starved transistor is a function of voltage drop across degeneration resistor, that creates sink current ability from inverter more modulated and smooth.

$$V_{GS} = V_{DD} - V_s$$

This makes more controlled transition and less sensitive to supply and thermal variation leads to less timing jitter, narrower spectral width and lower phase noise.

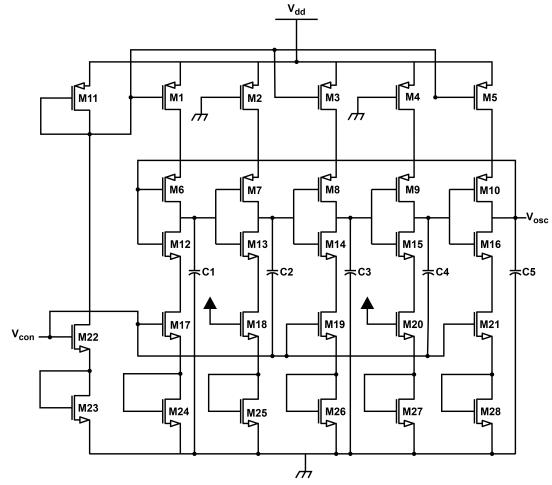


Fig. 5: Proposed Current Starved VCO.

TABLE I: Physical Dimension of Devices

Device Number	Width	Length
M_{11}	1 μm	180nm
M_1 , M_3 , M_5	900nm	180nm
M_2 , M_4	4 μm	180nm
M_6 - M_{10}	1 μm	100nm
M_{12} - M_{16}	500nm	100nm
M_{17} , M_{19} , M_{21}	450nm	180nm
M_{18} , M_{20}	2 μm	180nm
M_{22}	500nm	180nm
M_{24} - M_{28}	8.41 μm	180nm
M_{23}	120nm	180nm

IV. SIMULATION RESULTS

The proposed architecture is designed and simulated in 90 nm CMOS process technology in the cadence virtuoso environment. Transient analysis, pss, phase-noise and DC analysis have been performed on the schematic design and also post layout design to measure the performance attributes of the proposed topology.

Figure 6 shows the transient analysis that exhibits a sine wave that features the output of oscillator. Figure 7, illustrates a reasonably linear relationship between oscillation frequency and gradually increasing control voltages from 0.52 V to 1.6 V, maintaining a wide tuning range from 39 to 697 MHz in schematic and from 38 to 619 MHz in post layout. The lowest

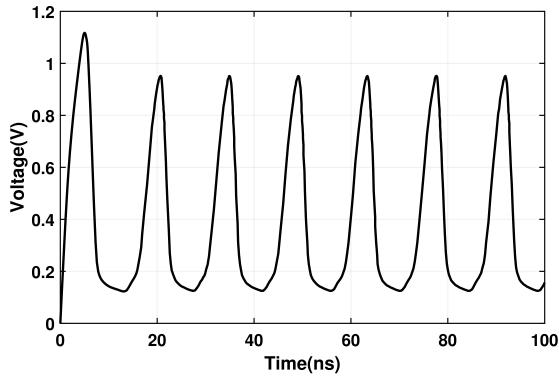


Fig. 6: Transient response at $V_{con} = 0.6V$ (Post layout)

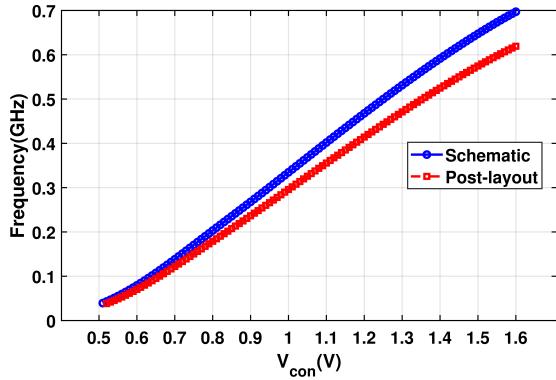


Fig. 7: Oscillation frequency for different control voltages.

frequency defines the oscillation frequency of the VCO, while the highest frequency satisfies the condition of being 16 times of the oscillation frequency.

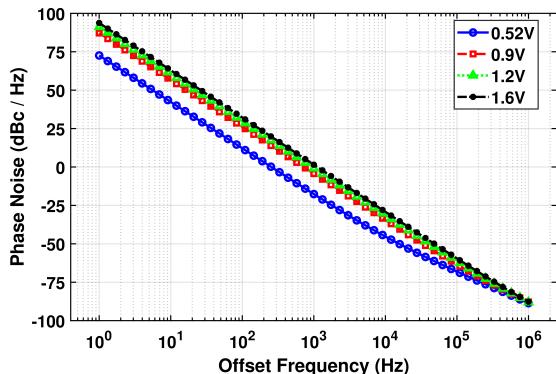


Fig. 8: Phase noise for different V_{con} (Post Layout).

Figure 8, represents the phase noise at the offset frequency of 1 MHz from -88.63 dBc/Hz to -87.66 dBc/Hz for two terminal control voltage. The figure of merit, FOM (in dBc/Hz), incorporating three basic performance parameters is calculated by the following equation [19],

$$FOM = L(\Delta\omega) + 10 \log \left(\frac{P_{diss}}{1 \text{ mW}} \right) - 20 \log \left(\frac{\omega_o}{\Delta\omega} \right)$$

Oscillation center frequency is 329MHz. Phase noise and DC power consumption at corresponding frequency is -87.92 dBc/Hz and $524.4 \mu\text{W}$. That exhibits the FOM of VCO is -141.15 dBc/Hz.

In Figure 9 and Figure 10, the PSS simulation and Phase noise is calculated over different process corner variation Fast Fast (FF), Fast Slow (FS), Slow Slow (SS), Slow Fast (SF). For all cases the bandwidth has meet the condition where the highest frequency is sixteen times of lower frequency and a stable phase noise is achieved at center frequency.

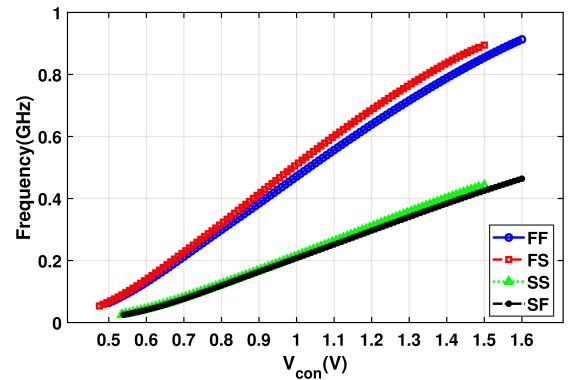


Fig. 9: Oscillation frequency vs V_{con} for different corner conditions.

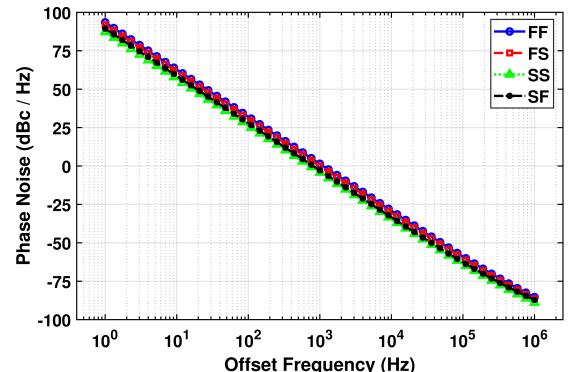


Fig. 10: Phase noise vs offset frequency for different corner condition.

The variation of temperature is an important metric for measuring performance due to affecting the MOSFET parameters like threshold voltage, mobility etc. The performance parameters of CSVCO's have been simulated from -65°C to 65°C that also includes PSS and Phase noise simulation.

In Figure 11 the PSS graph exhibits more linear relationship of frequency and V_{con} with the increasing temperature but lowers the bandwidth.

In Figure 12, the phase noise are -86.29 dBc/Hz for -65°C 86.93 dBc/Hz for 65°C at 1 MHz offset frequency. Therefore the phase noise is much stable with increase in temperature.

Figure 13 shows the performance of worst case scenario of phase noise where charge pump makes a more stable

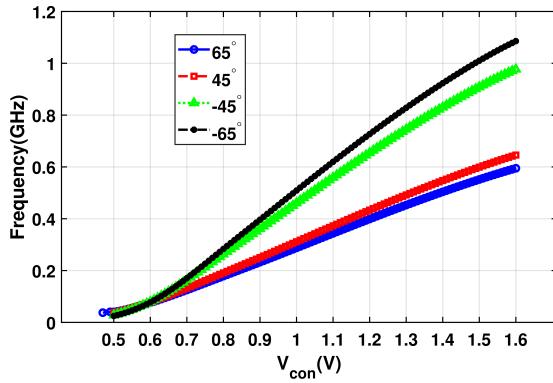


Fig. 11: Oscillation frequency vs control voltage for different temperatures.

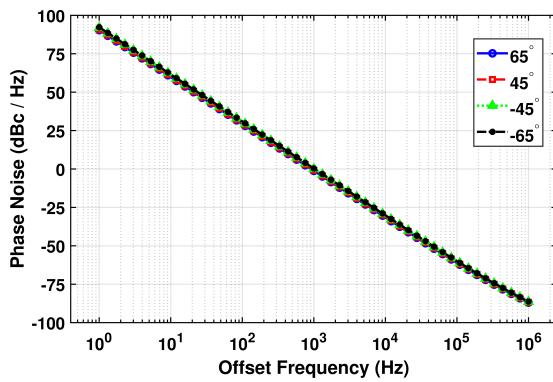


Fig. 12: Phase noise vs offset frequency for different temperature.

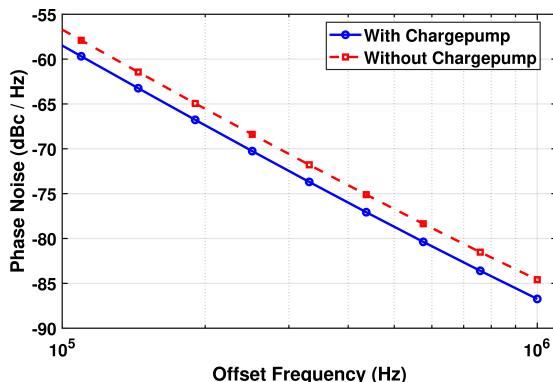


Fig. 13: Phase Noise difference with conventional and proposed VCO

phase noise with -86.73 dBc/Hz where the other shows -84.59 dBc/Hz .

The Figure 14 shows that higher temperatures in lower DC power consumption by the proposed architecture.

Figure 15 to Figure 17, illustrates Monte Carlo histogram for DC power consumption, Phase noise, Center frequency respectively. It is performed from the post layout simulation and have taken account for sufficient number of samples.

Figure 18 illustrates the layout of the proposed design.

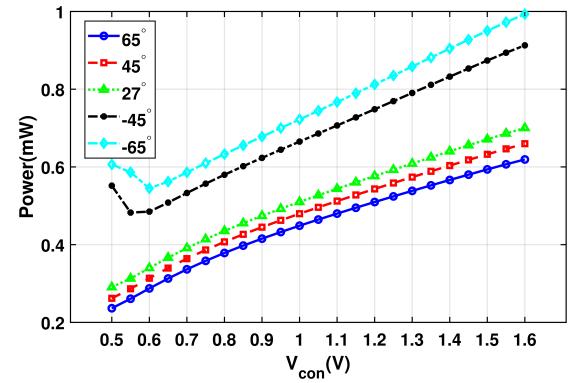


Fig. 14: DC Power consumption vs V_{con} for different temp.

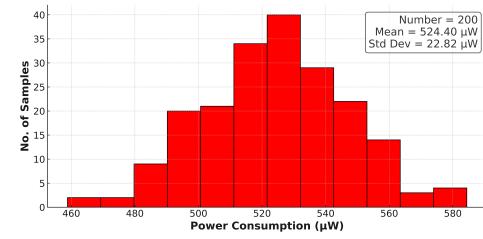


Fig. 15: Statistical analysis of DC power consumption for $V_{\text{con}} = 1.05\text{V}$

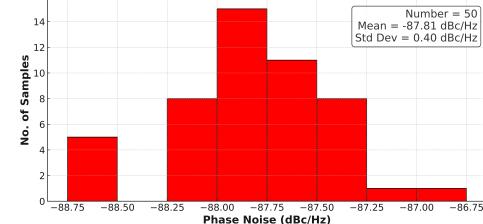


Fig. 16: Statistical analysis of Phase Noise for $V_{\text{con}} = 1.05\text{V}$

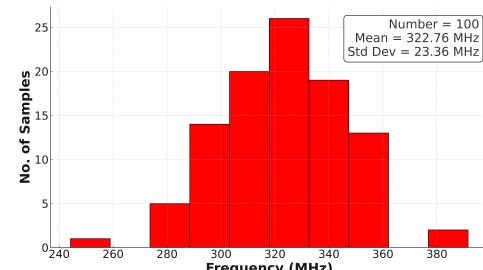


Fig. 17: Statistical analysis of centre Frequency for $V_{\text{con}} = 1.05\text{V}$

For interconnecting purposes, Metal1, Metal2, Metal3, Metal5, and Polysilicon were used. The total area used is $17.605 \times 16.64 \mu\text{m}$ or $292.94 \mu\text{m}^2$.

All the important parameters of VCO is compared with four other published works. The comparison table shown in Table II shows that the proposed circuit achieves a linear high tuning Bandwidth and low phase noise.

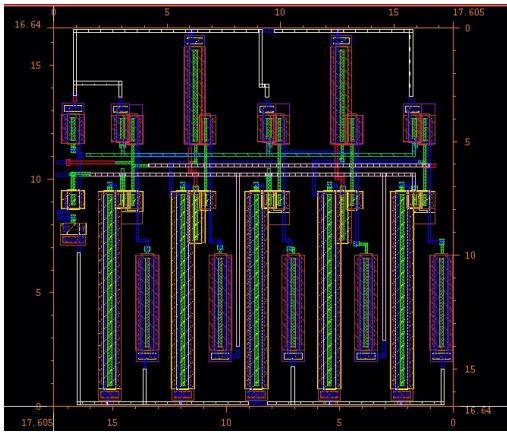


Fig. 18: Layout of the proposed CS-VCO.

TABLE II: Performance Comparison Table

Parameters	[20]	[21]	[22]	[8]	This Work
Technology	180nm	90nm	90nm	-	90nm
Supply Voltage (V)	1.8	0.6	1.2	-	1.8
Power Consumption (μW)	260	771	73.69	-	354.6
Center Frequency (MHz)	404.5	-	13.51	-	323
Tuning Range (%)	92.45	94	90	-	93.86
Phase Noise (dBc/Hz)	-82.28	-89	-112.25	-86.29	-88.63
FOM (dBc/Hz)	-140.27	-	-144.749	-	-141.15

V. CONCLUSION

The novel five-stage Current-Starved Voltage Controlled Oscillator in 90nm CMOS, incorporates the diode-connected NMOS source degeneration and an integrated charge pump. These techniques effectively enhance V/f linearity while significantly reducing phase noise compared to conventional designs. Simulations, accounting for layout parasitics and process/temperature variations, validate the architecture's robustness, demonstrating a wide frequency tuning range, consistent low phase noise (approximately -88 dBc/Hz @ 1MHz offset), and low power consumption within a compact area. The achieved performance characteristics makes the proposed VCO highly suitable for low-power ADC application at sensor node of Biomedical implants as well as CIM application where power efficiency and stable operation are critical.

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