Throughout this project, you are supposed to implement a GSM-900 receiver. A common RF receiver chain is shown in Fig.1. It has an LNA, a down-converter, a TIA, and a VGA, an A/D (analog-to-digital converter), followed by a DSP (digital signal processing) unit.

- In some chips, the A/D and DSP are not included, and a separate chip converts the analog baseband I/Q signals into the digital domain.
- In some chips, the A/D is included but the DSP unit is not. For example, an FPGA is used as the DSP unit, or a dedicated digital chip (often called digital modem) is used.

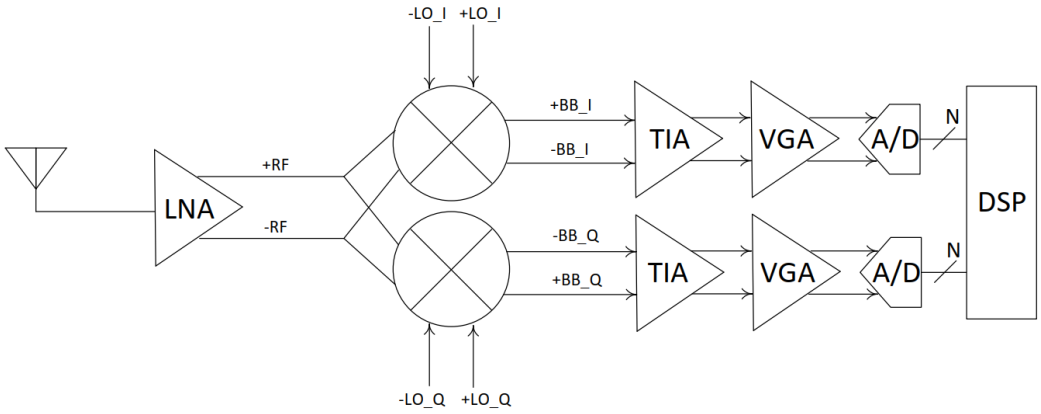


Fig. 1: RF Receiver Chain

A CMOS RF/analog IC designer deals with the design of every block that is shown in Fig.1, except for the DSP. The architecture in Fig. 1 is called a zero-IF (or homodyne) receiver. This modulated RF signal is down converted to zero IF using an LO that has the same frequency as the carrier frequency of the incoming RF signal.

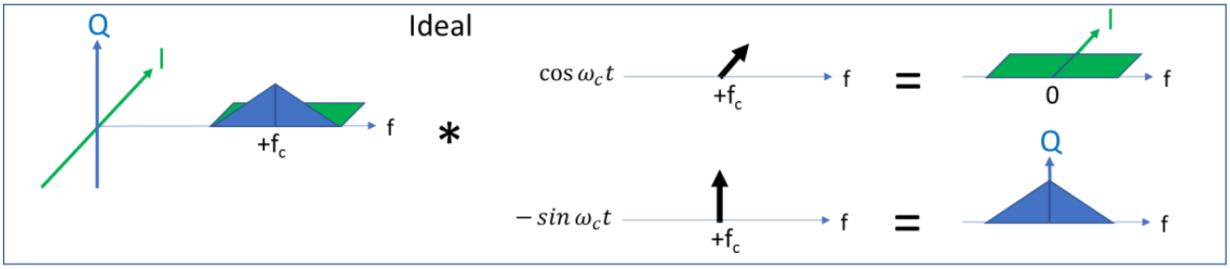


Fig. 2: A zero-IF receiver in frequency domain

Fig. 2 shows the frequency domain representation of an ideal zero-IF receiver. The real signal received by the antenna is amplified by an LNA. This real signal has distinct data that are modulated in two orthogonal carriers that have the same frequency but are 90 degrees out of phase, namely, “in-phase” and “quadrature”. The downconverter is then switched on and off with an LO frequency that is the same as the incoming carrier frequency. The output of the downconverter is then filtered to remove the higher frequencies and only keep the lower frequencies.

Fig. 3 shows a typical implementation of the TIA and the VGA in a CMOS receiver. You have already worked out the equations showing the frequency domain transfer function of this TIA+ VGA in previous electronics courses.

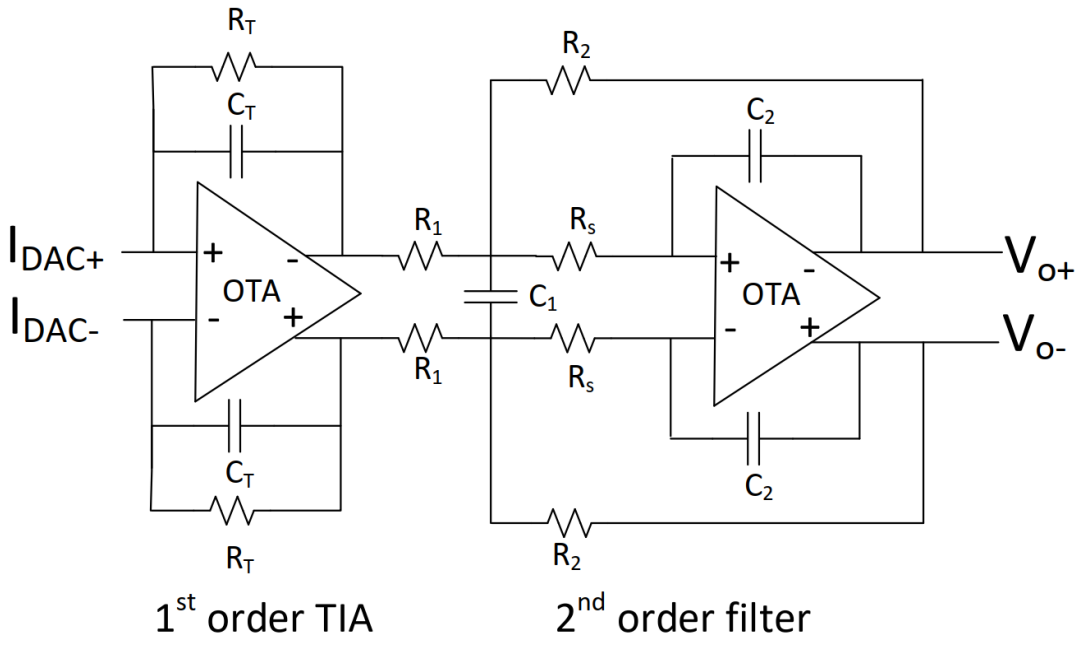
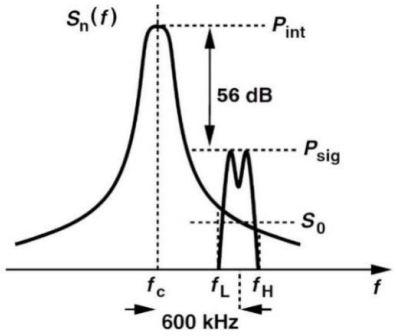


Fig. 3: 3rd order Butterworth Filter

We will not use the circuits in Fig. 3 for the sake of simplicity and will instead implement the RF blocks in this chain.

1- Implement the LNA based on the specifications extracted in the previous phase of the project using ADS.
2- Implement the downconverter based on the specifications extracted in the previous phase of the project using ADS. Use *P_nTone* as the signal source. Consider a frequency component at the frequency offset of 600 KHz, which is 56dB larger than the main component.



3- We already have done the downconverter and the LNA designs. We just need to connect the two designs and run the final chain simulations.