In this project, the design of a common gate LNA is discussed (Fig. 1). To understand more about the design steps, you can refer to pages 279 to 283 of Razavi's book (RF Microelectronics, second edition).

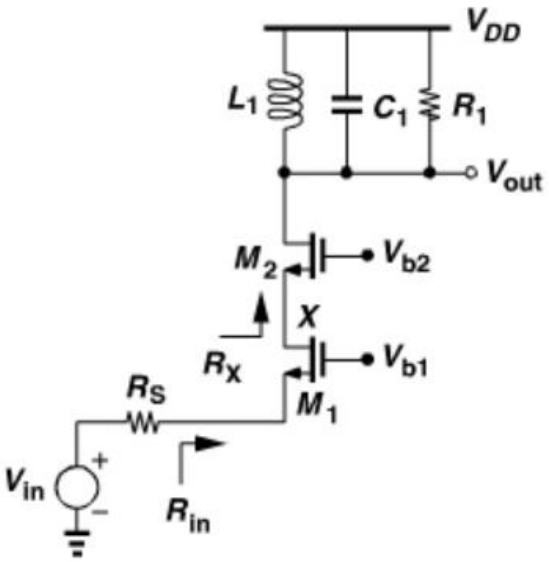
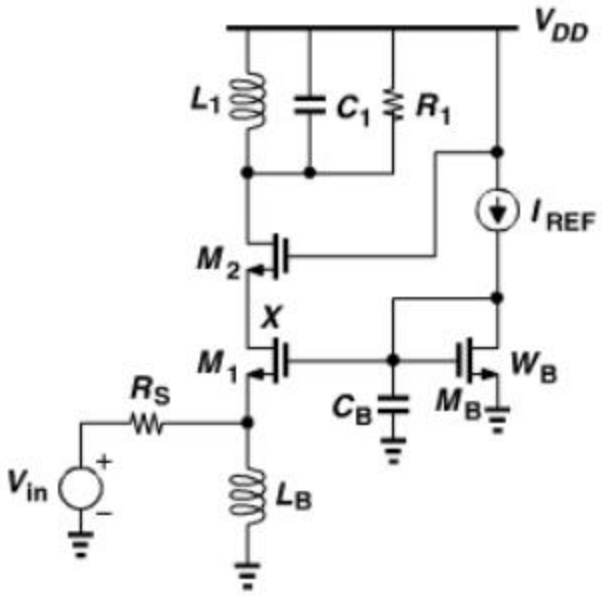


Figure 1- CG cascode LNA

The aim of the project is to achieve an LNA with gain of 18 dB at frequency of 2.4 GHz. Perform the design procedure according to the following steps. For simulation, use 180 nm CMOS technology in ADS software.

1. Assume center frequency = 2.4 GHz, V_{DD} = 1.8 V, Rs = 50 Ohm, L = 180 nm, and W_1 = 30 um.
2. Plot gm versus I_D.
3. Determine I_D so that gm = $1/R_s$.
4. Determine L_B (Fig. 2).



5. *Figure 2- CG cascode LNA with bias circuit*

6. For Q = 10, determine R_p (parallel resistance of L_B).
7. Design biasing circuit by choose the size of transistor M_B and I_{ref}.
8. Determine the size of M_2.
9. Determine R_1 and L_1 to obtain mentioned gain. R_1 is the parallel resistance of L_1 with Q = 10.
10. Plot S11 versus frequency and specify BW (S11 < -10 dB).
11. Plot NF and gain in specified BW.
12. Determine IIP3.