In this project, the design of a common source LNA is discussed (Fig. 1). Similar to mini project #1, to understand more about the design steps, you can refer Razavi's book (RF Microelectronics, second edition, pages 291 to 293).

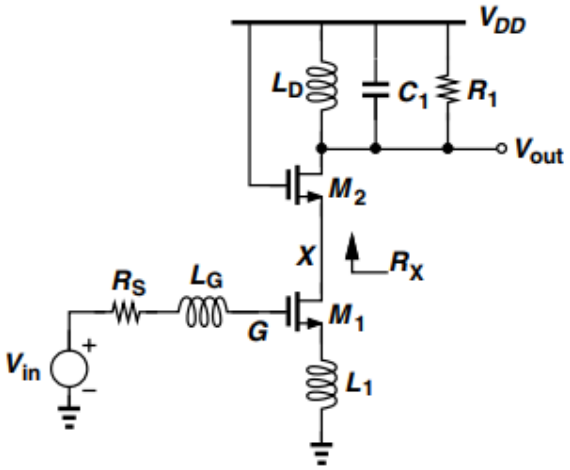

Figure 1- Inductively-Degenerated CS cascode LNA

This design can be done in two different ways. In the first section, you have to design this LNA knowing the value of some elements of the circuit and gain. But, in the second section, you are asked to design the circuit for a specified noise figure and gain. For simulation, use 180 nm CMOS technology in ADS software (V_{DD} = 1.8 V and L = 180 nm). Consider the center frequency as f = 2.4 GHz.

Section I:

Perform the design procedure according to the following steps to obtain A_v = 25 dB. Assume R_s = 50 Ohm, L_1 = 5 nH, L_G = 35 nH and C_{pad} = 50 fF.

1. Determine C_{gs} and gm of M_1.
2. Determine size of M_2.
3. Determine L_D with Q = 10. Add another resistor if needed to obtain mentioned gain.
4. Design biasing circuit by specifying value of I_B, R_B and size of M_B (Figure 2).

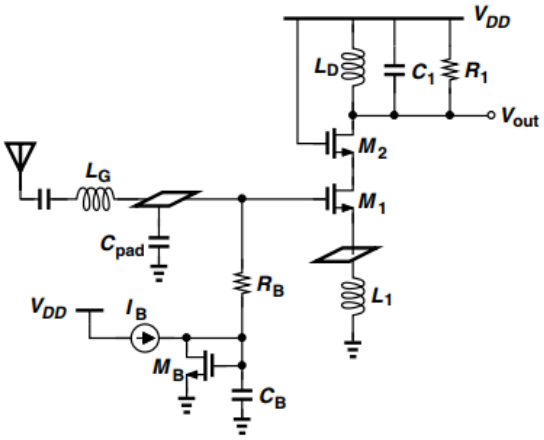

Figure 2-Inductively-Degenerated CS cascode LNA with bias circuit.

5. Optimize the value of L_G to have matching at center frequency (if needed).
6. Plot NF and gain in 0 to 12 GHz.

Section II:

Perform the design procedure according to the following steps to obtain NF less than 1.7 dB and A_v = 25 dB. Assume R_s = 50 Ohm, L_1 = 5 nH and C_{pad} = 50 fF.

1. Determine gm and C_{gs} of M_1.
2. Determine L_G.
3. Repeat steps 2 to 6 of section **I**.