Experiment 1 - Clock and Periodic Signal Generation

Mehdi Jamalkhah, 810100111

Mobina Mehrazar, 810100216

***Abstract*— This document is a report for experiment #1 of Digital Logic Design Laboratory at ECE department, University of Tehran. The purpose of this experiment is to provide different methods for clock generation in digital systems.**

***Keywords*— clock generation, clock signal, period, threshold, frequency, duty cycle.**

I. Introduction

The goal of this report is to introduce the concept of static characteristics of digital logic gates, delay times, clock frequency generation and digital system using schematic diagram.

II. Clock Generation using ICs and Analog Components

In this part, we will use 74 series discrete logic devices for implementing the circuits of clock generation.

A. Ring oscillator

A ring oscillator is composed of a chain of odd number of inverters (e.g. 5 inverters) in a ring as shown in figure 1.

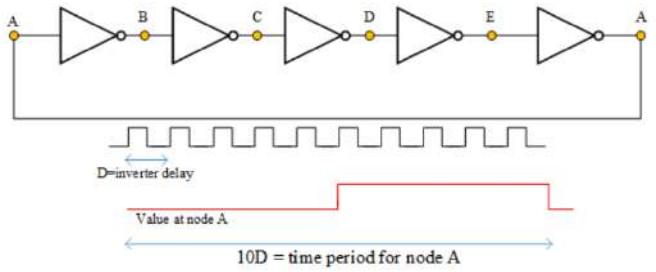

Fig. 1 **Ring oscillator**

It not only can be used for clock generation but also is used to measure the delay of single inverter. For this purpose, we consider the period time of output and use the following formula.

$$Delay_{inv} = \frac{T}{2 \times N} \quad (1)$$

Where N is number of inverters and T is period time of output.

We consider one of inverters' output as the oscillator's output. Output wave is shown in figure 2.

1) Propagation delay of chain: The oscillator period is in all cases equal to twice the sum of individual delay of all stages (propagation delay of chain), since output toggles at each propagation of chain and after two toggles the period time of output will become completed.

$$\text{oscillator period} = 47.20 \text{ ns}$$
$$\text{propagation delay of chain} = 23.60 \text{ ns}$$

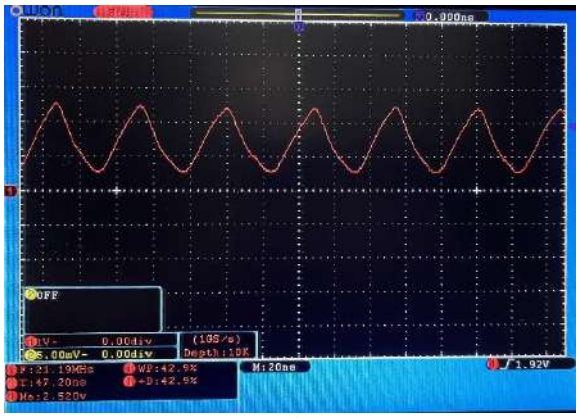

Fig. 2 Output of ring oscillator

2) Delay of a single inverter: As explained in part 1 the period time of output is twice of propagation delay of chain and the propagation delay is sum of individual delay of 5 inverters. By using (1):

$$Delay_{inv} = \frac{47.20}{2 \times 5} = 47.72\ ns$$

B. LM555 timer

We will implement the LM555 in astable mode using the wiring diagram from figure 3.

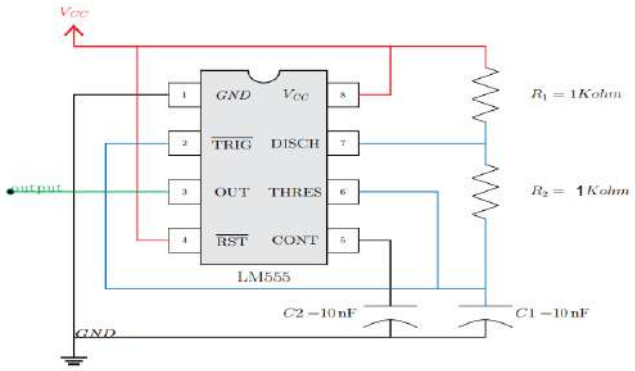

Fig. 3 LM5555 in astable mode

The external capacitor C1 charges through R_1 + R_2 and discharges through R_2. The charge time (output high) is given by:

$$T_1 = 0.693 \times (R_1 + R_2) \times C$$

And the discharge time (output low) by:

$$T_2 = 0.693 \times R_2 \times C$$

Total time period of square wave is

$$T = T_1 + T_2 = 0.693 \times (R_1 + 2R_2) \times C$$

Duty cycle can be computed by:

$$duty\ cycle = \frac{t_{output-high}}{t_{total}} = \frac{T_1}{T}$$

$$\rightarrow duty\ cycle = \frac{R_1 + R_2}{R_1 + 2R_2}$$

1) Output waveform: figure 4 shows output waveform of LM555 in astable mode with capacitor and resistor values that are shown in figure 3.

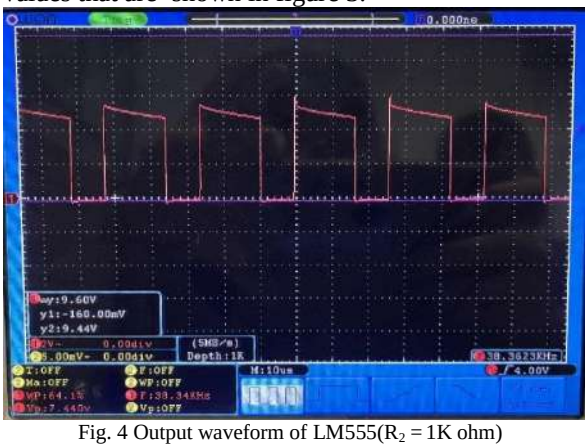

Fig. 4 Output waveform of LM555(R_2 = 1K ohm)

f = 38.34 kHz
T_1 = 16.5 us
T = 26 us
duty cycle = 63 %

2) Different values of R_2 resistor: produced clock frequencies by three different values of R_2 resistor is shown in figure 4, 5, and 6.

As R_2 resistor increases, the duty cycle gets closer to 50 % because we can ignore R_1 in duty cycle formula; and obviously frequency decreases.

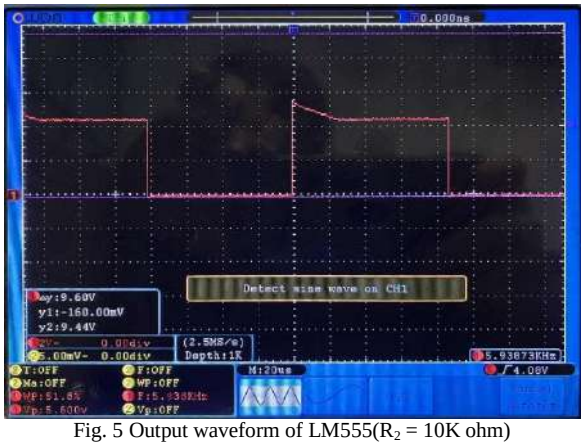

Fig. 5 Output waveform of LM555(R_2 = 10K ohm)

f = 5.93 kHz
T_1 = 88.0 us
T = 168.0 us
duty cycle = 52 %

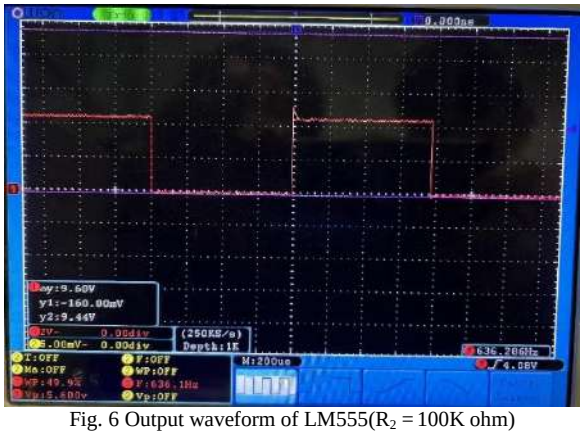

Fig. 6 Output waveform of LM555(R_2 = 100K ohm)

f = 636.1 Hz
T_1 = 800 us
T = 1600 us
duty cycle = 50 %

C. Schmitt trigger oscillator

Schmitt trigger oscillators are present in low-cost microcontrollers as a way to provide a reliable clock signal.

Let's explore the basic principle of operation of these circuits. First, let's look at very simple RC oscillator.

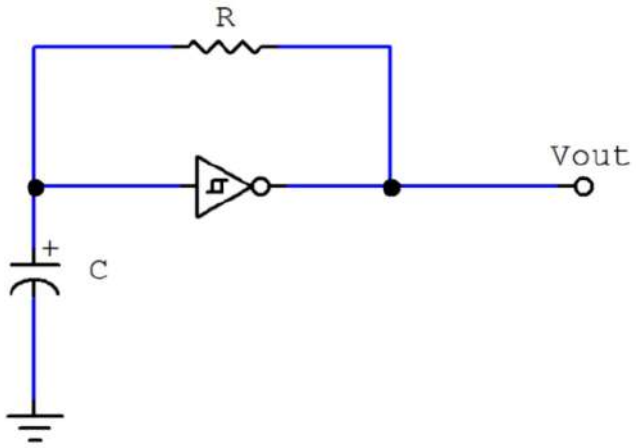

Fig. 7 Simple RC oscillator

Frequency of this oscillator can be calculated by

$$f = \frac{\alpha}{RC} \tag{2}$$

where α is a constant usually between 0.2 and 1.
Let's analyse this circuit and derive an expression for the α, then compare with the values that gained by experiment. For this purpose, we need to know what exactly are Schmitt trigger gates.

Schmitt trigger gates do not respond to a single voltage threshold in their inputs. Instead, their inputs respond to one rising (higher) threshold voltage and one falling (lower) threshold voltage: Whenever the input voltage exceeds the rising threshold, the input logical level is regarded as *high*, and whenever the input voltage drops below the falling threshold, the input is considered *low*. This means that a Schmitt Trigger input has some means of recalling its current level, which is the last level it changed to.

The following figure shows a noisy negative pulse that goes from 5V to 0V and then back up to 5V, and the output of a regular inverter and two different Schmitt Trigger inverters when fed that noisy signal:

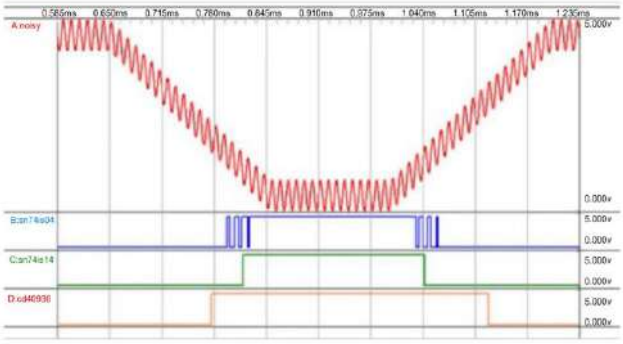

Fig. 8 A (Red): A Noisy signal fed to three inverters. B (Blue): The output of a 74LS04 regular TTL inverter. C (Green): The output of a 74LS14 Schmitt Trigger TTL inverter. D (Orange): The output of a Schmitt Trigger CMOS NAND gate configured as an inverter.

To produce an equation for the frequency of the output signal, we need to know its period, that is, how long it takes a cycle to complete. This is easily calculated by adding the high pulse width and the low pulse width.

The steady state high pulse width is the time it takes the capacitor's voltage to rise from the falling threshold voltage to the rising threshold voltage, while attempting to reach the high level voltage. This can be derived from the following equation:

$$V_c(t) = (V_{High} - V_{T-})\left(1 - e^{-\frac{t}{RC}}\right) + V_{T-} \tag{3}$$

$$V_c(t) = (V_{High} - V_{T-})\left(1 - e^{-\frac{t}{RC}}\right) + V_{T-}$$

$$V_{T+} = (V_{High} - V_{T-})\left(1 - e^{-\frac{t_h}{RC}}\right) + V_{T-}$$

$$\frac{V_{T+} - V_{T-}}{V_{High} - V_{T-}} = 1 - e^{-\frac{t_h}{RC}}$$

$$e^{-\frac{t_h}{RC}} = 1 - \frac{V_{T+} - V_{T-}}{V_{High} - V_{T-}}$$

$$-\frac{t_h}{RC} = \ln(1 - \frac{V_{T+} - V_{T-}}{V_{High} - V_{T-}})$$

$$t_h = -RC \ln(1 - \frac{V_{T+} - V_{T-}}{V_{High} - V_{T-}})$$

$$t_h = -RC \ln(\frac{V_{High} - V_{T+}}{V_{High} - V_{T-}})$$

$$t_h = RC \ln(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}}) \tag{4}$$

Now, for the low pulse width t_l, it's the time it takes for the capacitor's voltage to drop from the rising threshold V_{T+} down to the falling threshold V_{T-}, while attempting to reach zero volts, as follows.

$$V_c(t) = V_{T+} e^{-\frac{t}{RC}} \tag{5}$$

$$V_{T-} = V_{T+} e^{-\frac{t_l}{RC}}$$

$$e^{-\frac{t_l}{RC}} = \frac{V_{T-}}{V_{T+}}$$

$$-\frac{t_l}{RC} = \ln(\frac{V_{T-}}{V_{T+}})$$

$$t_l = -RC \ln(\frac{V_{T-}}{V_{T+}})$$

$$t_l = RC \ln(\frac{V_{T+}}{V_{T-}}) \quad (6)$$

Thus, the period of the output signal comes to

$$T = t_h + t_l \quad (7)$$

$$T = RC \ln\left(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}}\right) + RC \ln(\frac{V_{T+}}{V_{T-}})$$

$$T = RC[\ln\left(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}}\right) + \ln(\frac{V_{T+}}{V_{T-}})]$$

$$T = RC \ln(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}} \times \frac{V_{T+}}{V_{T-}})$$

$$f = \frac{1}{RC \ln(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}} \times \frac{V_{T+}}{V_{T-}})}$$

$$\alpha = \frac{1}{\ln(\frac{V_{High} - V_{T-}}{V_{High} - V_{T+}} \times \frac{V_{T+}}{V_{T-}})} \quad (8)$$

In 74LS14 inverter (V_{high} = 5V, and V_{low} = 0V), threshold voltages would be 0.55V and 2V which is written in its datasheet. So we expect α would be approximately 0.593 (calculated by (1)).

1) The following figures show output of this circuit with different values for the resistor.

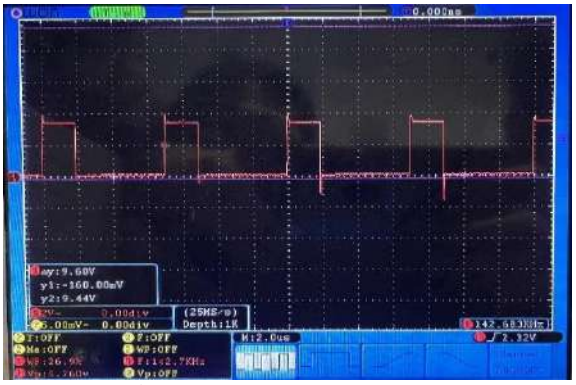

Fig. 9 Output of Schmitt trigger oscillator with C = 10nF, R = 470Ω

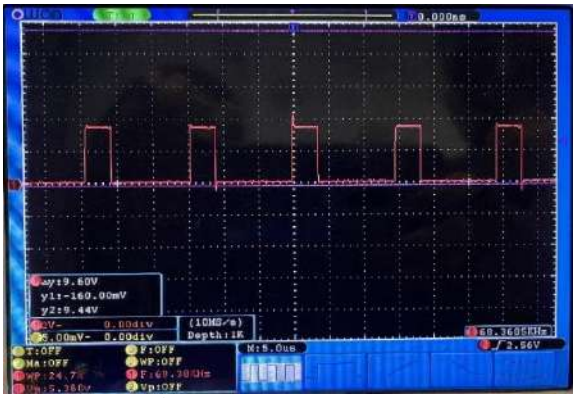

Fig. 10 Output of Schmitt trigger oscillator with C = 10nF, R = 1000Ω

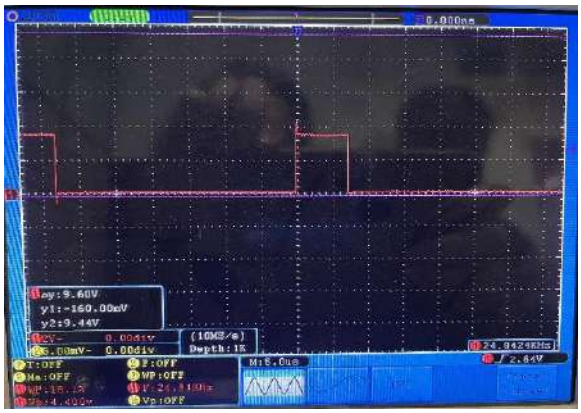

Fig. 11 Output of Schmitt trigger oscillator with C = 10nF, R = 2200Ω

2) Calculating α by (2):

$$C = 10\ nF,\ R = 470\ \Omega,\ f = 142.68\ Hz \rightarrow\ \alpha = 0.67$$

$$C = 10\ nF,\ R = 1000\ \Omega,\ f = 68.36\ KHz \rightarrow\ \alpha = 0.68$$

$$C = 10\ nF,\ R = 2200\ \Omega,\ f = 24.81\ KHz \rightarrow\ \alpha = 0.54$$

So α is approximately constant and is equal to the theoretically obtained value.

D. Synchronous counter as a frequency divider

Different clock signals can be produced by the aforementioned methods, but not all of them are suitable for all applications. Consider a 1Hz clock signal which can be easily produced by a LM555 timer. The timing error of this signal can be 1-2%, which is too much for a low frequency like this, while this error range is acceptable for higher frequencies. So, a higher frequency can be chosen and then a frequency divider can reduce the frequency to the desired one.

We load 256 – 200 = 56 as initial value to construct a divide by 200 synchronous up-counter.

$$56_d = 0011\_1000_b$$

We are going to use the ring oscillator of part A to generate a clock signal for clock input of the LSB counter.

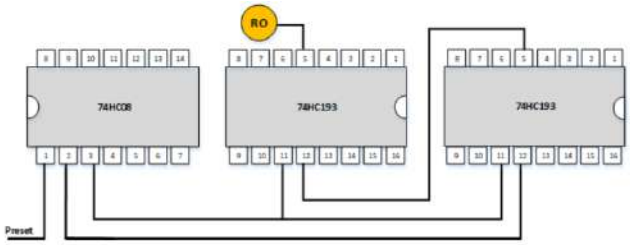

Fig. 12 Frequency divider using 74193

As this frequency divider divides by 200, after each 200 periods time of ring oscillator, carry out of MSB counter will be issued.

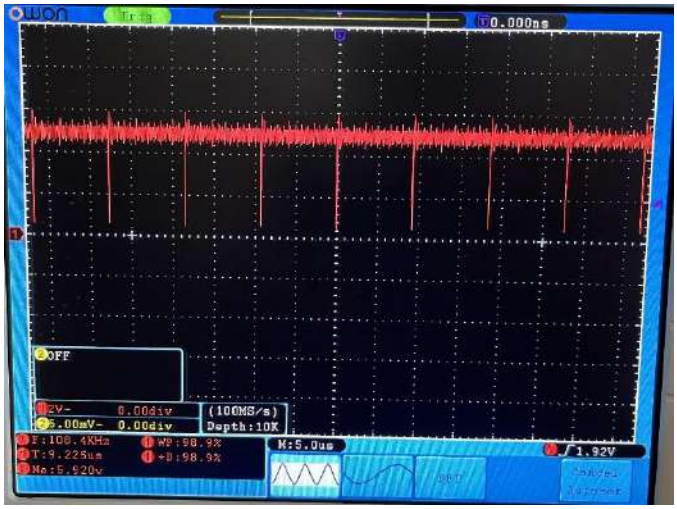

Fig. 13 Carry out of the MSB counter waveform

$$f_{clk} = 21.19\ \text{MHz}$$
$$f_{cy-out} = 108.4\ \text{KHz}$$
$$\rightarrow f_{cy-out} = \frac{f_{clk}}{200}$$

E. T Flip-Flop

The signal produced in part D was not a 50 percent duty cycle signal and now we are trying to make duty cycle 50 percent.

For this goal we use a T Flip-Flop which toggles at each time that input signal is issued.

So after two toggles the period will be completed, which means the period time of output signal is twice of the input one.

In this experiment we use a D Flip-Flop to create a T Flip-Flop just by wiring Qbar to the data (figure 14).

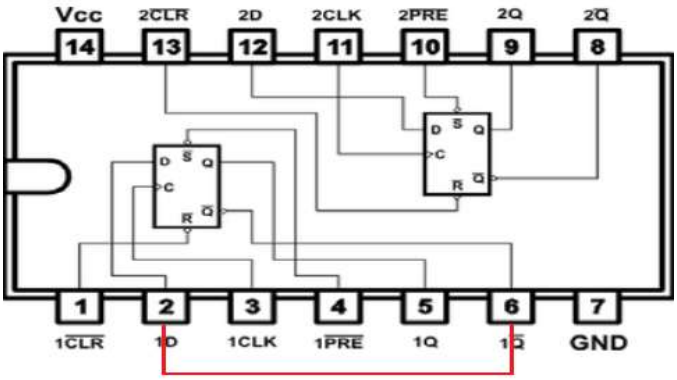

Fig. 14 D Flip-Flop connection

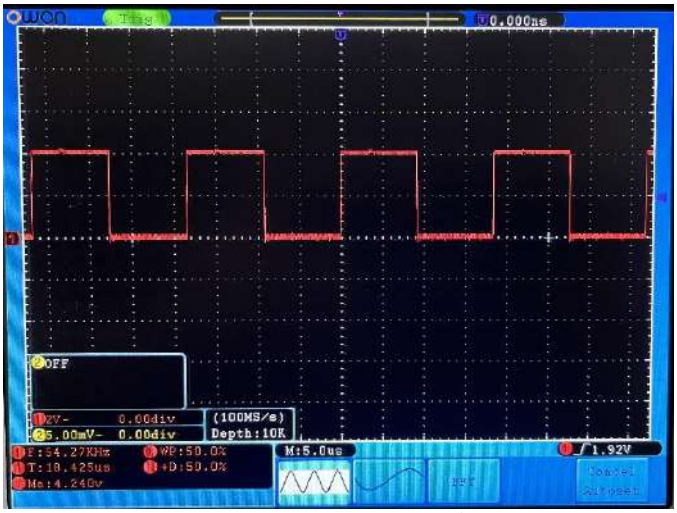

Fig. 15 T Flip-Flop output waveform

$$f_{TFF} = 54.27\ \text{KHz}$$

As we expected the frequency of T Flip-Flop output is half of frequency of the carry out in part D.
And the duty cycle is 50 percent.

III. Conclusions

A clock generator is an electronic oscillator that produces a clock signal for use in synchronizing a circuit's operation. There is variety of clock generator that some of them produces 50 percent duty cycle (e.g., ring oscillator and LM555 timer) and some types don't (e.g., Schmitt Trigger). Although duty cycle of these produced signals may differ, but can convert to 50 percent just by adding a TFF.

Another property of clock signals is periodicity that can convert to any value by make use of counters.

Acknowledgment

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REFERENCES

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