AVLSI SIMULATION REPORT

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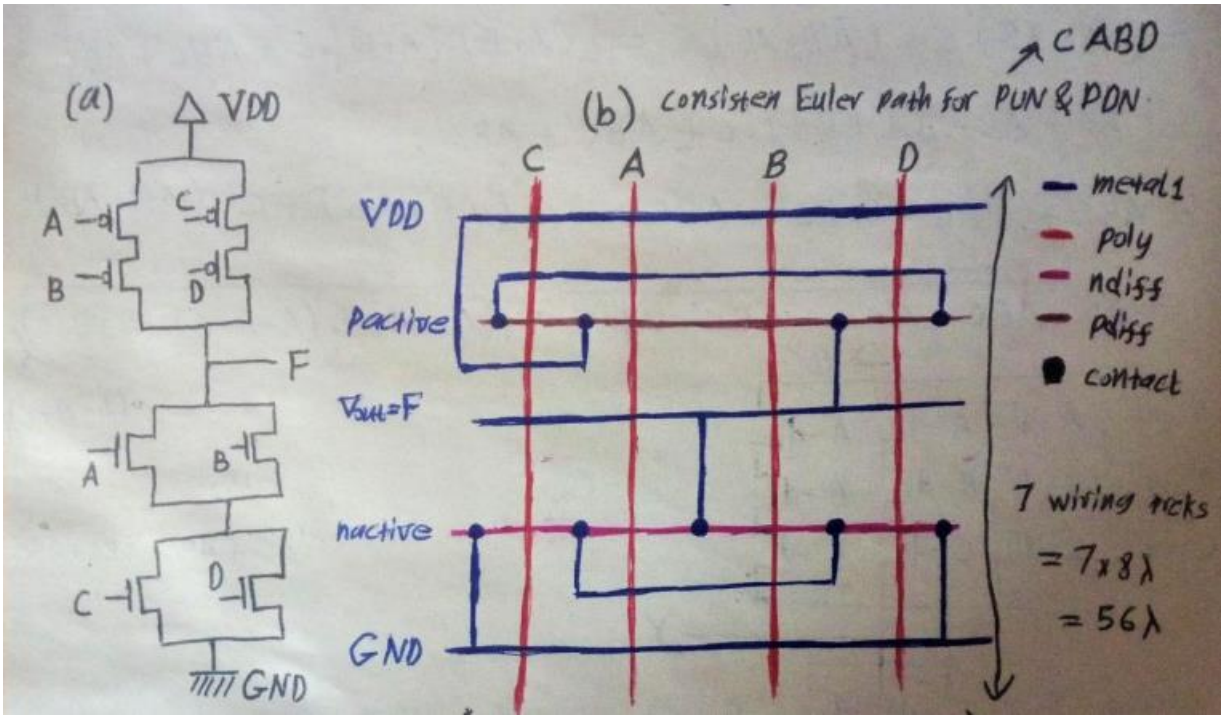
First Question:

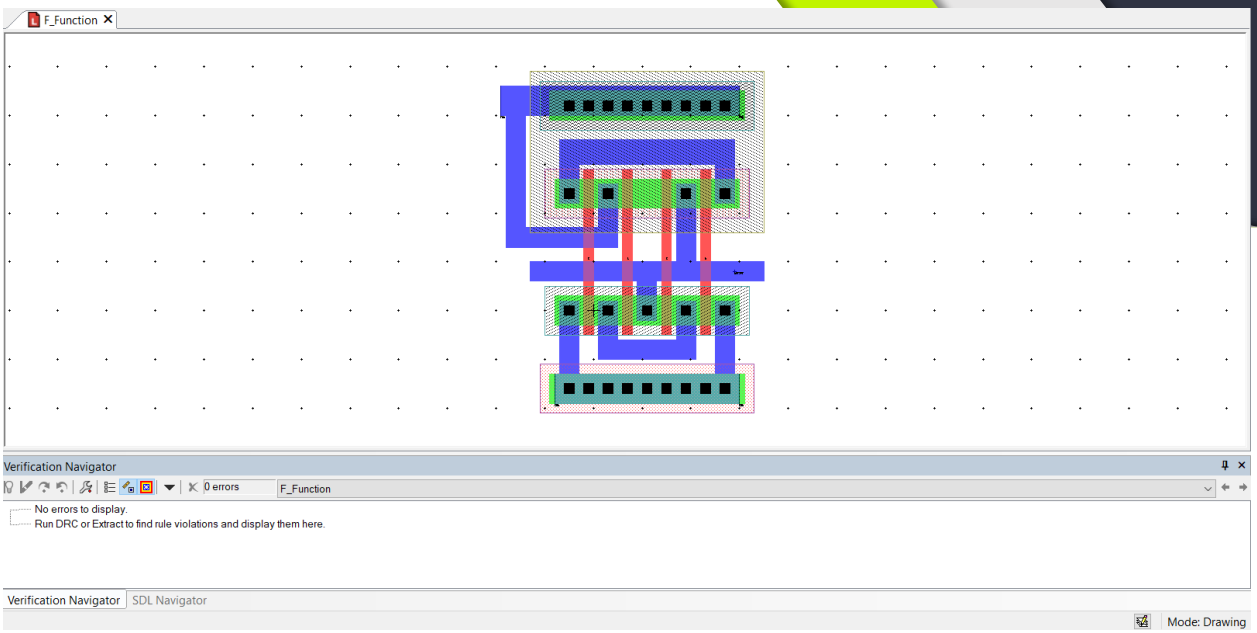
In the first question, we are required to draw the layout for the following function, do the design rule check (DRC), and show the results of its simulation.

$$F = \overline{(A+B)\cdot(C+D)}$$

Here is the implementation of the function in CMOS logic, and its associated stick diagram.



The following figure shows the layout of function F in the LEdit tool.



As we can see, the Design Rule Check (DRC) shows that there is no design problem. Our approach to drawing the layout was based on the lambda rules and we used 180nm technology to do this.

We only have transistors layout in the $.spc$ file generated by the EDA tool. Thus, to be able to see the waves of the simulation, we add the voltage sources and other necessary commands and then change the extension of the file from $.spc$ to $.sp$ to be able to simulate the file in the Hspice simulation tool. Here is how we've done it for a simple CMOS inverter gate (the file can be found in the example folder with the name $NOT.sp$).

In the above figure, the yellow line indicates the input and the red line shows the output. To assure the veracity of the layout and its consistency with our implementation, we show the name of the transistors, the necessary nodes, and the required voltage sources in the following picture (the corresponding file is $F\_Function.sp$ in the example folder).

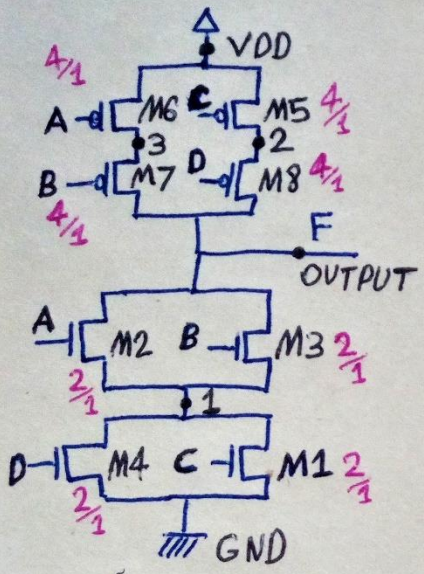
$F = \overline{(A+B).(C+D)}$

⇐ چهار منبع ولتاژ مستقل برای ورودی‌ها

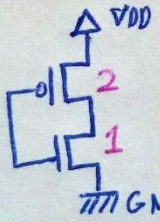
⇐ منابع پالسی (VA ، VB ، VC ، VD)

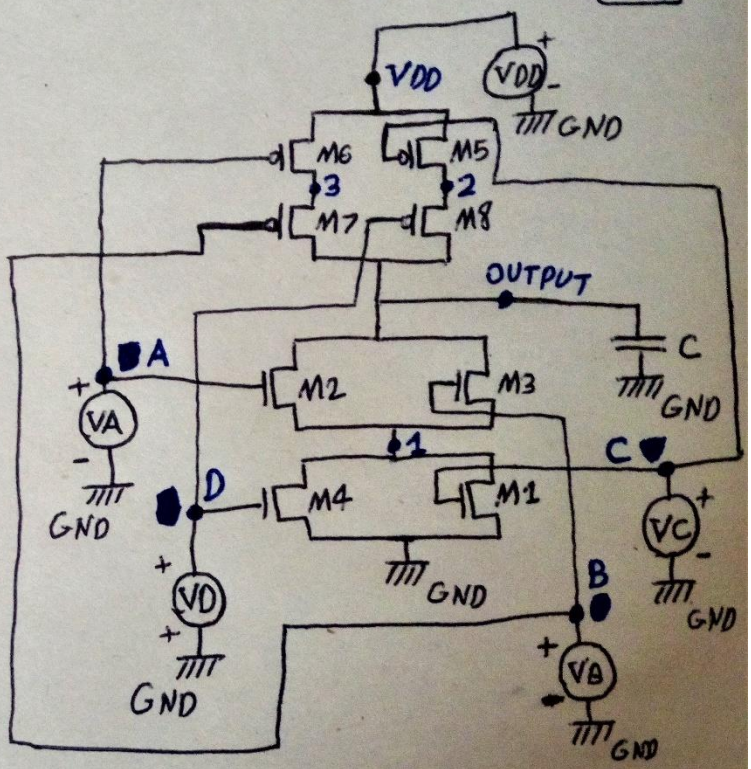
- sizing $(\frac{W}{L})$ → Dual: AB+CD

⇐ منبع ولتاژ برای منبع تغذیه با مقدار ثابت

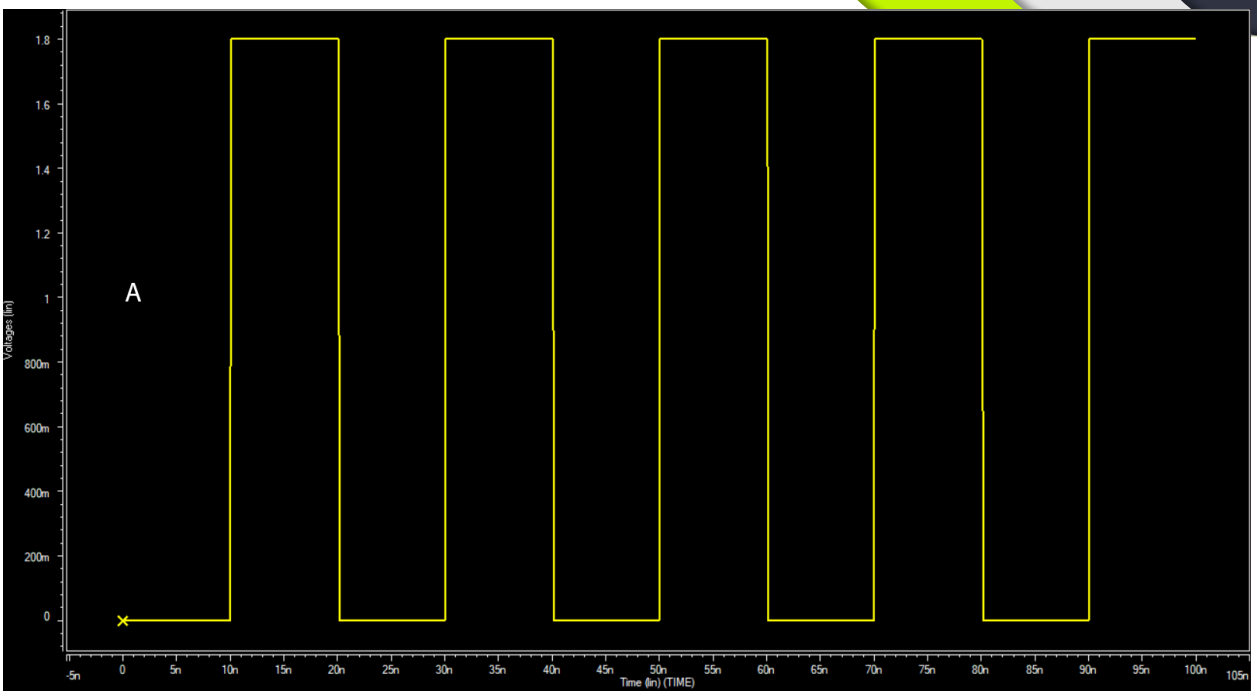


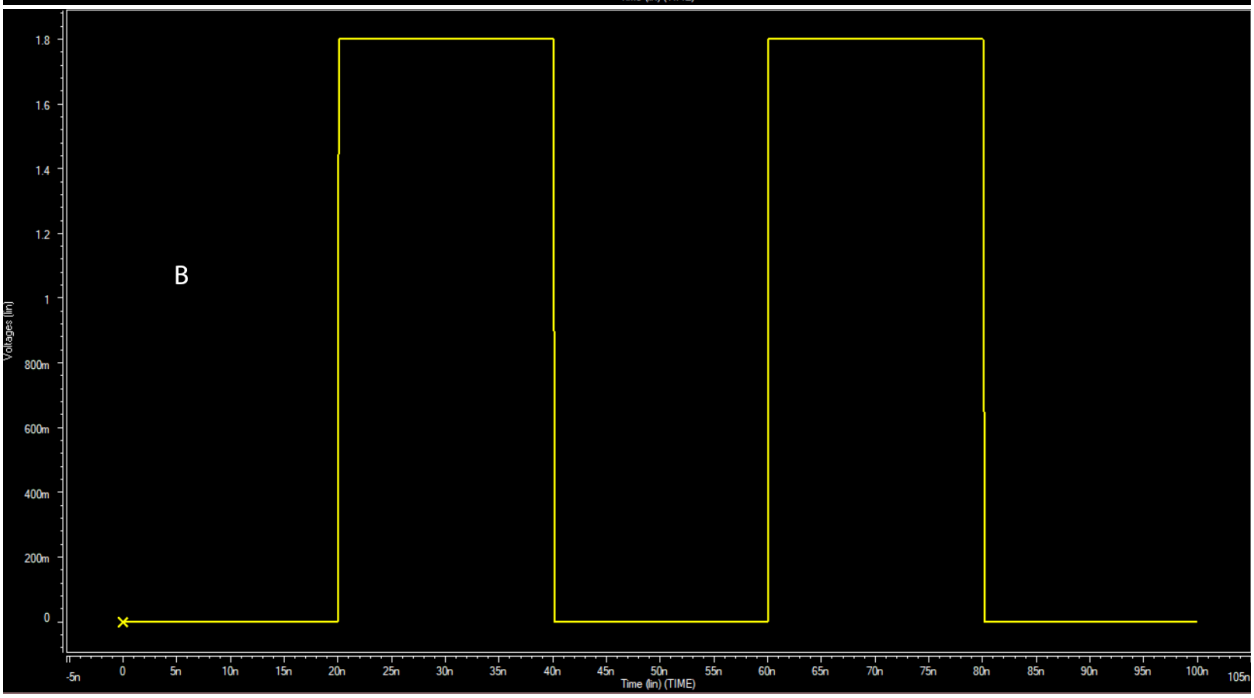
sizing based on CMOS unit inverter:

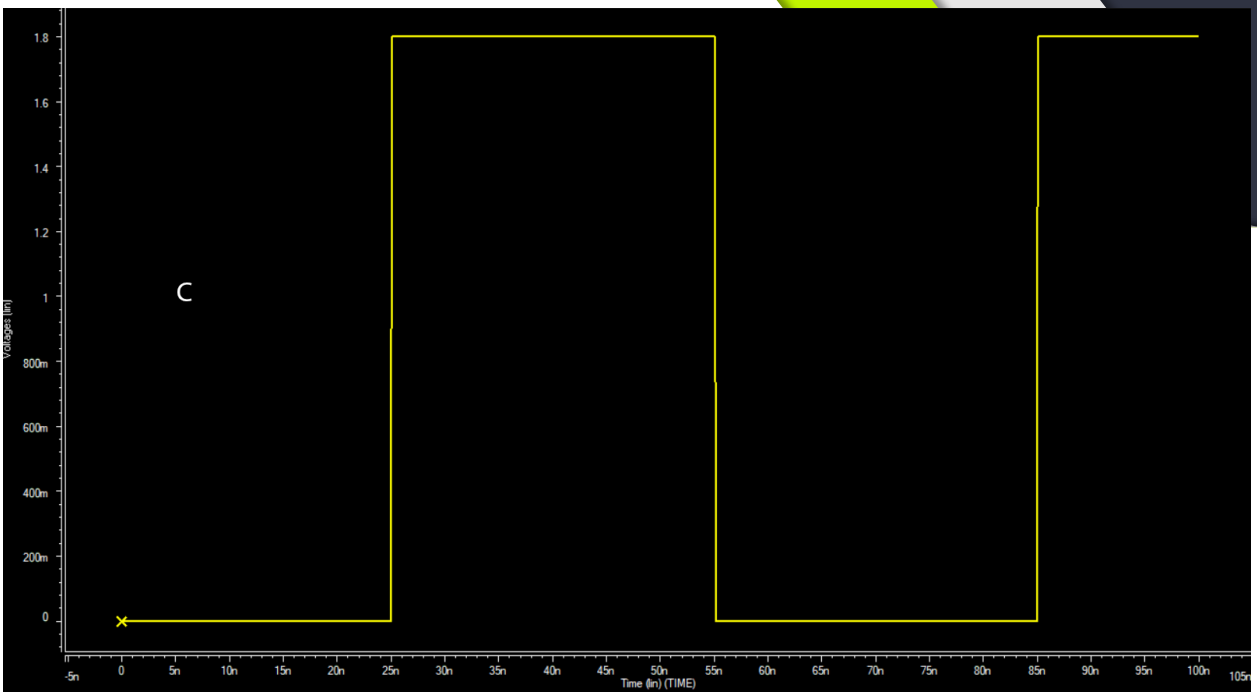


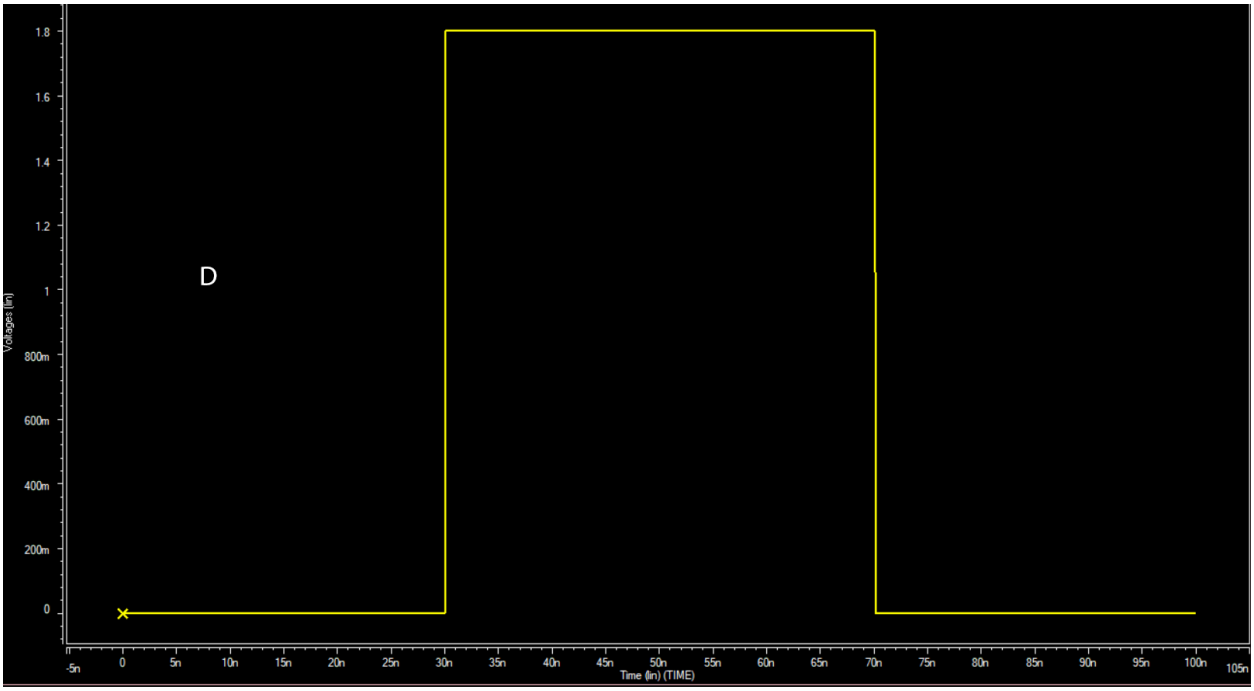


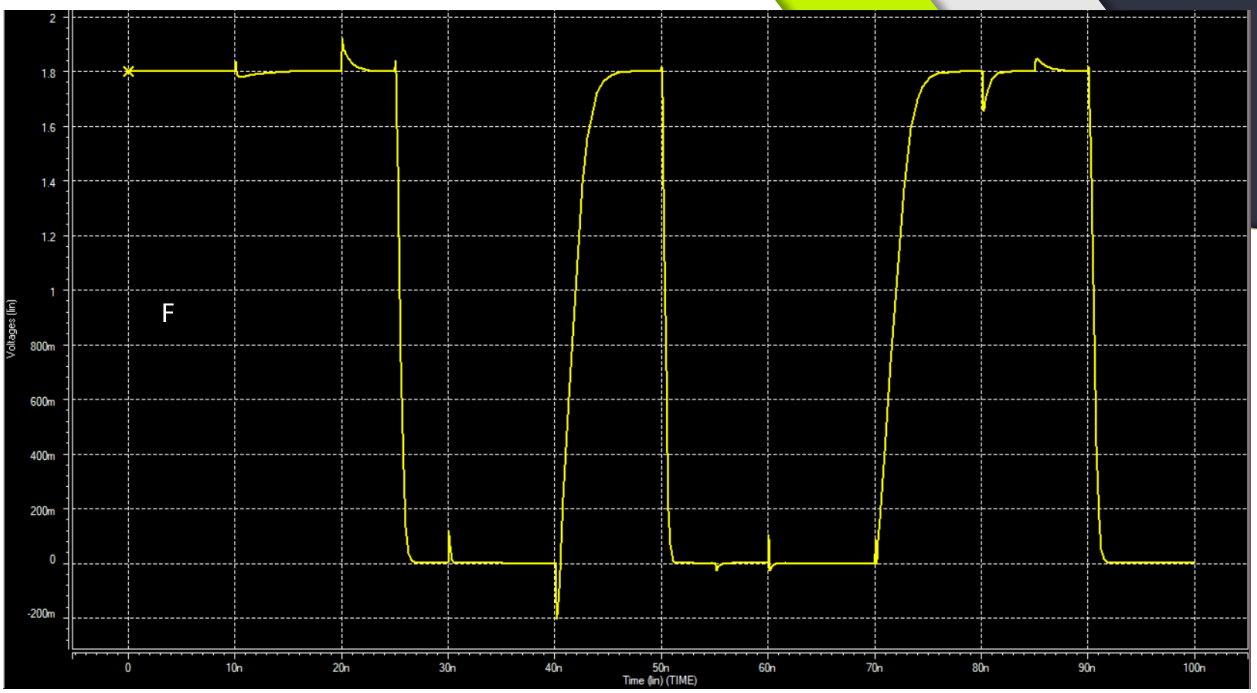
In the end, we have the simulation results for the F function in the following figures.






C
Voltages (in)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-5n
0
5n
10n
15n
20n
25n
30n
35n
40n
45n
50n
55n
60n
65n
70n
75n
80n
85n
90n
95n
100n
105n
Time (in) (TIME)


D
Voltages (in)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-5n
0
5n
10n
15n
20n
25n
30n
35n
40n
45n
50n
55n
60n
65n
70n
75n
80n
85n
90n
95n
100n
105n
Time (in) (TIME)

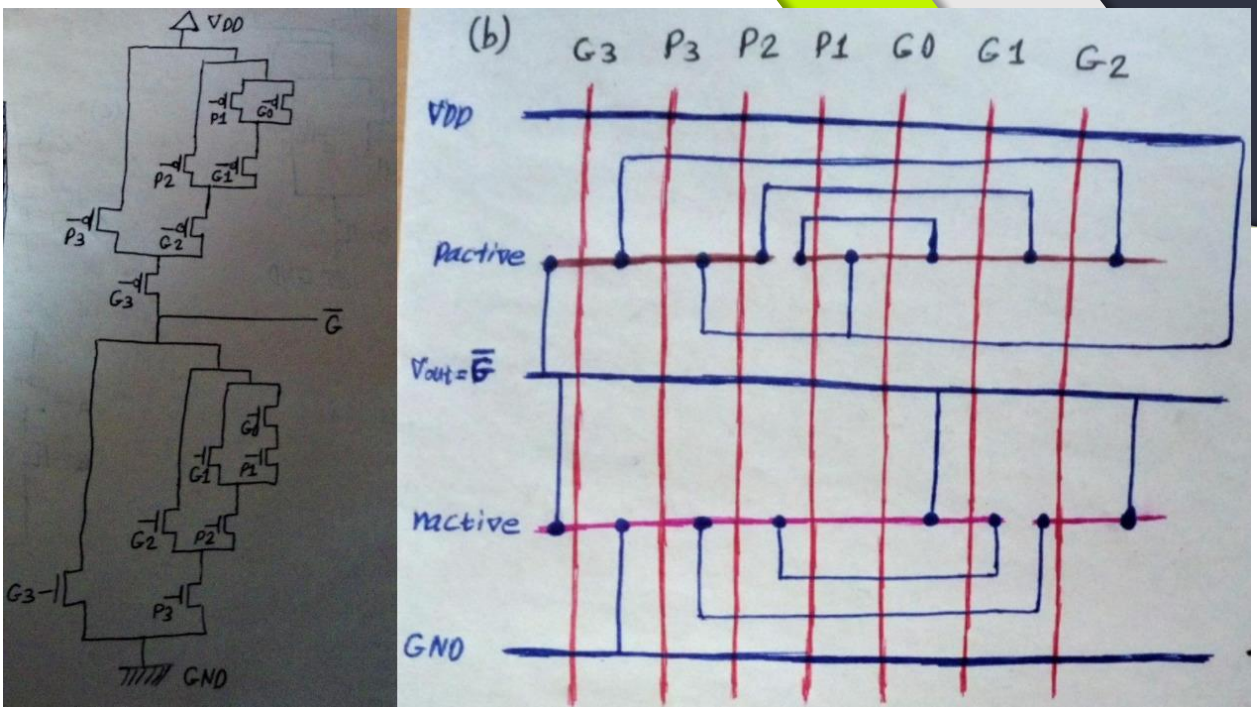


Second Question:

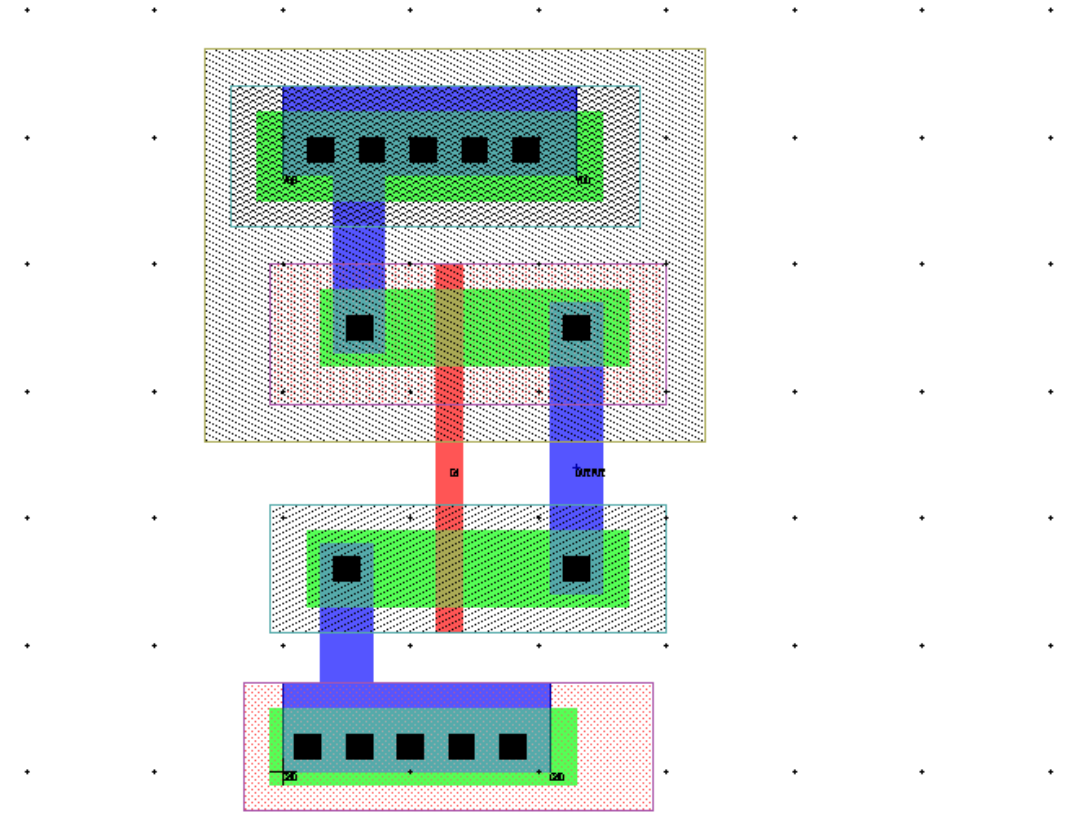
In this question, the function that needs to be implemented is as follows.

$$G = G_3 + P_3(G_2 + P_2(G_1 + P_1 G_0))$$

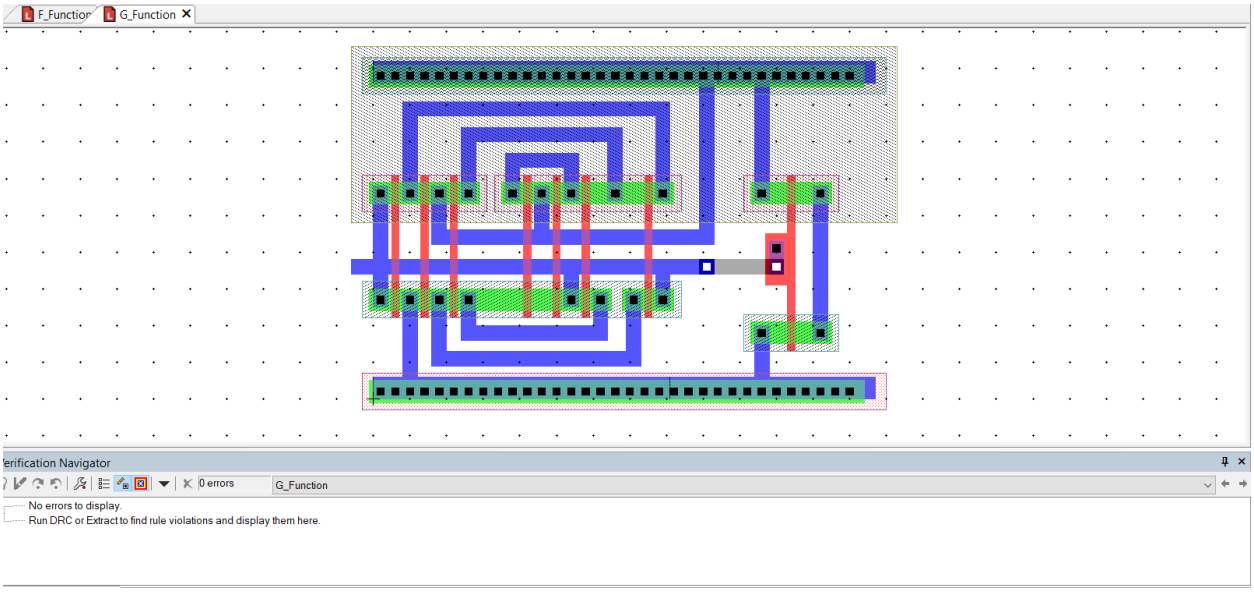
In the previous exercise, we have implemented the G' in CMOS logic and its corresponding stick diagram.



As we can see, the above logic implements G', thus rather than changing the whole implementation, we just add a CMOS inverter to the output of the function. Here is the sample layout for a CMOS inverter in the LEdit tool.

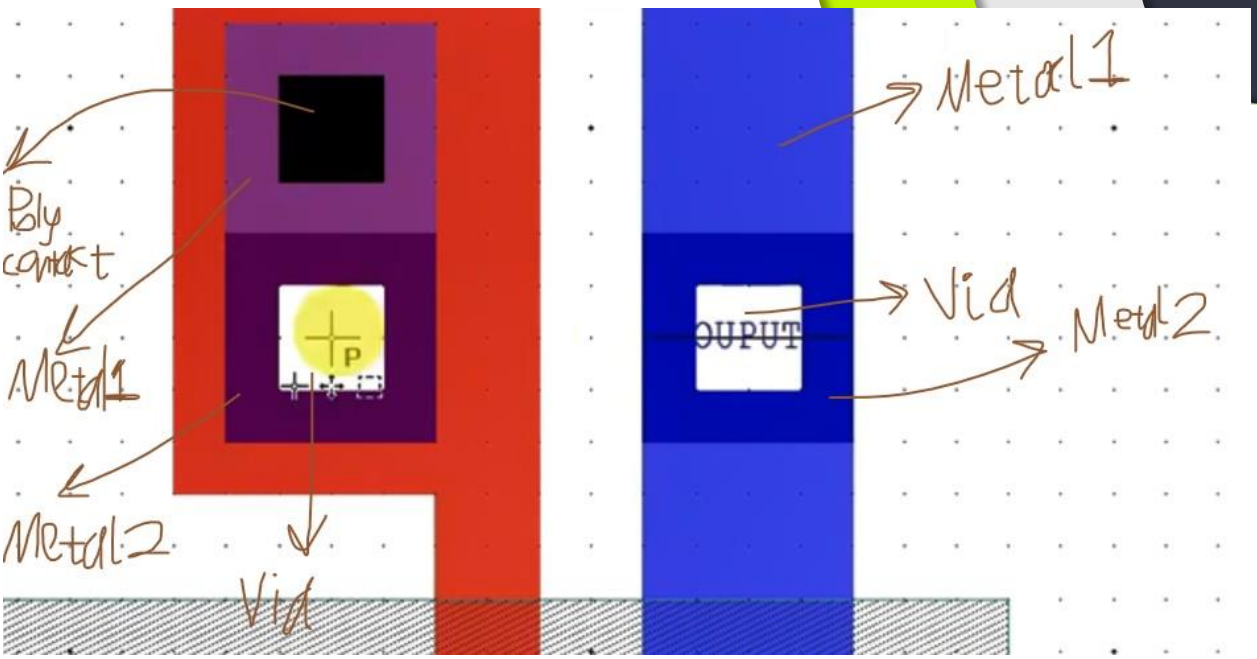


By simply adding this layout to the end of our G' function, we can get the G function. This is what we've done in the following layout.



The DRC is clean (shows no error). To connect the two gates, we use a via at the end of the G' gate and a poly contact on the poly of the inverter gate. We use the Metal1 on the poly, to put another via on

the input of the inverter gate, and therefore, we can easily connect the two gates by Metal2. Here is a picture of how this can be done.



To assure the veracity of the layout and its consistency with our implementation, we show the name of the transistors, the necessary nodes, and the required voltage sources in the following picture (the corresponding file is $G\_Function.sp$ in the example folder).

$$G = G_3 + P_3(G_2 + P_2(G_1 + P_1G_0))$$

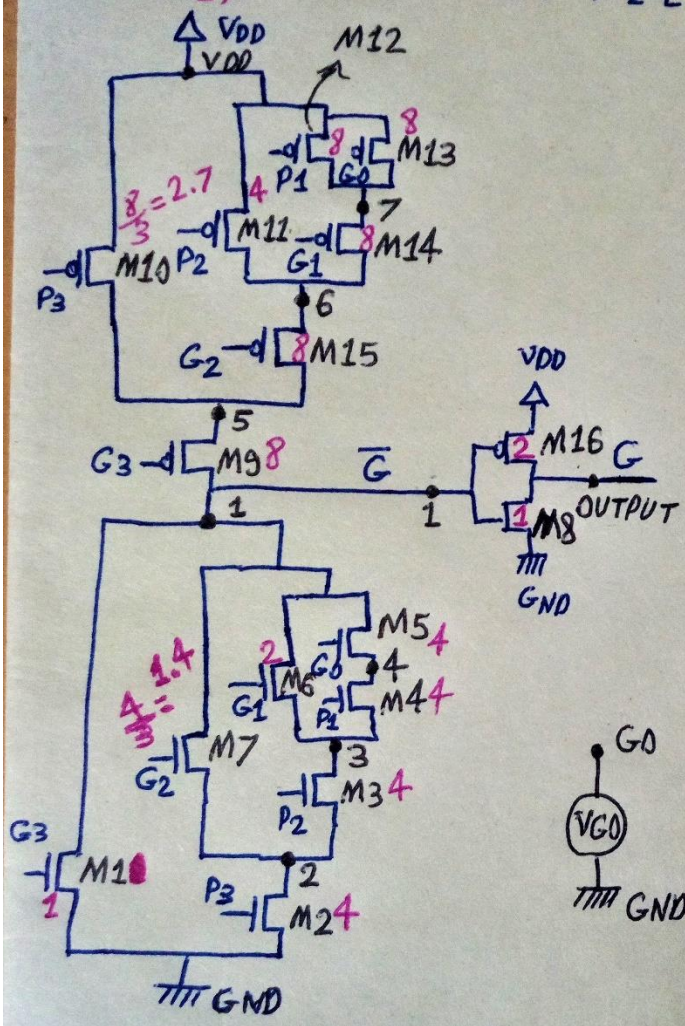
$$\overline{G} = \overline{G_3 + P_3(G_2 + P_2(G_1 + P_1G_0))}$$

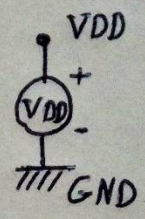
$$\text{Dual: } G_3 \cdot [P_3 + (G_2 \cdot [P_2 + (G_1 \cdot (P_1 + G_0))])]$$

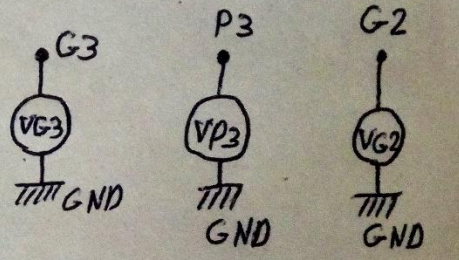
منابع ولتاژ پالسی:
VG3 ، VP3 ، VG2 ، VP2 ،
VG0 ، VP1 ، VG1

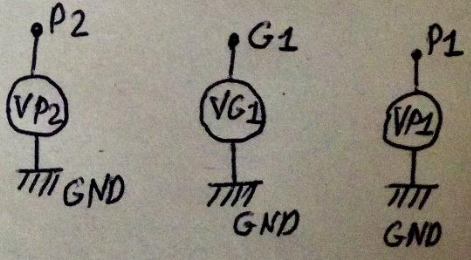
منبع ولتاژ DC ثابت برای منبع تغذیه:
VDD

• sizing($\frac{W}{L}$)

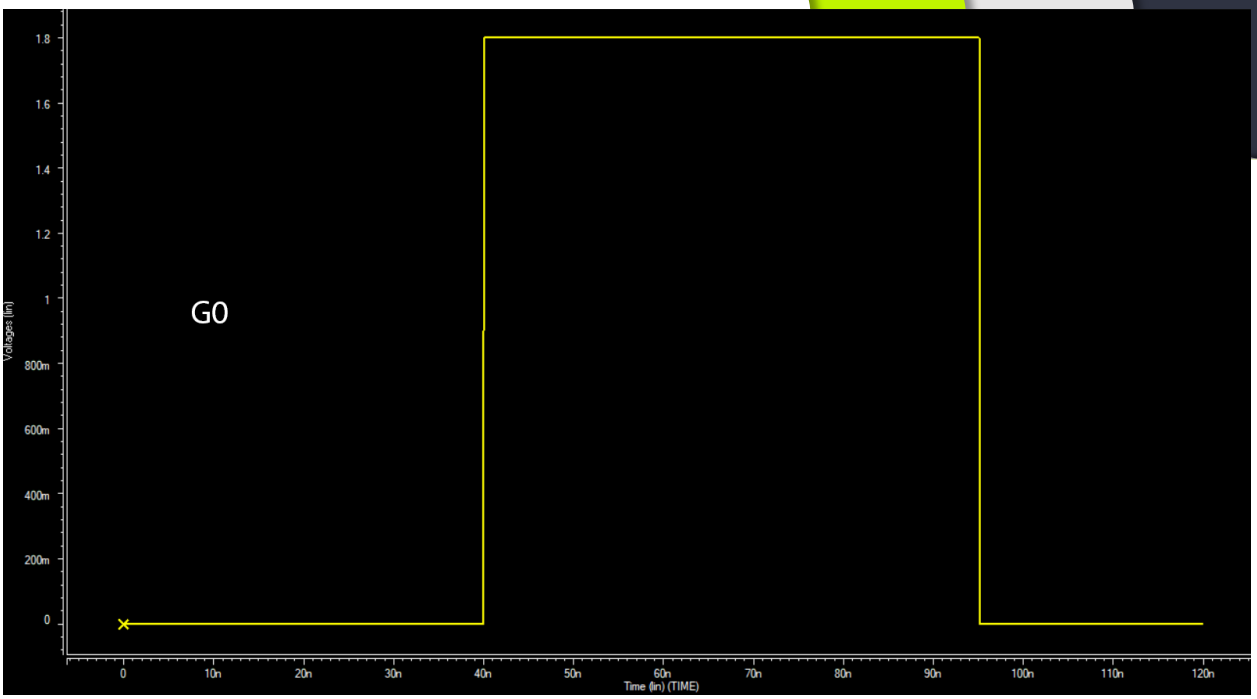


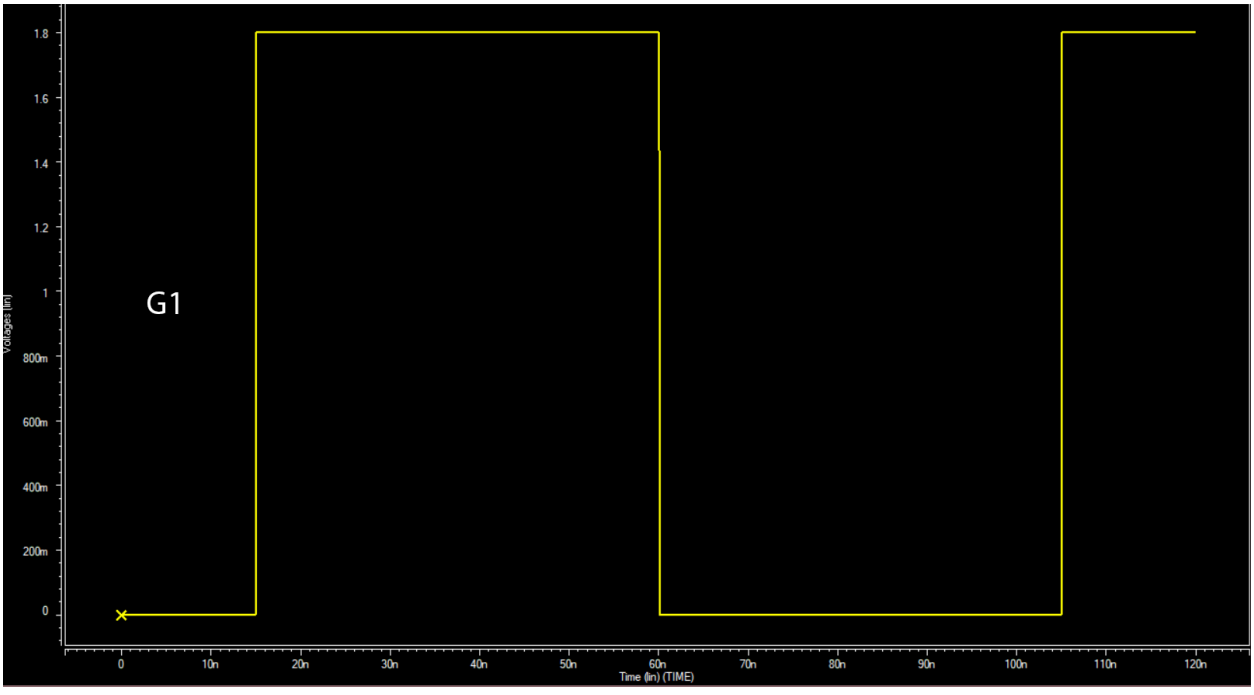


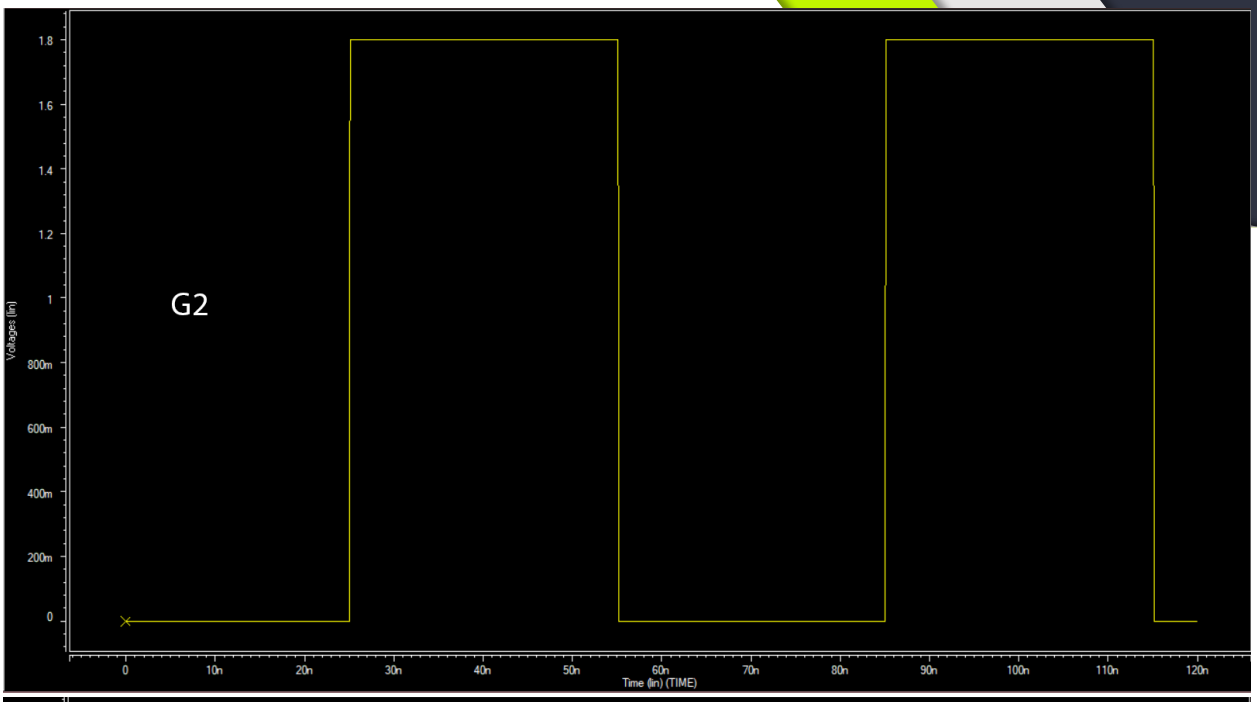


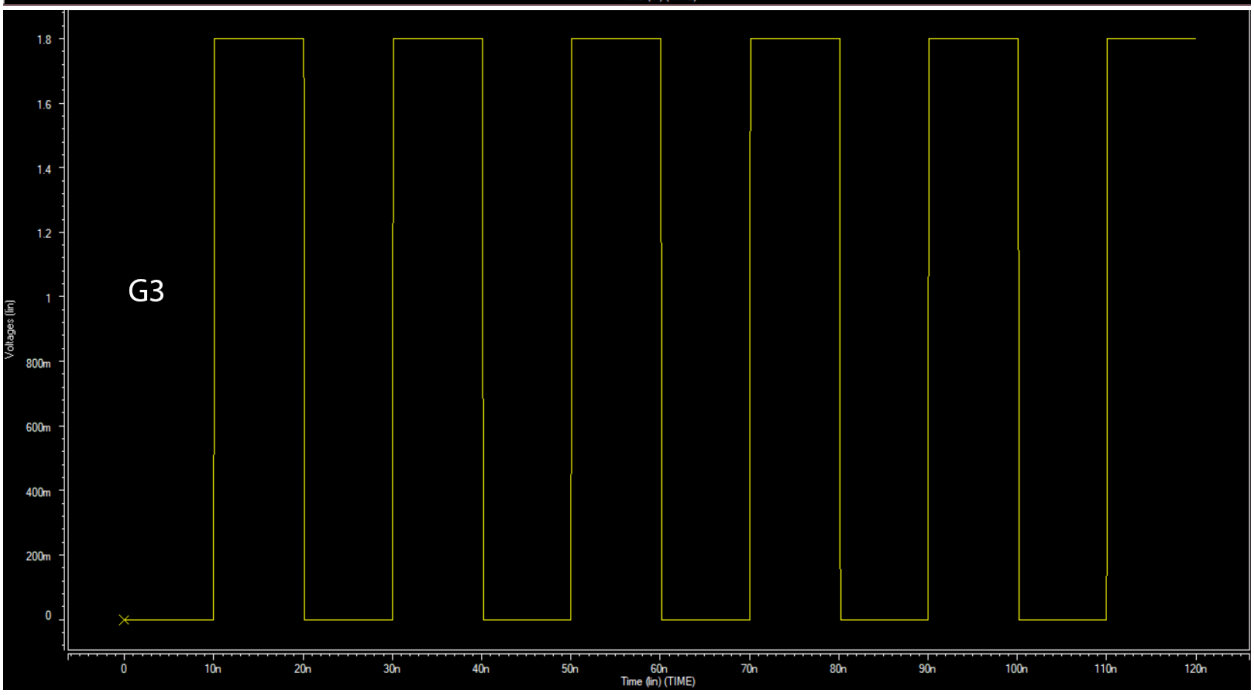


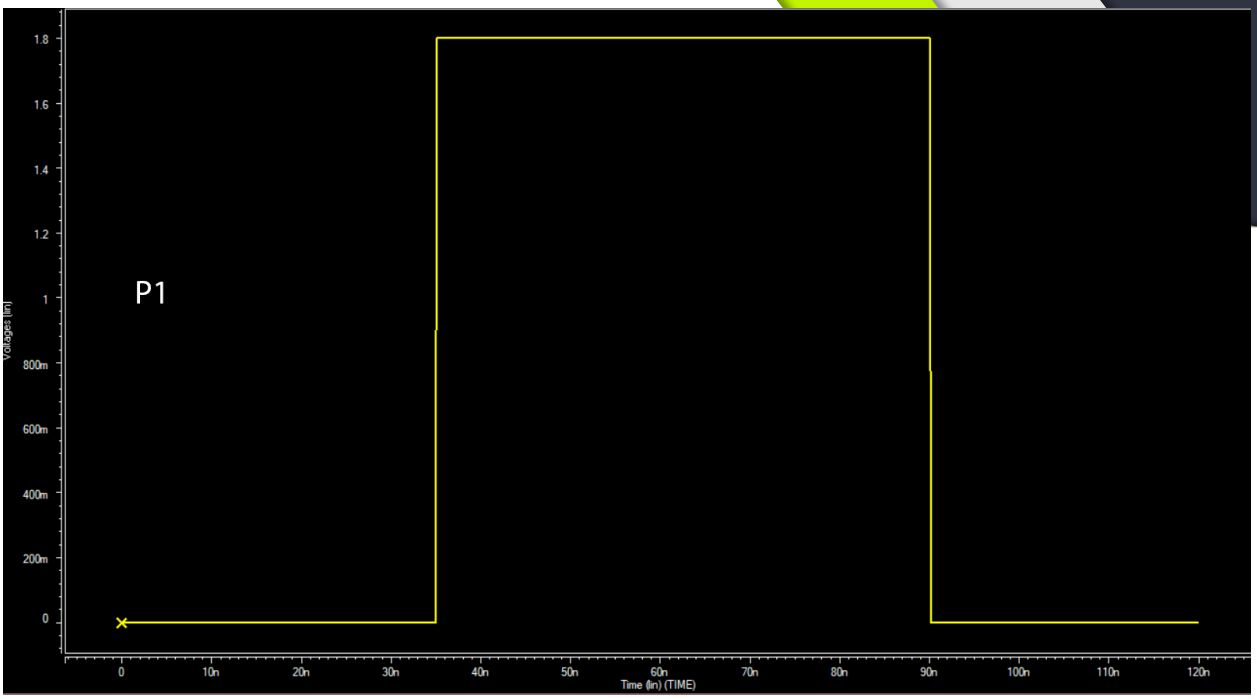
Finally, we have the simulation results as follows.

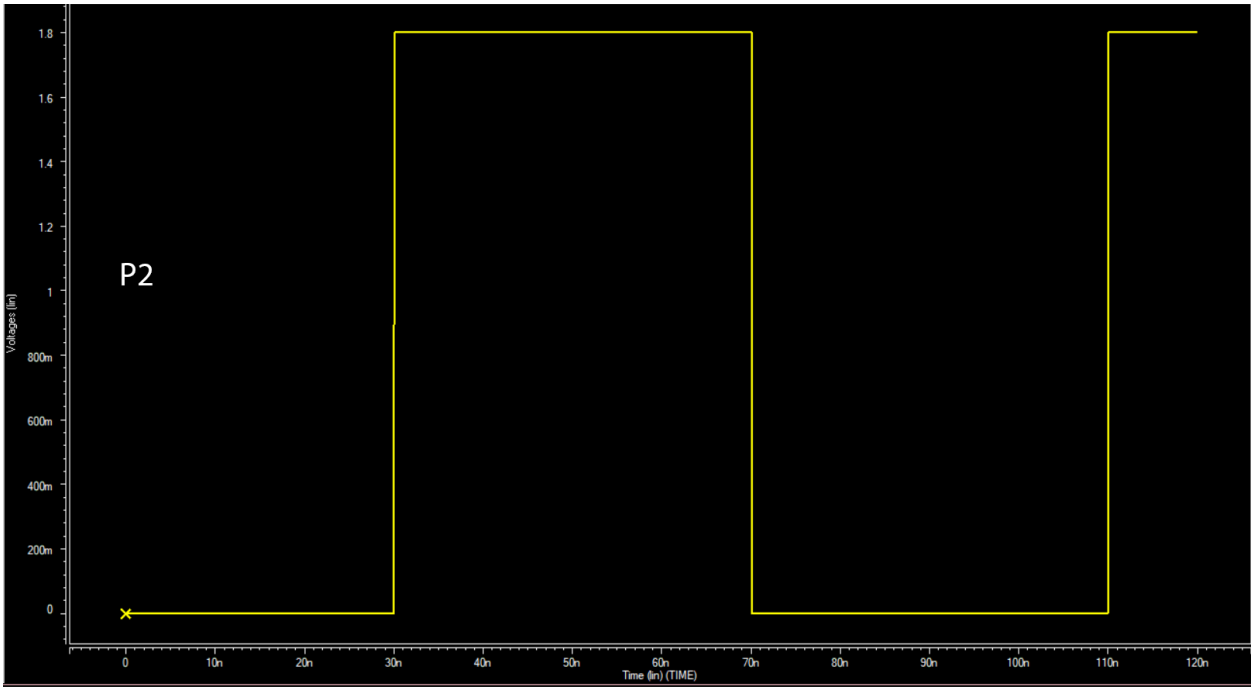


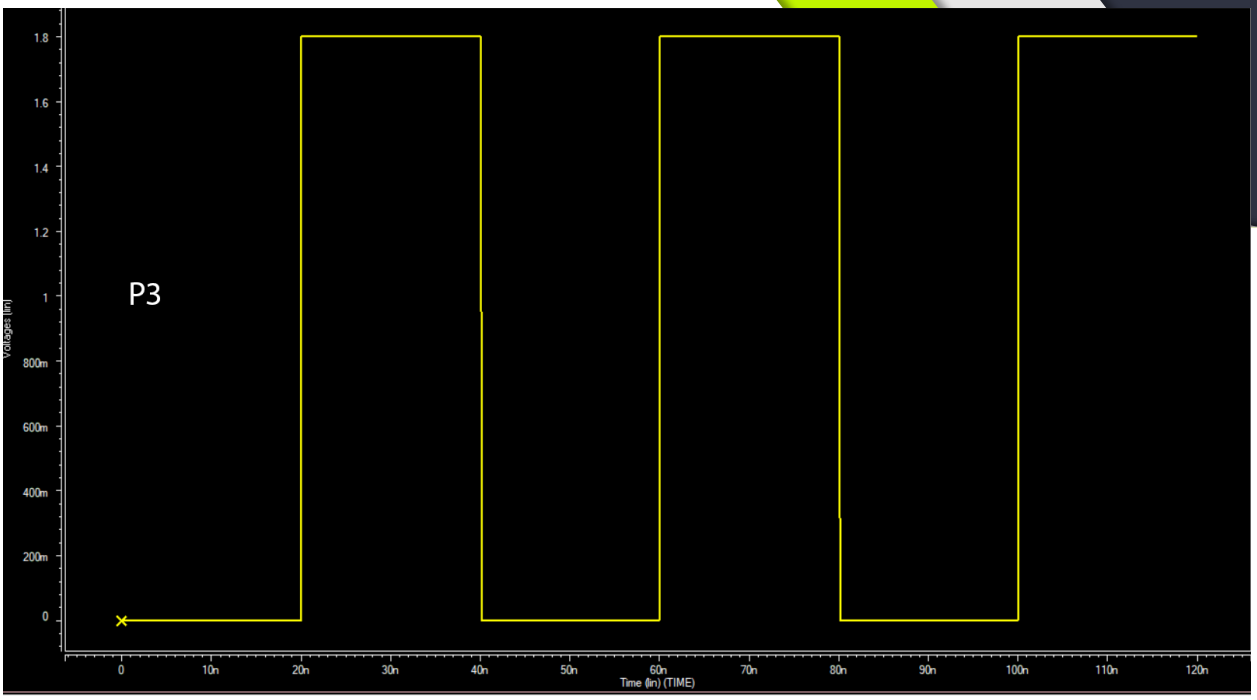


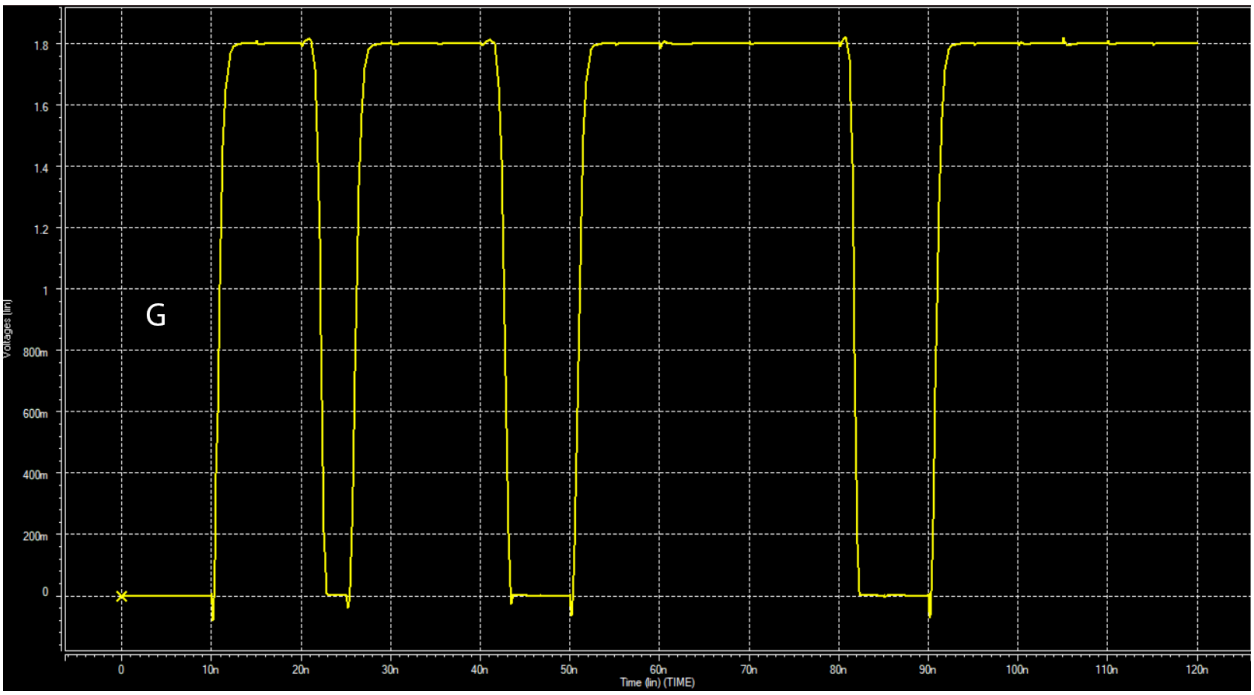

G2
Voltages (lin)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (lin) (TIME)


G3
Voltages (lin)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (lin) (TIME)


P1
Voltages [lin]
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (lin) (TIME)


P2
Voltages [lin]
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (lin) (TIME)


P3
Voltages (in)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (in) (TIME)


G
Voltages (in)
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
10n
20n
30n
40n
50n
60n
70n
80n
90n
100n
110n
120n
Time (in) (TIME)