UV-Sensitive Low Dark-Count PureB Single-Photon Avalanche Diode

Lin Qi, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon, *Senior Member, IEEE*, and Lis K. Nanver, *Member, IEEE*

***Abstract*— A single-photon avalanche diode with high sensitivity in the ultraviolet (UV) wavelength range has been fabricated on Si using pure boron chemical vapor deposition to create both a nanometer-thin anode junction and a robust light entrance window. The device shows high sensitivity at the wavelengths of 330–370 nm when operated in the Geiger mode and good selectivity for UV light without applying a capping filter. The dark count rates can be as low as 5 Hz at room temperature for an active area of 7 μm^2. An implicit guard ring, using an n-enhancement implantation in the central region of the diode, is applied instead of peripheral diffused p-type guard rings to achieve a high fill factor.**

***Index Terms*— Avalanche breakdown, boron, chemical vapor deposition (CVD), Geiger-mode avalanche photodiode, single-photon avalanche diode (SPAD), ultrashallow junctions, ultraviolet (UV).**

I. Introduction

WITH pure boron (PureB) technology, Si photodiode detectors have been fabricated and commercialized with outstanding performance for low-penetration-depth beams such as vacuum/extreme ultraviolet (UV) (VUV/EUV) light and low-energy electrons [1]. For planar diffused diodes, the spectral sensitivity to light signals is dependent on the attenuation length (penetration depth) of the light in silicon. As shown in Fig. 1, the penetration depth of UV light into silicon approaches values lower than 10 nm in the wavelength range of 100–350 nm. In particular, an attenuation length of ∼5 nm is reached at the deep ultraviolet wavelength of 193 nm, used for advanced lithography, and a minimum of ∼3 nm is reached at wavelengths around 280 nm. Therefore, to optimize the optical conversion efficiency, the photosensitive depletion region should be within this distance from the surface of the light-entrance window. The PureB layer is formed by a PureB chemical vapor deposition (CVD) in a manner that allows integration of bare 2-nm-thin boron layers as light-entrance windows [2]. At the same time, the PureB layer provides an effective p^+-doping of the semiconductor surface to form a nanometer-thin p^+n junction. The responsivity measured in the EUV/VUV range for one of the shallowest PureB junctions, achieved with a 2.5-nm-thick boron deposition, is included in Fig. 1. Even for the 200–300-nm spectral range, the responsivity is close to the theoretical value.

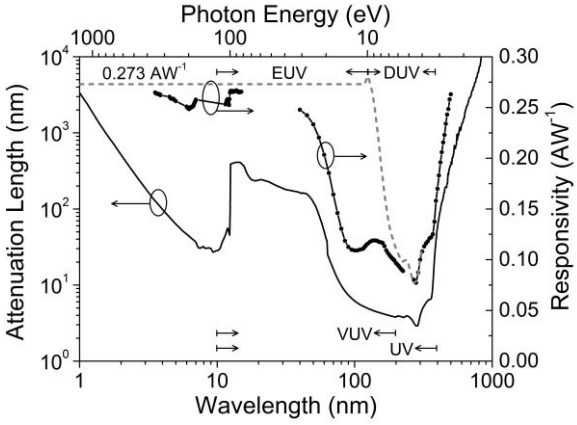


Fig. 1. Attenuation length in Si and responsivity as a function of radiation wavelength. The theoretical curve (gray dashed line) is for bare Si with 3-nm native oxide coverage and considers the reflectivity [13], [14]. Solid black curve follows the measured responsivity (dot symbols) of PureB photodiodes with a 2.5-nm-thick PureB-only light-entrance window [5].

The compatibility of the PureB process with CMOS technology is high, not least because a certain amount of post-PureB thermal treatments can be tolerated. With an *in situ* drive-in step, adjusted to the targeted light wavelengths and specific application, the junction depth can be increased and the sheet resistance be lowered. For anneal temperatures of up to 900 °C giving an increase of junction depth around 100 nm, it has been shown in [3] that when the PureB layer surface coverage is maintained, the responsivity remains high, even in the critical region around 200–300 nm. The experimental evidence indicates that two factors play a role. For the first, unlike implanted and annealed junctions, the junction is damage-free and the ample supply of boron for drive-in prevents roll-off of the resulting doping profile at the surface [4], [5]. Second, due to the diffused doping gradient and the effective p^+ layer at the PureB/Si interface, an electric field to separate the photogenerated charge carriers is created and it is particularly high at the surface where recombination of electrons will otherwise degrade the performance [3].

The PureB layer itself can be integrated as a robust and almost nonabsorbing light-entrance window. This layer is

Manuscript received April 28, 2014; revised June 25, 2014 and July 31, 2014; accepted August 20, 2014. Date of current version October 20, 2014. This work was supported by the Huygens Scholarship Programme, Ministry of Education, Culture and Science, The Netherlands. The review of this paper was arranged by J. Huang.

L. Qi, K. R. C. Mok, E. Charbon, and L. K. Nanver are with the Delft University of Technology, Delft CT 2628, The Netherlands (e-mail: l.qi@tudelft.nl; c.mokkairine@tudelft.nl; e.charbon@tudelft.nl; l.k.nanver@tudelft.nl).

M. Aminian is with École Polytechnique Fédérale de Lausanne, Lausanne CH-1015, Switzerland (e-mail: mahdi.aminian@epfl.ch).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2351576

conductive, does not oxidize, and does therefore not charge during irradiation [6]. Moreover, it is chemically resistant in many situations and it can be used to form a barrier against silicidation/spiking of metals like Al [7]. Capping layers such as Al and SiO_2 can be removed selectively from the PureB layer using HF wet etching. With all these properties, it has been possible to integrate detectors that have surpassed the performance of other existing technologies on points such as internal/external quantum efficiency, dark current, and responsivity degradation [8]–[10].

The PureB technology has mainly been used for large area photodiodes operating at low reverse bias voltages. The work in this paper has been performed to extend the capabilities of PureB photodiodes, so that highly sensitive imaging arrays with micrometer-sized pixels can be fabricated [11]. High-sensitivity and exceptional timing accuracy are achieved by creating single-photon avalanche diodes (SPADs) that in recent years have received renewed interest due to their wide applicability and versatility [12]. In our case, a p-n junction is fabricated in PureB technology and operated as an avalanche photodiode in Geiger-mode by biasing it well above breakdown. To prevent edge breakdown, a guard ring is generally implemented around the active area that often is a circle of 5–50 μm in diameter. The requirement of small device dimensions complicates the processing with respect to the fabrication of the guard rings and the opening of the light-entrance windows. As a solution, an implicit guard ring is implemented using an n-enhancement implantation in the central region of the diode. The lack of a deep peripherally diffused p-type guard ring also demanded the development of more critical processing for contacting of the p^+ anode as well as the removal of the anode metallization on the light-entrance window in a fill-factor effective manner.

II. Device Fabrication

To achieve high sensitivity despite the small size, a design for operation in Geiger-mode is realized. A schematic cross section of the process flow for fabricating PureB SPADs is shown in Fig. 2. Starting with p-type (100) 2–5-Ωcm Si substrates, a 1.0-μm-thick n^- epitaxial layer is grown on an n^+ buried layer which is contacted by implanted n^+ plugs. An n-enrichment is created by implanting phosphorus through a 30-nm thermal silicon oxide, first at 40 keV to a dose of 1×10^{12} cm^{-2} and then at 300 keV to a dose of 5×10^{12} cm^{-2}. This defines the active region of the detector. A 300-nm low-pressure CVD tetra-ethoxy silane is then deposited and the implants are annealed at 950 °C for 20 min in argon gas. The anode contact windows are plasma etched to the Si with soft landing and native oxide is removed by dip etching in HF 0.55% followed by Marangoni drying. The PureB layer is then deposited from diborane in an ASM Epsilon 2000 CVD reactor. The deposition time and temperature, 6 min at 700 °C, have been calibrated to give a 2.5-nm PureB deposition on bare Si wafers. Due to global and local loading effects, it is expected that the PureB thickness in the anode windows can be about a nanometer thicker [15], [16]. A drive-in for 1 min at 850 °C is performed

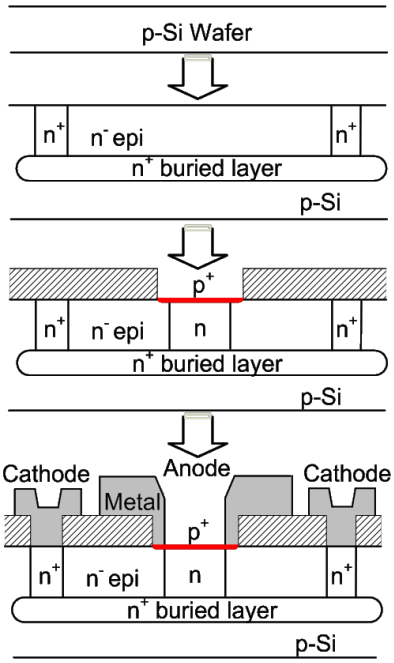


Fig. 2. Schematic process flow for the fabrication of a PureB SPAD.

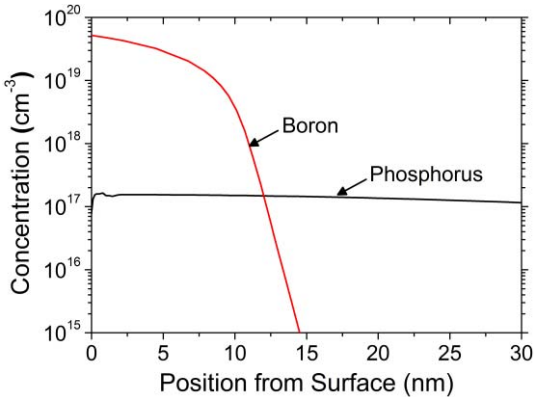


Fig. 3. Simulated doping profiles in the Si as a result of a 6-min PureB deposition at 700 °C and drive-in for 1 min at 850 °C as well as phosphorus implantations at 40 keV to a dose of 10^{12} cm^{-2} and at 300 keV to a dose of 5×10^{12} cm^{-2}. The n-type epidoping is 10^{15} cm^{-3}.

to form a p^+ anode region with a junction depth around 12 nm as extracted from the TCAD-simulated doping profiles shown in Fig. 3. Due to the reaction with the Si, a small thinning of the PureB layer may occur in this thermal step, but the overall results suggest the effect is insignificant for this thermal budget. Right after the PureB deposition, 675-nm pure Al is sputtered at 50 °C, directly onto the PureB layer. Then, the cathode contact windows are opened by plasma etching. Another 675-nm Al layer containing 1% Si layer is deposited, also at 50 °C. After metal patterning, the light-entrance windows are opened and aligned to the n-enrichment region, first by plasma etching until 100–200-nm Al is left and then removing the remaining Al by wet etching in HF 0.55% for 3–5 min. At last, a 400 °C alloy step in forming gas is performed to improve the contact resistivity of the Al to the PureB/Si surfaces.

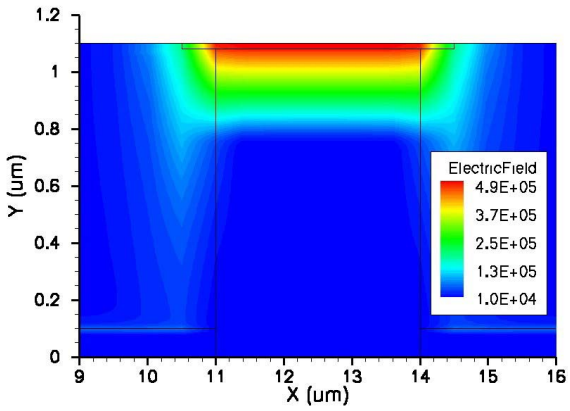


Fig. 4. Simulated electric field distribution in Si when the maximum electric field reaches approximately 5×10^5 V/cm, i.e., the maximum electric field for a one-sided abrupt junction with a background doping of 1×10^{17} cm^{-3} in Si. The device is created by following the process flow of the fabricated devices [18].

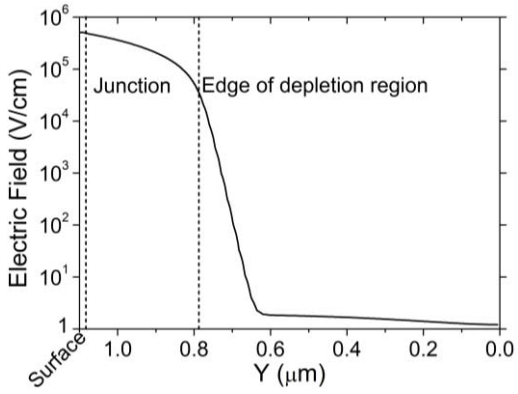


Fig. 5. Simulated electric field profile in the Y (vertical) direction along the center of the device ($X = 12.5$ μm), where the maximum electric field reaches approximately 5×10^5 V/cm. Around $X = 0$, the electric field in the p$^+$-region should drop to zero, but the simulation grid is too course to reproduce this.

In this paper, the anode windows of the fabricated and characterized device have a diameter of 4 μm and the light-entrance windows are only 1 μm smaller in diameter, i.e., the edge to edge distance from the anode perimeter to light-entrance window/n-enrichment region is only 0.5 μm. To validate the efficiency of the implicit guard ring, a device simulation in TCAD is performed. A 4-μm wide p$^+$ anode region is defined at the Si surface with a constant doping concentration of 10^{19} cm^{-3} and a junction depth of 12 nm. The bulk Si is n-type with a doping concentration of 10^{15} cm^{-3}. The n-enrichment region is right underneath the p$^+$ region but 1 μm smaller in width, and it is n-type with a constant doping concentration of 10^{17} cm^{-3}. The n-enrichment region extends into the Si and is connected to the n$^+$ buried layer. The cathodes are also connected to the buried layer through an n$^+$ plug. As found in [17], for one-sided abrupt junctions with a background doping of 10^{17} cm^{-3}, the maximum electric field at breakdown in Si is approximately 5×10^5 V/cm. From the simulated electric field distribution graph in Fig. 4, we can see that the maximum electric field lies at the junction between the p$^+$ region and the n-enrichment region. In the implicit guard ring region, the electric field is reduced to less than half of the maximum electric field value, thus preventing premature edge breakdown. Due to the ultrashallow nature of the junction, the electric field in the p$^+$ region is close to the maximum value and it stays quite high through the depletion region to fall off abruptly in the n-enrichment region beyond the depletion region, as shown in Fig. 5. Thus, the avalanche multiplication region reaches to the surface and overlaps the light absorption region, which should make the sensitivity to (V)UV light optimal.

In contrast to what is seen in Fig. 5, the electric field in the p$^+$-region should drop to zero toward the surface. However, the grid has a minimum mesh dimension of 2 nm, which is too coarse to reproduce such abrupt behavior over a junction depth of less than 10 nm. In any case, the high electric field at the junction will dominate the movement of the charge carriers and the electrons generated by the incident light in this region can be easily swept into the depletion region and trigger an avalanche.

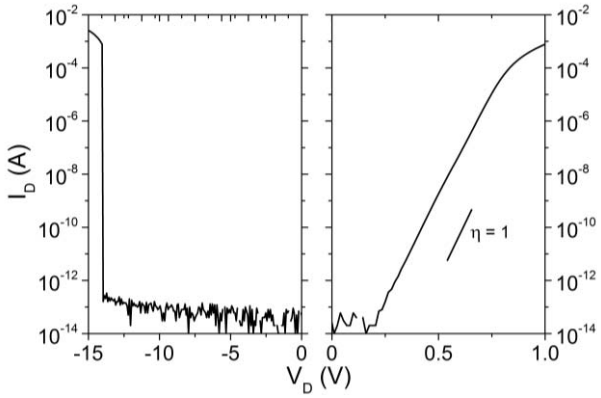


Fig. 6. I–V characteristics of a PureB SPAD with a diameter of 4 μm.

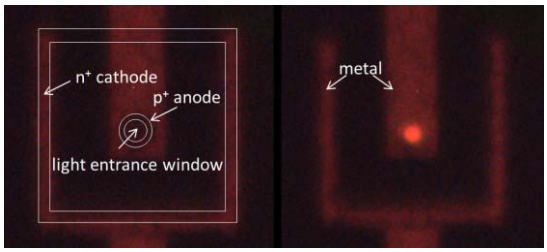


Fig. 7. Light emission test (right image) for a PureB SPAD operating at a bias voltage of −14 V. The device at zero bias (left image): the n$^+$ cathode plug, the p$^+$ anode region, and the light entrance window are indicated.

III. Optical/Electrical Characterization

In Fig. 6, the current–voltage (I–V) characteristics are shown for the fabricated PureB SPAD. The diode ideality factor is almost 1 indicating that there are very few defects in the depletion region over the junction created by the PureB deposition. A very sharp and abrupt breakdown is observed and the V_{BD} is found to be around −14 V. The dark current before breakdown is below the detection limit and it increases to hundreds of microamperes past breakdown. A light emission test is shown in Fig. 7, which confirms that the onset of the breakdown is within the n-enrichment region and not at the anode edge.

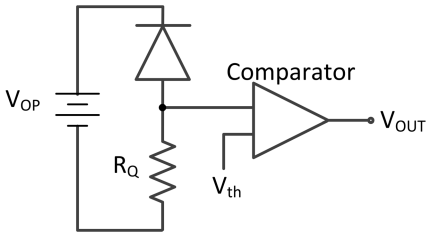


Fig. 8. Electronic circuit schematic of a SPAD with passive quenching and passive recharge.

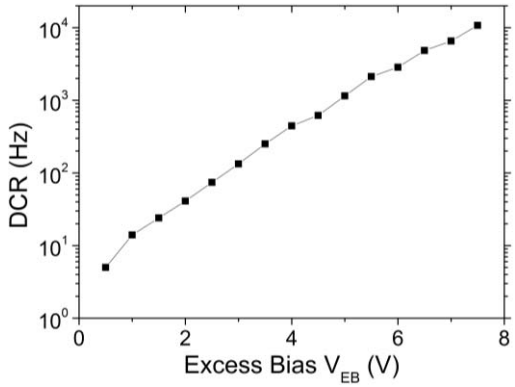


Fig. 9. DCR measurements of a PureB Si photodiode with a diameter of 4 μm as a function of excess bias voltage V_{EB} at room temperature.

The basic measurement circuit is shown in Fig. 8 for operating the SPAD in Geiger-mode with passive quenching and passive recharge via a ballast resistor R_Q chosen to be 100 kΩ in this case. The device is biased above breakdown (V_{BD}) by a voltage known as the excess bias (V_{EB}) so that the operating voltage is $|V_{OP}| = |V_{BD}| + V_{EB}$. With the resulting high electrical field, an incoming photon can trigger an avalanche event. With the passive quenching mechanism, the high avalanche current must pass through R_Q, creating a voltage drop over the resistor that brings the voltage across the diode below breakdown. Thus, the avalanching is stopped, the diode biasing is restored to the initial values, and a new incoming photon can be detected. This cycle takes an average time known as the dead time. The avalanche pulses are sensed using a comparator with an appropriate threshold voltage Vth, thus converting the Geiger pulses into digital signals for photon counting.

Pulses can also be generated by nonphoton-induced carriers, such as those originating from diffusion from the neutral regions, Schottky–Read–Hall thermal direct or trap-assisted generation, direct or trap-assisted band-to-band tunneling, or by the release of trapped carriers [19]. All these mechanisms result in dark counts, characterized by a parameter called dark count rate (DCR). The DCR is measured at room temperature as a function of excess bias voltage V_{EB} and plotted in Fig. 9. The values are extremely low, down to 5 Hz when $V_{EB} = 0.5$ V, i.e., the noise level at room temperature is very low and could be further reduced by cooling the device. In Fig. 10, a corresponding oscilloscope image taken with $V_{EB} = 4.5$ V displays a DCR of ~600 Hz.

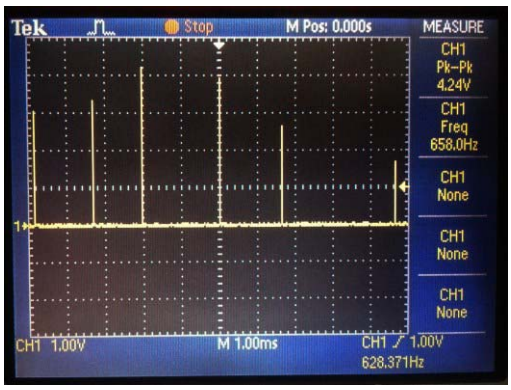


Fig. 10. Oscilloscope image of Geiger pulses in the absence of light at $V_{EB} = 4.5$ V. The sampling rate was subsampled to show more avalanche pulses, which is why the amplitude of the pulses is not always exactly V_{EB}.

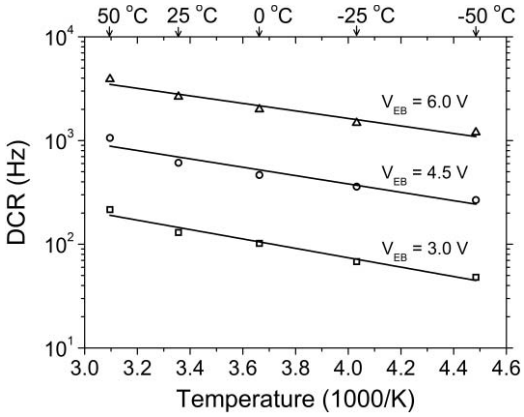


Fig. 11. Measured DCR (symbols) with exponential fit (lines) as a function of temperature for an excess bias of 3.0, 4.5, or 6.0 V.

The measured DCR as a function of temperature is shown in Fig. 11 for three different excess bias voltages. All curves show a good exponential relationship to the ambient temperature, suggesting that the DCR is dominated by the thermally generated carriers rather than field-assisted generation. The latter occurring without the help of a phonon has, compared to the thermal generation, a relatively small impact [20], and it is hardly reduced by lowering the temperature. This sets a limit to the reduction of the DCR that can be obtained by cooling the device [21].

The spectral sensitivity is evaluated by illuminating the device at different wavelengths with a light-source spot that is much larger than the diode area. The measured photocurrent I_D is compared with the photocurrent I_{REF} measured on a reference photodiode with an area larger than the spot size and for which the quantum efficiency is known for all wavelengths of interest. The ratio I_D/I_{REF} is plotted as a function of wavelength in Fig. 12 for the operating voltages of -10 V (below breakdown), -14 V (breakdown), and -20 V (Geiger-mode). The sensitivity shows a peak at 330 nm in Geiger-mode, where the optical gain is a 1000 times higher than when operating below breakdown and a 100 times higher than when operating right at the breakdown voltage.

The photon detection probability (PDP) is defined as the percentage of incoming (external) photons that trigger an

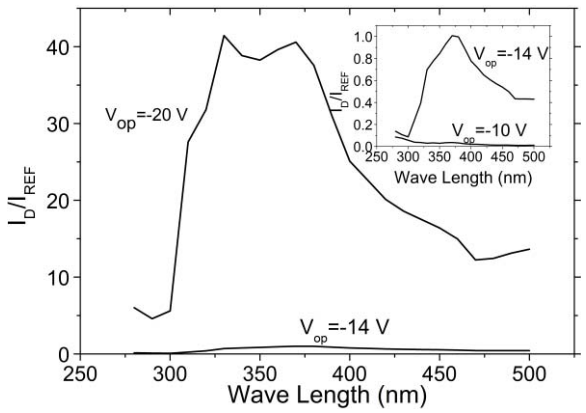


Fig. 12. I_D/I_{REF} of a PureB SPAD with a diameter of 4 μm in the UV spectrum for various operating voltages V_{OP}.

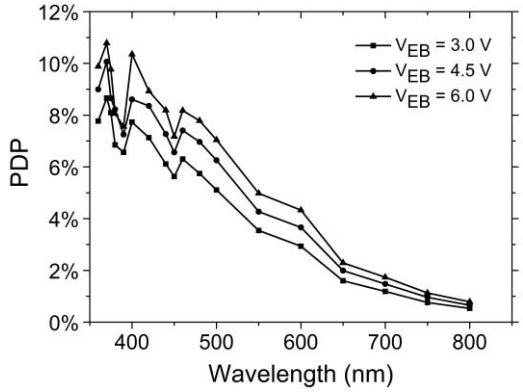


Fig. 13. PDP for a PureB SPAD with diameter of 4 μm as a function of wavelength with excess bias $V_{\mathrm{EB}} = 3.0$, 4.5, or 6.0 V.

avalanche pulse at the incident light wavelength

$$\mathrm{PDP}(\lambda) = \frac{A - \mathrm{DCR}}{P} \tag{1}$$

where A is the avalanche pulse rate sensed by the SPAD in hertz and P is the incoming photon flux, given in hertz at wavelength λ, with which the active region of the SPAD is illuminated. The P is calculated by taking the current reading of the reference diode of the monocromator and, from a knowledge of all the areas involved, estimating the actual flux arriving on the active area of the SPAD. The P is controlled so that A is between 20 and 80 kHz to prevent pile-up. The dead time, the time when the SPAD is unable to detect photons including both quenching and recharge time, is around 6 μs as can be measured with high excess bias voltage above about 6 V. Here, we use passive quenching and recharge with an external circuit, but if suitable active circuitry is employed, the dead time can be very significantly reduced.

The PDP at different excess bias voltages as a function of incident light wavelength is plotted in Fig. 13. It increases with increasing excess bias since more photons can be collected and counted at higher electric fields. The results display a good selectivity to UV light, with a maximum PDP of around 11% at 370 nm when the excess bias voltage is 6.0 V. For this device, the peak of the PDP is in the UV spectrum, unlike the SPADs

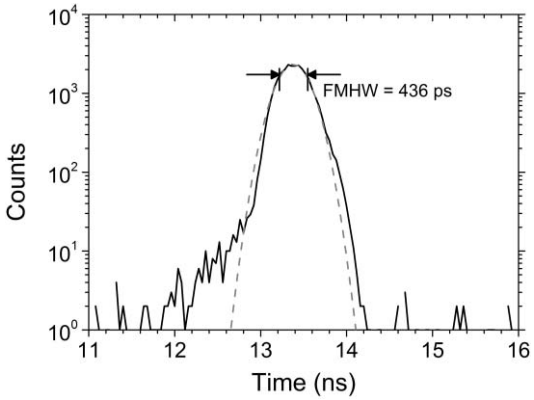


Fig. 14. Measured jitter performance (black solid line) and Gaussian fitting (gray dashed line) of a PureB SPAD with a diameter of 4 μm when operated in Geiger mode with an excess bias $V_{\mathrm{EB}} = 4.5$ V.

normally produced in CMOS technology, for which the peak is in the visible light spectrum [22]. This is in accordance with the fact that the p^+-n junction here only has a junction depth of $\sim$12 nm and although the PureB layer itself is absorbing, it is only about 2–3-nm thick. For UV light, as shown in Fig. 1, the penetration depth in Si is less than 100 nm and the photon-generated carriers (electron-hole pairs) outside the depletion region can easily reach the multiplication region and cause an avalanche. However, for visible light, the penetration depth in Si increases with the wavelength and becomes hundreds of nanometers already at a wavelength of 500 nm. It is then more probable that the generated carriers will be swept into or be isolated in the substrate, therefore recombining outside the multiplication region where no avalanche can be triggered.

Due to the limitations of the measurement setup, the PDP measurement could only be performed down to 360 nm. Nonetheless, from the high VUV responsivity of PureB photodiodes in general, the PDP at shorter wavelengths such as 330 nm is expected to be significantly higher than 11%.

Timing jitter is the time distribution of counts taken from the moment of photon absorption to the triggered avalanche process. The jitter performance is measured with the SPAD exposed to a 40-MHz pulsed laser source at a wavelength of 405 nm, and the light is attenuated to the single-photon level to prevent pile-up, as described in [23]. The timing response is plotted in Fig. 14 for a PureB SPAD with an excess bias voltage of 4.5 V. The measurement is obtained using the embedded time discriminator of a LeCroy WaveMaster 8600A. The measured full-width at half-maximum (FWHM) jitter is 436 ps. The jitter performance shows a good Gaussian distribution with no diffusion tail, suggesting that most of the avalanching occurred within the multiplication region and secondary avalanche processes are essentially absent. The timing jitter can be further reduced by increasing the excess bias voltage, as shown in Fig. 15. This results in higher electric field so that the avalanche process can be triggered faster.

During an avalanche process, the carriers released from deep level traps can cause secondary avalanche processes known as afterpulsing [24]. In this paper, as shown in Fig. 16, the afterpulsing probability is measured at room temperature using

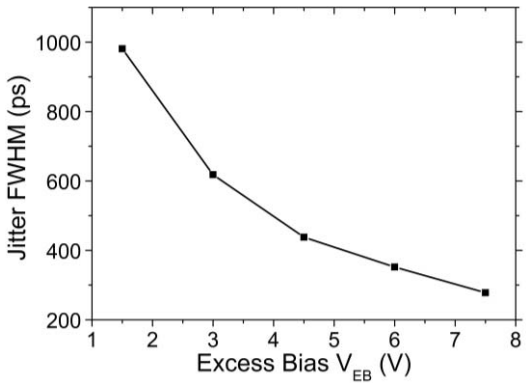


Fig. 15. Timing jitter (FWHM) of a PureB SPAD with a diameter of 4 μm when operated in Geiger Mode as a function of excess bias.

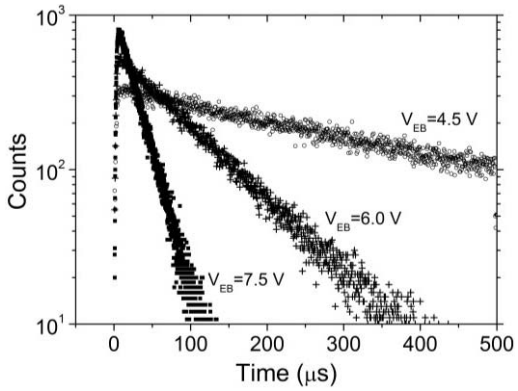


Fig. 16. Afterpulsing distributions of a PureB SPAD with a diameter of 4 μm when operated in Geiger mode with excess bias V_{EB} of 4.5, 6.0, and 7.5 V.

the interavalanche time method [25] at three different excess bias voltages, namely 4.5, 6.0, and 7.5 V. In all three cases, the afterpulsing distributions show very good exponential behavior and the afterpulsing probability is less than 1%, which is also an indication that the trap density in the device is very low and proof that a high quality device has been achieved.

IV. Conclusion

Highly UV-sensitive SPADs have successfully been fabricated using PureB technology to create a nanometer-thin light-entrance window and a near-ideal p^+n junction diode. The use of an implanted n-enrichment layer in the central region of small circular anodes sets the breakdown voltage. When the diode is reverse biased, the leakage current is very low below breakdown ($\ll 10^{-12}$ A) and increases abruptly by five decades in less than 100 mV upon breakdown at -14 V. The device exhibits a very low frequency of dark counts with a 5-Hz DCR at room temperature for a low excess bias of 0.5 V, more than 11% PDP in the UV region at 370 nm, and an afterpulsing probability less than 1%. The device performance can be further improved by increasing the excess bias voltage and in the studied range up to $V_{EB} = 6$ V, there is no clear indication that the noise level in the form of timing jitter and afterpulsing performance, increases despite the increasing DCR. The absence of peripheral diffused p-type guard rings is beneficial for the fill factor. In this nonoptimized version, the diameter of the p^+-anode region is only 1 μm larger than the n-enrichment region, promoting a high fill factor for individual detectors and detector arrays.

Acknowledgment

The authors would like to thank the DIMES-ICP Group for their help with processing and measurements.

References

[1] L. K. Nanver *et al.*, "Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices," *ECS Trans.*, vol. 49, no. 1, pp. 25–33, 2012.

[2] L. Shi, S. Nihtianov, X. Sha, L. K. Nanver, A. Gottwald, and F. Scholze, "Electrical and optical performance investigation of Si-based ultrashallow-junction p^+-n VUV/EUV photodiodes," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 5, pp. 1268–1277, May 2012.

[3] L. K. Nanver *et al.*, "Robust UV/VUV/EUV PureB photodiode detector technology with high CMOS compatibility," *J. Sel. Topics Quantum Electron.*, vol. 20, no. 6, pp. 1–11, Nov./Dec. 2014.

[4] F. Sarubbi, L. K. Nanver, and T. L. M. Scholtes, "High effective Gummel number of CVD boron layers in ultrashallow p^+n diode configurations," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1269–1278, Jun. 2010.

[5] L. Shi, S. Nihtianov, L. Haspeslagh, F. Scholze, A. Gottwald, and L. K. Nanver, "Surface-charge-collection-enhanced high-sensitivity high-stability silicon photodiodes for DUV and VUV spectral ranges," *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 2888–2894, Nov. 2012.

[6] L. Shi, S. Nihtianov, L. K. Nanver, and F. Scholze, "Stability characterization of high-sensitivity silicon-based EUV photodiodes in a detrimental environment," *IEEE Sensors J.*, vol. 13, no. 5, pp. 1–8, May 2013.

[7] A. Šakic, V. Jovanović, P. Maleki, T. L. M. Scholtes, S. Milosavljević, and L. K. Nanver, "Characterization of amorphous boron layers as diffusion barrier for pure aluminium," in *Proc. 33rd Int. Convers. MIPRO*, Opatija, Croatia, May 2010, pp. 26–29.

[8] A. Sakic, G. van Veen, K. Kooijman, P. Vogelsang, T. L. M. Scholtes, W. de Boer, W. H. A. Wien, S. Milosavljevic, and L. K. Nanver, "High-efficiency silicon photodiode detector for sub-keV electron microscopy," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2707–2714, Oct. 2012.

[9] A. Gottwald and F. Scholze, "Advanced Si radiation detectors in the VUV and EUV spectral range," in *Smart Sensors and MEMS*. Cambridge, U.K.: Woodhead Publishing Limited, 2013, pp. 102–123.

[10] V. Mohammadi *et al.*, "VUV/low-energy-electron Si photodiodes with post-metal 400 °C PureB deposition," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1545–1547, Dec. 2013.

[11] Q. Lin, K. R. C. Mok, E. Charbon, L. K. Nanver, M. Aminian, and E. Charbon, "UV-sensitive low dark-count PureB single-photon avalanche diode," in *Proc. IEEE Sensors*, Baltimore, MD, USA, Nov. 2013, pp. 1–4.

[12] E. Charbon, "Towards large scale CMOS single-photon detector arrays for lab-on-chip applications," *J. Phys. D, Appl. Phys.*, vol. 41, no. 9, p. 094010, May 2008.

[13] F. Scholze, H. Rabus, and G. Ulm, "Mean energy required to produce an electron-hole pair in silicon for photons of energies between 50 and 1500 eV," *J. Appl. Phys.*, vol. 84, no. 5, pp. 2926–2939, Sep. 1998.

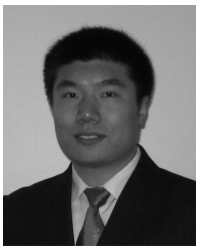
[14] F. Scholze, H. Henneken, P. Kuschnerus, H. Rabus, M. Richter, and G. Ulm, "Determination of the electron–hole pair creation energy for semiconductors from the spectral responsivity of photodiodes," *Nucl. Instrum. Methods Phys. Res. A, Accel., Spectrometers, Detectors Assoc. Equip.*, vol. 439, nos. 2–3, pp. 208–215, Jan. 2000.

[15] V. Mohammadi, S. Ramesh, and L. K. Nanver, "Thickness evaluation of deposited PureB layers in micro-/millimeter-sized windows to Si," in *Proc. 27th Int. Conf. Microelectron. Test Struct. (ICMTS)*, Udine, Italy, Mar. 2014, pp. 194–199.

[16] V. Mohammadi, W. B. de Boer, and L. K. Nanver, "An analytical kinetic model for chemical-vapor deposition of pure-boron layers from diborane," *J. Appl. Phys.*, vol. 112, no. 11, p. 113501, 2012.

[17] S. M. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded *p-n* junctions in Ge, Si, GaAs, and GaP," *Appl. Phys. Lett.*, vol. 8, pp. 111–113, 1966.

[18] *TCAD*, Synopsys Inc., Mountain View, CA, USA. [Online]. Available: http://www.synopsys.com/Tools/TCAD, accessed 2007.
[19] R. H. Haitz, "Mechanisms contributing to the noise pulse rate of avalanche diodes," *J. Appl. Phys.*, vol. 36, no. 10, pp. 3123–3131, Oct. 1965.
[20] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron. Devices*, vol. 39, no. 9, pp. 2090–2098, Sep. 1992.
[21] S. Cova, M. Ghioni, A. Lotito, I. Rech, and F. Zappa, "Evolution and prospects for single-photon avalanche diodes and quenching circuits," *J. Modern Opt.*, vol. 51, nos. 9–10, pp. 1267–1288, Jul. 2004.
[22] E. Charbon and M. W. Fishburn, "Monolithic single-photon avalanche diodes: SPADs," in *Single-Photon Imaging*, P. Seitz and A. Theuwissen, Eds. Heidelberg, Germany: Springer-Verlag, Jul. 2011, ch. 7, pp. 123–156.
[23] S. Mandai, "Multi digital silicon photomultipliers for time-of-flight PET," Ph.D. dissertation, Dept. Elect. Eng., Math., Comput. Sci., TU Delft, Delft, The Netherlands, 2014.
[24] S. Cova, A. Lacaita, and G. Ripamonti, "Trapping phenomena in avalanche photodiodes on nanosecond scale," *IEEE Electron Device Lett.*, vol. 12, no. 12, pp. 685–687, Dec. 1991.
[25] M. W. Fishburn, "Fundamentals of CMOS single-photon avalanche diodes," Ph.D. dissertation, Dept. Elect. Eng., Math., Comput. Sci., TU Delft, Delft, The Netherlands, 2012.



Lin Qi received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2010, where he is currently pursuing the Ph.D. degree.

His current research interests include electrical analysis of silicon devices, in particular high-sensitivity silicon photodiodes such as single-photon avalanche diodes.

K. R. C. Mok received the Ph.D. degree in chemical engineering from the National University of Singapore, Singapore.

She is currently a Post-Doctoral Researcher with the Delft University of Technology, Delft, The Netherlands, where he was involved in the development of doping and surface passivation techniques for the fabrication of photodiode detectors and solar cells.

Mahdi Aminian received the M.Sc. degree from the Amirkabir University of Tehran, Tehran, Iran, in 2008.

He joined Advanced Quantum Architecture Group, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2009, as Doctoral Assistant. He is focused on Ge-on-Si single photon image sensors and Si deep junction sensors for near-infrared detection.

Edoardo Charbon (SM'10) received the Ph.D. degree in electrical engineering and electrical and engineering computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 1995.

He joined the Faculty of Delft Institute of Technology, Delft, The Netherlands, in Fall 2008, as a Full Professor, where he has been involved in VLSI design, succeeding P. Dewilde.

Lis K. Nanver (S'80–M'83) received the Ph.D. degree from the Delft University of Technology (TU Delft), Delft, The Netherlands.

She is currently a Professor with TU Delft, where she heads a research group on device/circuit integration for microwave and sensor applications.