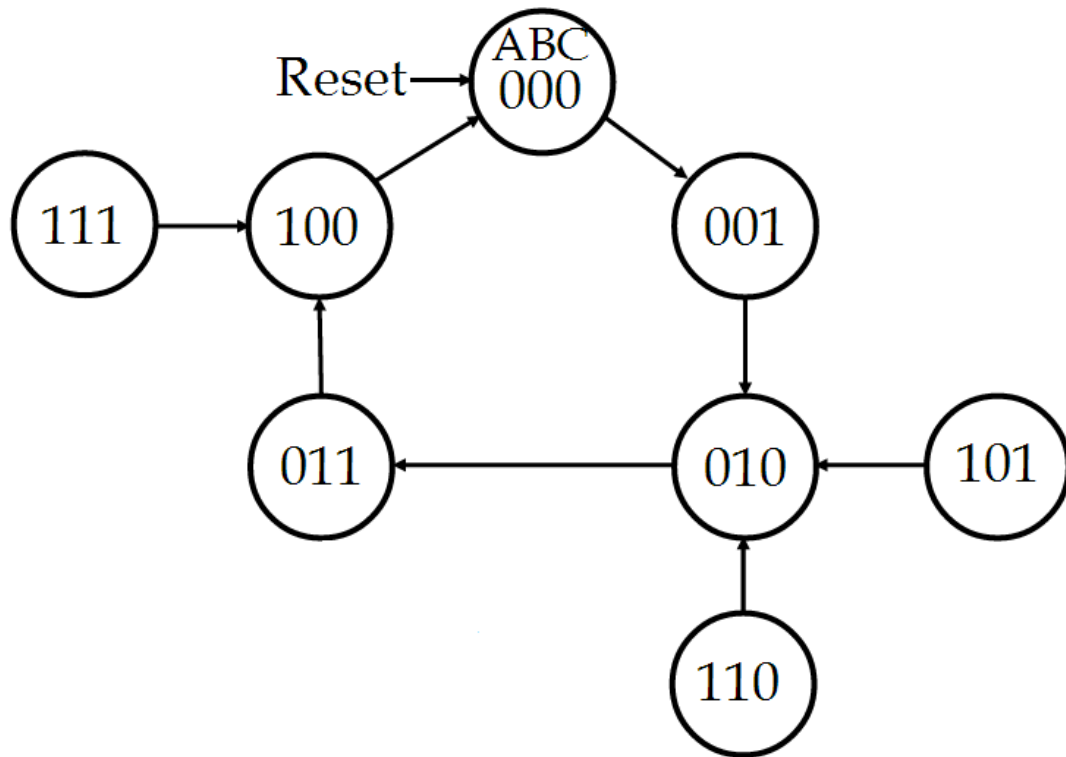


Explanation Document

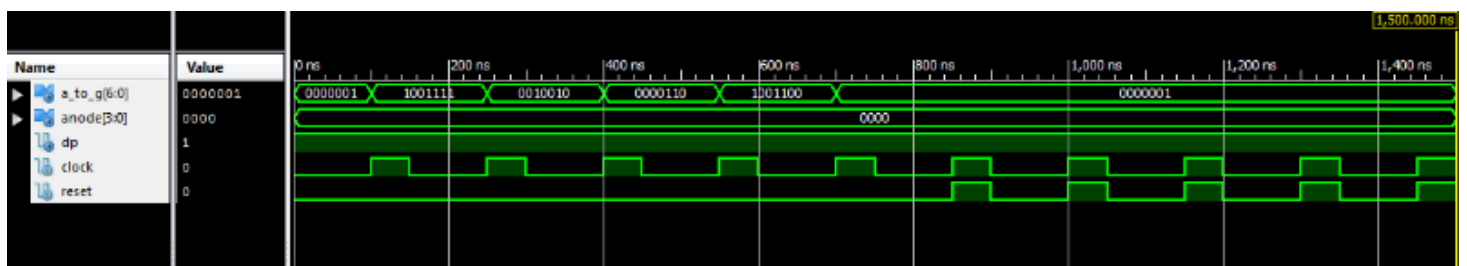
State Table

A B C	A'B'C'
0 0 0	0 0 1
0 0 1	0 0 1
0 1 0	0 0 1
0 1 1	0 0 1
1 0 0	0 0 1
1 0 1	0 0 1
1 1 0	0 0 1
1 1 1	0 0 1

State Diagram



Simulation



Circuit Mapping

